Received 27 November 2017; revised 19 January 2018; accepted 20 January 2018. Date of publication 2 February 2018; date of current version 23 February 2018. The review of this paper was arranged by Editor K. Shenai.

Digital Object Identifier 10.1109/JEDS.2018.2797951

InGaAs/AlAs Resonant Tunneling Diodes for THz Applications: An Experimental Investigation

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This work was supported in part by the Royal Society through a Brian Mercer Award, and in part by the EPSRC through "Future compound semiconductor manufacturing HUB" under Grant EP/P006973/1.

ABSTRACT This paper presents an experimental study of InGaAs/AlAs resonant tunneling diodes designed to improve the diode characteristics using five different device structures. A promising high peak to valley current ratio of 5.2 was obtained for a very low current density device. As expected, the measured results show a significant increase in the current density with thinner barriers and quantum well widths. This is, however, at the expense of an increase in the peak voltages for high peak current density devices. A 36-mV/μm^2 voltage deviation was found for a diode with a peak current density of 10.8 mA/μm^2 that we attribute to self-heating of the diodes, and which were confirmed using pulsed dc voltage tests. To demonstrate how the self-oscillation at low frequency can be eliminated, a 25 Ω resistor was integrated in parallel with the diodes. The experimental findings suggest that the partially stabilizing resistor is limited by the absolute value of the negative differential resistance. The equivalent circuit of the diodes was validated using on-wafer S-parameter measurements up to 40 GHz. An estimated high frequency operation limit of 2.7 THz was deduced for RTD sample #327.

INDEX TERMS InGaAs/AlAs heterostructure, RTDs, tunnelling device characterizations.

I. INTRODUCTION

Room temperature operating resonant tunneling diodes (RTD) are promising compact solid state electronic devices for use in the millimeter and sub-millimeter wave regions [1]. Such quantum based diodes have the capability of supporting high switching speed, exploiting its unique feature of negative differential resistance (NDR) [2]. Among all heterostructure tunneling diodes, double barrier InGaAs/AlAs RTDs, have been intensively investigated [3]–[6]. This includes numerical modeling, improvement in fabrication process and significant progress in THz wave applications. So far, the highest fundamental oscillation of an integrated RTD emitter achieved has reached approximately 2THz [7]. Due to rapidly growing trends in data rates for wireless communications, an implementation of a transmitter utilizing resonant tunneling diode capable of 34Gb/s data rates was recently reported [8]. To satisfy these increasing demands, downscaling of device sizes to submicron features is required to further minimize the intrinsic RTD capacitance, providing high speed operation beyond 1 THz [9]. To this end, achieving a useful indoor propagation distance requires a high output power source at such frequencies. This can be accomplished in two ways: first by improving the peak current density (J_P) and second by reducing the electron intraband transit time. For high J_P, wide band gap energy III-nitride RTDs have been demonstrated [10], [11]; however, GaN-based devices still suffer from lack of reproducibility, mostly attributed to deep energy level trapping centers, which in turn degrade the peak to valley current ratio (PVCR) [12], [13]. By contrast, previous work using pseudomorphic InGaAs/AlAs/InAs and thin and deep quantum well (QW) InGaAs/AlAs RTDs demonstrated high current densities of 4.5 and 14.5mA/μm^2 respectively [14], [15] as well as tens of femtoseconds transit times [15], [16]. As a key parameter of tunneling devices performance, f_{max} (maximum oscillation frequency) is strongly equivalent circuit parameters dependent, and depends in particular on the absolute value of the negative

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TABLE 1. DC and RF characteristics of different RTD structures.

	Design parameters			Extracted from the measured data					Calculated	
RTD Sample	t_s (nm)	t_b (nm)	t_w (nm)	J_P (mA/μm²)	PVCR	$\|G_{RTD}\|$ (mS)	Rs (Ω)	C_{RTD} (fF)	f_{max} (THz)	Max RF Power (μW)
276	20	1.6	4.5	0.08	5.2	1.4	2.2	30	0.13	18
277	20	1.3	4.5	0.26	3.2	3.8	2.2	30	0.22	37
300	5	1.2	4.5	1.1	3.8	19.6	1.6	36	0.48	166
302	5	1.1	4.5	3.7	3	76	2	33	0.86	380
327	5	1.1	3.5	10.8	4.9	260	1.6	30	1.64	1200

differential conductance (G_{RTD}). Thus investigating as well as improving the RTD's DC and RF characteristics is important for RF circuit implementation. There is a compromise to be struck between achieving high J_P and the complexity of the epitaxial growth process, for example using graded spacers or cap layers or/and emitter layer with quaternary materials for lower voltage bias [17], [18].

This work; however, shows that high current density RTDs can be obtained with relatively uncomplicated epitaxial layer structures. It also concentrates on a comparative investigation of five different diode epitaxial structures. Our approach is to quantitatively analyze the influence of high J_P on peak voltage shift with variations in mesa sizes of the diodes, which has not been discussed yet, and demonstrates that shift seen in the peak voltage V_P with high current density is due to a self-heating effect. Another important aspect also studied was the effect of a partially stabilizing resistor value on the negative differential conductance of the RTDs. The equivalent circuit of the diodes was experimentally validated using on-wafer S-parameter measurements up to 40 GHz. Further discussions including RF characteristics and optimum design of an RTD Epilayer structure to reduce the peak voltage shift is also presented in this work.

II. DEVICE STRUCTURE AND FABRICATION

Five RTD structures, which were grown on lattice-matched semi-insulating InP substrates using Solid Source Molecular Beam Epitaxy (SSMBE), were investigated. The samples, in these runs, are denoted as XMBE#276, #277, #300, #302 and #327, depending on the variation in their DBRTD structures and both spacer regions. The epitaxial stack of the structures is shown in Fig. 1. Dimensions of the DBQW (double barrier quantum well) and spacer layers are tabulated in Table 1 and all other dimensions are indicated in Fig. 1 and are similar for all RTDs. The devices were fabricated using standard i-line photolithography and utilizing both dry and wet etching techniques. Self-aligned diode mesas were first formed using reactive ion etching (RIE) for the top contacts. The bottom contacts were then deposited allowing wet etching of the self-aligned air-bridges and device isolation to be carried out. The non-alloyed ohmic contact scheme used was thermally evaporated Pd/Ti/Pd/Au for both upper anode and lower cathode electrodes. In spite of the fact that molybdenum-based contacts to n-type InGaAs give a low specific contact resistance (ρ_c) of $(1.1 \pm 0.9) \times 10^{-8}$ Ω.cm² [19], transmission line model measurements for the non-alloyed ohmic contact scheme of Pd/Ti/Pd/Au used in this work showed an equivalent ρ_c value of 1.3×10^{-8} Ω.cm², essentially comparable. The inset in Fig. 1 shows an SEM image of the RTD sample XMBE#302 with a designated mesa size of $1 \times 2\mu m^2$ including top and bottom electrodes.

III. DEVICE CHARACTERISTICS

A. DEVICE DC CHARACTERISTICS

The DC characteristics of the diode samples XMBE#300, #302 and #327 are depicted in Fig. 1. As expected, sample #327 has the highest J_P of 10.8mA/μm² due to the thin well and barriers, followed by sample #302 as illustrated in Table 1. The key DC characteristics parameters are tabulated in Table 1 including J_P, PVCR and absolute value of the negative differential conductance (G_{RTD}). The latter parameter can be approximately expressed as a function of the voltage span (ΔV) and current width (ΔI); $(3/2)(\Delta I/\Delta V)$ [20]. Apart from the peak current density of the RTDs; all other parameters are calculated for 4μm² device areas. Asymmetrical IV characteristic of the RTDs were observed, mainly attributed to the existence of both "normal" and "inverted" InGaAs-AlAs interfaces and potentially any unintentional variation in barrier thickness which are possible in these multi-interfaces structures.

As the transmission probability of the RTDs is exponentially dependent on the barrier thicknesses, this might exacerbate this effect. Lower doping profile in the n^+-$In_{0.53}Ga_{0.47}$ As ohmic bottom layer compared with the top one might also have a small effect on the I-V symmetry.

A thicker t_b from the collector side of sample #276, can suppress additional current through the collector barrier [21], as compared with sample #277 contributing to the increase in PVCR. However, this is at the expense of a reduction in J_P. I-V characteristics of the latter samples are shown in Fig. 2. For high G_{RTD}, the width of the barriers for sample #302 was grown with a thickness of 1.1nm, providing a significant increase in current density. Table 1 shows good device characteristics including a high PVCR of 5.2 exhibited by sample #276 despite its very low current density. A comparable PVCR value was achieved for sample #327 with a significant increase in J_P and G_{RTD} obtained through decreasing both well and barriers thicknesses. However, the experimental data indicates that a high PCVR can still be obtained in relatively thicker wells. Since a thick spacer

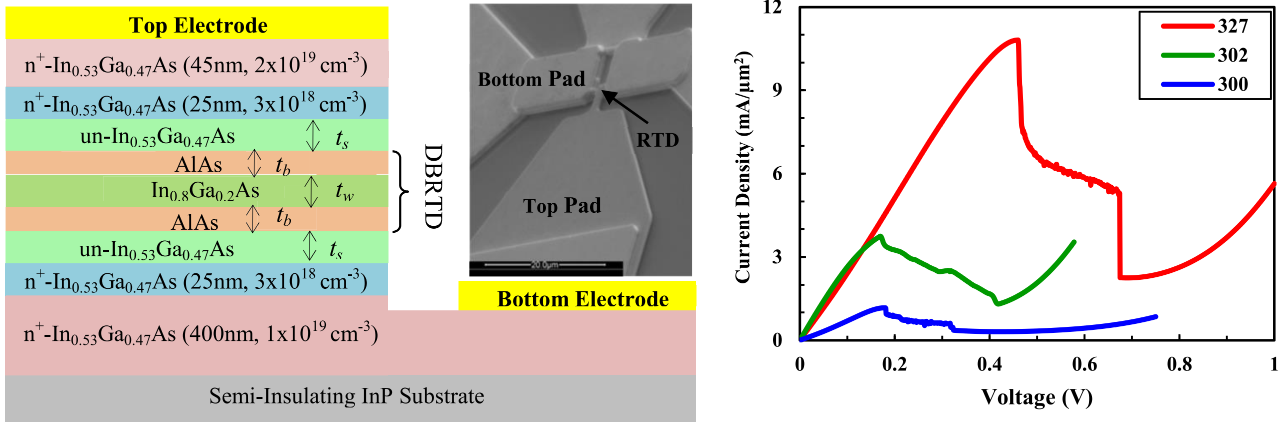

FIGURE 1. Left side: typical RTD structure including layer dimensions of the double barrier quantum well layers and spacers regions which are varied in the five structures investigated. Inset: SEM image of an RTD with a mesa size of 1 × 2μm^2. Right side: current density of the RTD samples XMBE#300, #302 and #327.

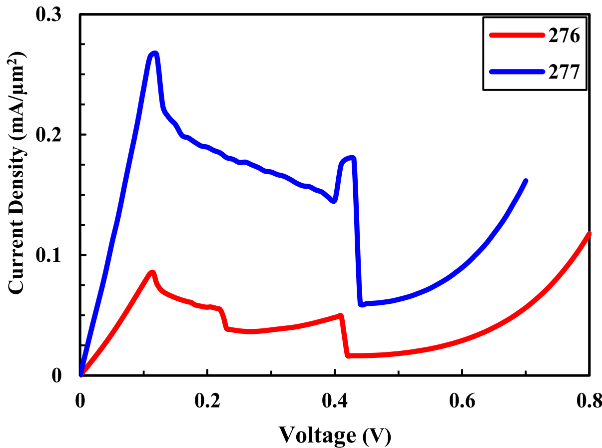

FIGURE 2. Current density of the RTD samples XMBE#276 and #277.

region of 20nm for sample #276 offers fewer carriers scattering events, the PVCR has been improved. Additionally, further reduction in valley current of sample #276 is due to the existence of a wide collector barrier thickness of 1.6nm. The incoherent tunneling mode caused by scattering mechanisms occurs because of interactions with impurities or/and defects encountered by the injected electrons [22]. Such an RTD characteristic emphasizes that this performance is undeniably important in implementation of RF circuit amplifiers with submilliwatt level dc power consumption [23], [24]. Conversely, this sample would not be suitable as a terahertz emitter due to its rather low estimated output power.

There is a trade-off between accomplishing a high J_P and the dependency of PVCR on spacer and DBQW dimensions. A well-designed asymmetrical RTD structure could effectively compromise between these key parameters, for example a thin t_b with a wide spacer layer from the emitter side alongside relatively thick t_b with a moderate spacer thickness from the collector side could contribute to increase in J_P whilst maintaining a high PVCR. A small degradation in the PVCR as the device size gets smaller was experimentally noticed, as a result of anisotropic side-wall due to the dry etching process as shown in Fig. 3. The argument for this is attributed to a parasitic sidewall current, thus smaller undercut with appropriate surface passivation could improve scalability of the submicron devices [25]. It is known that reducing the quantum well thickness makes the separation between the first and second resonant levels inside the well larger thereby improving the PVCR and with a considerable increase in J_P. Boosting of these two parameters was achieved for sample #327 which had a relatively simple epitaxial structure. Accordingly, a high G_{RTD} of 260mS was obtained. The structure simplicity mainly refers to the fact that no graded or quaternary layers were used. Both of these would be extremely difficult to control in a manufacturing environment since the exact compositions and grading would need to be achieved over very small distances. The structures we present rely exclusively on timing of shutter without any change in temperature of the effusion cells during growth, making the structures much more reproducible, which are important for tunnel devices were the characteristics tend to depend exponentially on thicknesses. The DC characteristics of RTDs have been examined in great detail in [16], [17], and [26] and will not be discussed further here.

From the experimental data, shifting of the peak voltage with peak current density of the diode was observed. Though such influence was briefly discussed in [27], clarifying it has not been quantitatively presented. This aforementioned work claimed that a drop in voltage at the contact layer could be the reason behind this behaviour. It is important to point out that the ohmic contact resistance (and overall resistance) of the RTDs decreases as device dimension increases. Our experimental data reveals different trends for each RTD sample which are extremely peak current density dependent. Deviation in V_P with mesa size was found to be negligibly small for devices with low J_P (samples: #276, #277 and #300).

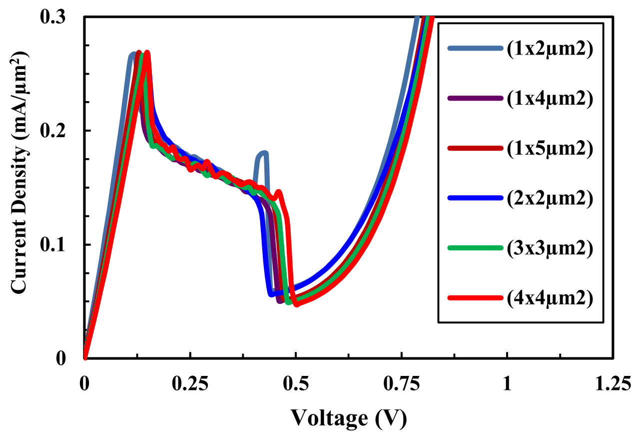

FIGURE 3. Current density of RTD sample XMBE#277 showing a very small variation in the valley current for small mesa diodes in comparison with large ones.

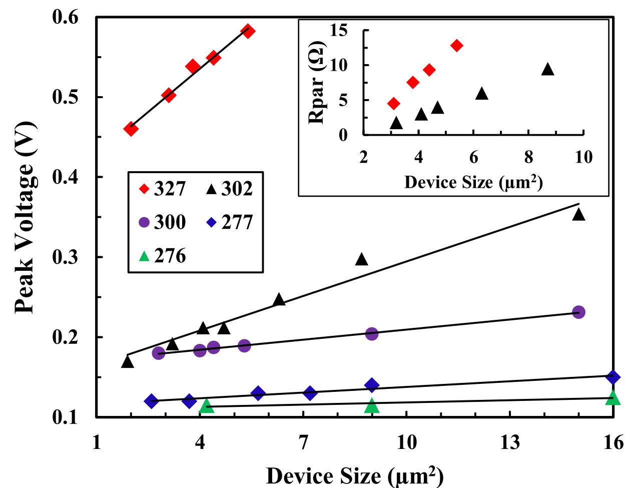

FIGURE 4. Peak voltage of the InGaAs/AlAs RTDs as a function of device sizes for different peak current density samples. The peak voltages were obtained from the measured I-V characteristics of the diodes. Inset: estimated parasitic resistance as a function of diode size for RTD samples XMBE#302 and 327 (all other samples were excluded from the graph due their very low associated R_{par}).

On the other hand, it rises considerably for high peak current density RTDs (samples: #302 and #327) as shown in Fig. 4. These latter diodes have a deviation in V_P in the range of 14 and 36mV/μm^2 respectively. These findings are interpreted as follows: the diodes with high J_P (and higher areas) are heated up due to the high current passing through them, causing excess carriers scattering and in particular throughout the entire doped layers. Reduction in the mobility of the electrons consequently occurs, leading to an additional parasitic resistance associated with the series resistance of the diode which further increases with mesa size of the device. A polynomial fit to the RTDs peak voltage was used to estimate the parasitic resistance (R_{par}). The intrinsic series resistances of the devices were taken into account in the modeled IV curves. The simulation data shows that R_{par} is in the range of 1.4 and 3.6 Ω/μm^2 for samples XMBE#302 and 327 respectively as depicted in Fig. 4 while all other diode samples had very low parasitic resistances depending on their current densities (i.e., $< 0.5\ \Omega/\mu$m^2). To support this explanation, a 1μm width TLM (transmission line model) air-bridge using Pd/Ti/Pd/Au with a thickness of 10/20/20/700 nm were fabricated. The measured data showed that an air-bridge passing a 100mA current has a very low voltage drop of 3.8mV/μm. This multilayer air-bridge can handle a current exceeding 100mA for a 30μm length. With this in mind, the self-heating resistance is clearly caused by the RTDs themselves. Therefore to minimize the variation in peak voltage and thus ensure very small additional resistance for high current density diodes, submicron devices are necessary.

Further measurements using pulsed dc voltage bias (P) were carried out and from which the self-heating problem was clearly seen. The time period of the voltage was varied from 10 to 500ms with a duty cycle (DuC) of 10%. These measurements did not show any significant differences in the current-voltage characteristics of the low current density devices (i.e., #277) as shown in Fig. 5(a). Note that the set up oscillations present at DC are absent during pulse measurements. On the contrary, the high current density device sample #302 shows a marked trend in which higher current (less resistance) was obtained as depicted in Fig. 5(b). The enhancement in J_P was about 60% with a duty cycle and period time of 10% and 10ms respectively. However, it is noticeable that the PVCR deceases, particularly with long period times. Different duty cycles were also tried but did not reveal any further information. Due to equipment limitations, large mesa area devices of sample #327 could not be measured.

To the best of our knowledge, an RTD structure design, in which the self-heating issue effect is insignificant, has not been reported to date. However, the importance of minimizing V_P is important for relatively large device sizes for low DC power dissipation in RTD integrated circuits. While further increase of the doping profile in the top cap layer can reduce the specific contact resistance and hence minimize voltage drop at the interface, minimizing the spreading resistance is far more important for lowering the peak voltage as well as yielding efficient high frequency performances.

A graded InGaAs emitter layer is an alternative way exploited to reduce the bias voltage due to occurrence of the alignment between the resonant state in the well and conduction band edge of the emitter at a low bias voltage [28]. This is however, at the expense of an increase in complexity of the growth process.

One more important aspect that has also been studied in this work is the influence of an integrated resistor value on the characteristic of the RTDs. A 25Ω NiCr shunt resistor (R_{sh}) with a 50Ω/□ sheet resistance was sputtered into both sides of the coplanar waveguide (CPW) in parallel with the

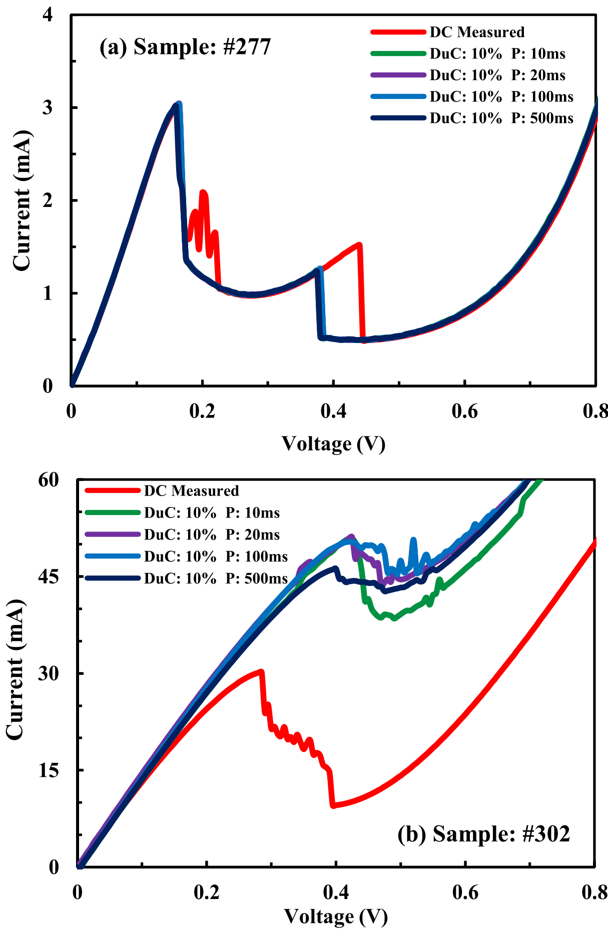

FIGURE 5. RTD I-V characteristic with various pulse widths of the applied DC voltage (a) Sample #277 with a 11.4μm^2 mesa size, (b) Sample #302 with an mesa size of 8μm^2.

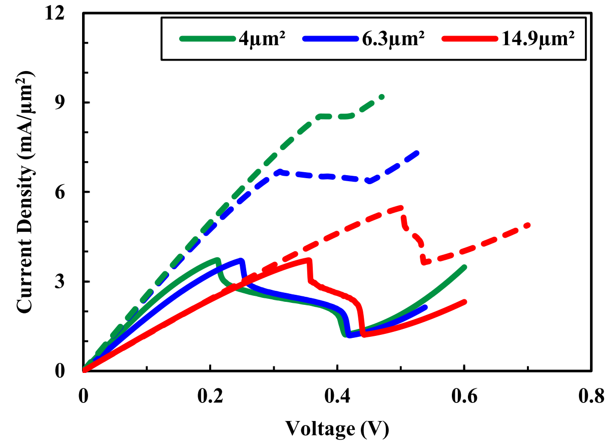

FIGURE 6. Current density of different RTD sizes for sample #302 with and without a 25Ω NiCr shunt resistor plotted in dash and solid lines respectively.

diodes. The measured data is shown in Fig. 6. It is apparent from the graph that the negative conductance region almost vanishes for a 4μm^2 device size, meaning that a 25Ω resistor is an overestimate to suppress the low frequency parasitic oscillation. Thus, optimizing R_{sh} was found to be consistent with theoretical analysis in the literature as R_{sh} is constrained by G_{RTD} (i.e., $R_{sh} < 1/|G_{RTD}|$) [17], [29]. A large deviation in V_P depicted in Fig. 4 is not only caused by self-heating problems of the RTDs but also due to current dividing between the resistor and diode, leading the peak current density to occur at higher V_P.

B. RTD RF CHARACTERISTICS

The RTDs were fabricated into one port 50Ω GSG (ground signal ground) coplanar waveguide (CPW) layouts including open and short structures. The measurements were performed on-wafer using a Vector Network Analyzer (VNA, Anritsu 37369A) up to 40GHz. It is noteworthy mentioning that due to self-oscillation issues in the NDR region, care was taken to produce stable scattering parameters data, through attenuating the input RF power to about −30 dBm [30]. Generally speaking, continuous scaling of the lateral dimensions of the tunneling devices for high frequency operation, which in turn minimizes the size of the equivalent circuit parameters, makes the de-embedding method more complicated due to the existence of several parasitic elements. This is problematic for >100GHz frequency measurements in which the effects of the fringing capacitances between the air-bridge finger and InGaAs bottom ohmic layer as well as between the bridge and CPW are not trivial [31]. However, up to 40GHz a simple equivalent circuit model and straightforward extraction method are adequate especially with relatively large emitter device sizes (i.e., 4μm^2).

Thus, for the sake of simplicity, the intrinsic junction capacitance of the devices (C_{RTD}) was extracted after the parasitic bond pads surrounding the RTDs were carefully de-embedded using a two-step de-embedding technique [32]. The well-known diode's equivalent circuit model was realized in advanced design system (ADS) software as shown in Fig. 7. It was validated through a fitting approach with the experimental reflection coefficient data as depicted in Fig. 8. The measured and simulated results are in good agreement. Additionally, the derived $R_s + R_{RTD}$ (R_{RTD} is the junction resistance of the RTDs) in the positive differential region (PDR) calculated from $\partial V/\partial I$ of the measured I-V characteristic, is well matched to the extracted values from the S_{11} data. The series resistance of the devices (R_s) is normally comprised of the top ohmic contact resistance (ρ_c/RTD_{Area}), resistance due to epi-layers ($R_{epi-layers}$) and spreading resistance (R_{spr}), caused by the current flowing through the bottom InGaAs highly doped layer in a horizontal path [17].

$$R_s = \frac{\rho_c}{RTD_{Area}} + R_{epi-layers} + R_{spr} \tag{1}$$

R_s was first calculated as illustrated in Table 1 and then used to fit with the experimental S-parameters data. As discussed previously, a specific contact resistance of 1.3×10^{-8} Ω.cm^2 was obtained for all samples utilizing TLM measurements.

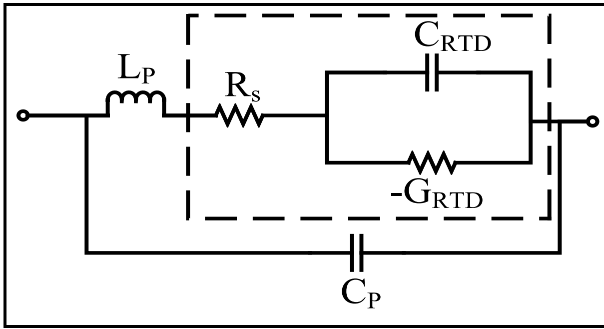

FIGURE 7. Typical equivalent circuit of the RTDs including the embedded parasitic elements (pad capacitance and inductance, C_P and L_P respectively) and the intrinsic RTD equivalent circuit (dash lines).

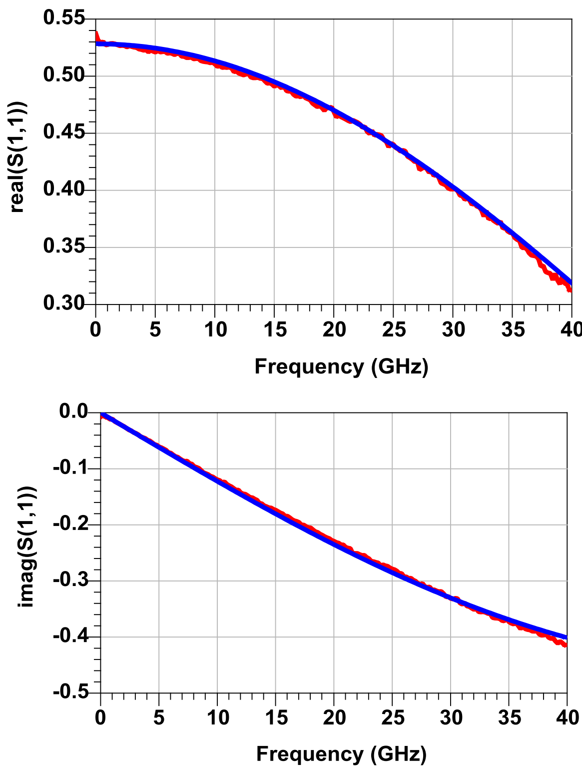

FIGURE 8. Real and imaginary parts of the equivalent circuit and S-parameters Measurement of the RTD sample #277 with a mesa size of 4μm² (red and blue lines are the measured and simulated data respectively).

Two terminal devices operating in the terahertz regime have been experimentally demonstrated to have frequency dependent series resistances [33]. This dependency was attributed to two major effects; firstly the electromagnetic (EM) field effect which interacts with the diode itself and additional pads surrounding the diode. It has been reported that it is difficult to fully understand the geometry-dependent EM field with a conventional series resistance model [34]. However, to analytically extract the mm-wave/THz diode's equivalent circuit model including losses caused by the EM field interaction, numerical methods are necessary. In addition, thinning the diode's buffer layer is one possible way to minimize field-coupling issue [31]. Secondly, the spreading resistance of the device increases with frequency due to a decrease in the bottom ohmic conductivity as the frequency increases [35]. An effective approach used to remedy this is to minimize the distance between the ohmic InGaAs layer and the bottom electrode to submicron scale. As conventional i-line photolithography technology is restricted to $\sim 1\mu$m resolution, optimizing this key distance can be carried out through exploiting a trilayer soft reflow technique as reported previously [5]. In practice, the impact of both aforementioned issues is insignificant for parameters extraction below 100GHz measurements.

For the RTD, C_{RTD} includes both the depletion region (C_{dep}) and quantum capacitances (C_Q) as given by $C_{RTD} = C_{dep} + C_Q$ [17]. The depletion region capacitance can be estimated using $C_{dep} = \varepsilon_o\varepsilon_r A/d$, where ε_o, ε_r, A and d are the free space permittivity, the relative dielectric constant, the RTD mesa size and thickness of the double barriers quantum well region including emitter and collector spacers respectively. An increase in the negative charge in the accumulation region and quantum well, which counter balances the positive charge in the depletion region, is the main reason behind introducing such an associated quantum capacitance. It is formulated as $C_Q = |G_{RTD}|\tau_{RTD}$, where τ_{RTD} is the transit time through the double barriers quantum well (τ_{dwell}) and collector depletion region (τ_{dep}) [36]. Under this consideration, the carrier transit time in a resonant tunnelling diode is expressed as [17]:

$$\tau_{RTD} = \tau_{dwell} + \frac{\tau_{dep}}{2} \tag{2}$$

The key factor of $\frac{\tau_{dep}}{2}$ has been mathematically derived for collector depletion region transit time in the analysis of transistors [37]. It would be worthwhile highlighting that continuous downscaling of a high G_{RTD}RTD to $< 1\mu\text{m}^2$ can contribute to an increase in the quantum capacitance over the depletion region one. From the small signal equivalent circuit of the RTD, the theoretical maximum oscillation frequency has been derived by Brown *et al.* [38]. As the quantum inductance does not have a significant impact on the upper operating frequency limit, it can be approximately expressed as:

$$f_{max} = \frac{|G_{RTD}|}{2\pi C_{RTD}}\sqrt{\frac{1}{R_s\,|G_{RTD}|} - 1} \tag{3}$$

From (3), minimizing the passive elements including R_s and other parasitic components is fundamental in ensuring an efficient operation in the mm-wave/THz regions. Due to the 5 nm spacer thicknesses for sample #300, a large value of C_{RTD} was obtained. For both, the thin barrier RTD sample #302 and the 3.5nm well thickness device #327, there is a decrease of their respective capacitances, leading to a significantly increase in f_{max} exceeding 0.8 and 1.6THz respectively as illustrated in Table 1. This is an important consideration for manufacturing and commercial applications

TABLE 2. Calculated transit time and intrinsic high frequency limit for the RTD samples.

RTD Sample	t_s (nm)	t_b (nm)	t_w (nm)	τ_{RTD} (fs)	$f_{int\text{-}limit}$ (THz)
276	20	1.6	4.5	1880	0.13
277	20	1.3	4.5	800	0.31
300	5	1.2	4.5	410	0.61
302	5	1.1	4.5	260	0.96
327	5	1.1	3.5	92	2.7

and a key advantage of RTDs for achieving such high f_{max} values utilizing a relatively large RTD size of $4\mu m^2$ compared with other technologies (i.e., HEMTs and HBTs), for instance where extremely small, nanometer scale gate lengths are required for HEMTs and thin base and collector contacts for HBTs.

Assessments of the suitability of our RTD structures for use as terahertz emitter requires an estimation of carriers' transit time in both DBQW and collector depletion region. From a first glance of the data in Table 1, samples XMBE#302 and #327 should be suitable for relatively high output power oscillators as a result of their high current density and so further discussion in this section is mainly concentrated on these RTD samples. The quantum based capacitance and carrier transit time in an RTD ($\tau_{dwell} + \tau_{dep}/2$) for small signal analysis at low frequency (where $\omega\tau_{dwell}$, $\omega\tau_{dep}/2 \ll 1$) can be approximately expressed as [39]:

$$C_Q \simeq (\tau_{dwell} + \frac{\tau_{dep}}{2})G_{RTD} \quad (4)$$

The evaluation of the term $\tau_{dwell} + \tau_{dep}/2$ has been found from the measured data of the extracted intrinsic capacitance values of the RTDs. C_Q was first obtained as stated in [39] from which τ_{RTD} was then estimated as shown in Table 2. It is noteworthy to point out that a moderate spacer thickness is necessary as a compromise between an optimum transport time across the depletion region and the capacitance of the device. Regardless of limitation in high frequency operation caused by parasitic elements of the diodes, the intrinsic high frequency limit due to both tunneling and depletion region delay times is given by [20]:

$$f_{int-limit} = \frac{1}{4(\tau_{dwell} + \frac{\tau_{dep}}{2})} \quad (5)$$

Since the delay time in double barriers RTDs is negative differential resistance dependent, a relatively low frequency operation limit was obtained for samples #276 and 277. As expected, sample #327 has the highest $f_{int-limit}$ followed by sample #302 as a result of their thinner well and barriers as shown in Table 2. These particular RTDs are promising candidates for mm-wave/THz applications. Further reduction in the thickness of the quantum well would significantly increase $f_{int-limit}$.

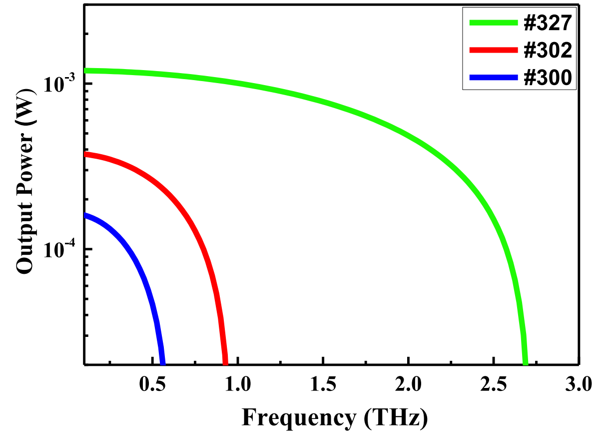

FIGURE 9. Calculated output power as a function of operating frequency for RTD samples #327, #302 and #300.

For an efficient THz RTD emitter, the difference between peak and valley voltages (ΔV) is a key driver in maximizing the RF output power. With this in mind, producing a peak resonance at lower bias voltage is also important for low dc power consumption. The maximum output power was calculated using $P_{max} = (3/16)\Delta I \Delta V$ [40], and was found to be 1.2mW for diode sample #327. However, in practice, the actual output power is degraded as a consequence of a decrease in G_{RTD} with frequency (i.e., long transit delay time), so the above formula becomes [41]:

$$P_{RF} = (3/16)\Delta I \Delta V \cos \omega\tau_{RTD} \quad (6)$$

Accordingly, Fig. 9 shows the predicted output power as a function of frequency for devices #300, #302 and #327 with different barriers and well thicknesses. As depicted in Table 2, sample #327 can theoretically operate up to 2.7THz. This clearly emphasizes that high J_P RTDs with an adequately large value of PVCR have the potential for switching beyond 2THz.

IV. CONCLUSION

An experimental investigation of InGaAs/AlAs resonant tunneling diodes aimed at high current density devices was carried out. This was performed using five different heterostructure devices including DC and RF characteristics comparisons and equivalent circuit parameters' analysis. An important result obtained in this work is the achievement of a high PVCR of 5.2 for a very low current density RTD. The measured data reveals that the current density is exponentially dependent on barriers and quantum well thicknesses. The increase in J_P, however, occurs at the expense of a shifting in the peak voltages with peak current density of the RTDs which increases even further due to self-heating effect suggesting submicron mesa device sizes to suppress this effect. Investigation of integrated shunt resistors indicates that their optimum values are constrained by the diode's negative differential conductance and thus must have

appropriately designed values according to the particular RTD used.

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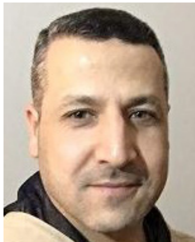

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