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Interface Coupled Photodetector (ICPD) With High Photoresponsivity Based on Silicon-on-Insulator Substrate (SOI)

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ABSTRACT A CMOS-compatible photodetector with high responsivity is reported. This device utilizes the unique interface coupling effect found in fully depleted silicon on insulator (SOI) MOSFETs. Unlike conventional SOI photodetectors, the proposed device shows higher photoresponsivity in thinner Si films due to stronger interface coupling, as confirmed by TCAD simulations. A prototype device fabricated with a simplified process flow achieves a record photoresponsivity up to 3.3×10^4 A/W.

INDEX TERMS Interface coupling effect, SOI/GeOI based photodetector, high photoresponsivity, imaging sensor arrays.

I. INTRODUCTION

The silicon-on-insulator (SOI) substrate has been an attractive platform for applications in electronics and photonics thanks to its unique advantages [1]–[6]. CMOS devices built on SOI have inherently low parasitic capacitance and low leakage currents, and thus are extensively used in radio frequency (RF) and low power consumption circuitry. Besides, the isolation of the top device layer from the bulk substrate makes the SOI device highly resistant to radiation, which is attractive for aerospace applications. Thanks to the low loss of infrared light and excellent confinement of light in the Si waveguide, the SOI substrate can also find applications in photonics. If made sufficiently responsive, SOI-based photodetectors could find many applications in space navigation and low-power imaging systems. As a bridge connecting electronic and photonic devices, the photodetectors also play an important role in electronic-photonic integrated circuits (EPICs).

In modern SOI CMOS, the top Si thickness is typically less than 100nm in order to suppress the short-channel effects (SCEs) and achieve aggressive scaling. But for photodetection purposes, this thin Si layer degrades the quantum efficiency and thus reduces the responsivity dramatically. A conventional SOI based *p-i-n* photodetector typically has very low responsivity, for example ~0.0075A/W as reported in [7]. For this reason, SOI-based photodetectors with internal gain have been studied extensively, such as the bipolar junction transistors [8], junction field effect transistors (JFETs) [9], [10], MOSFETs and gate-body tied MOSFETs [11]–[13], with reported responsivities as high as 2×10^4 A/W. However, many of these devices are built on sapphire to reduce optical losses and feature complex device structures, which increases production cost and impacts CMOS integration [12], [13]. Recently, an FD-SOI photodetector with excellent response was reported [14], [15], based on a $p-n$ photodiode embedded in the substrate to accumulate photogenerated electrons and thereby modulate the threshold voltage V_{th} of a MOSFET.

In this work, we propose and demonstrate a novel interface-coupled photodetector (ICPD) built on an SOI substrate. Unlike the aforementioned devices, the ICPD utilizes the interface coupling effect that is stronger in thinner SOI [16]–[18]. TCAD simulations are performed to study its operating mechanism and benchmark its photoelectric response. An in-depth study is performed to investigate the impact of operation voltage, dimensions and carrier lifetime on the performances. Further, ICPDs based on germanium-on-insulator (GeOI) are proposed for infrared detection and

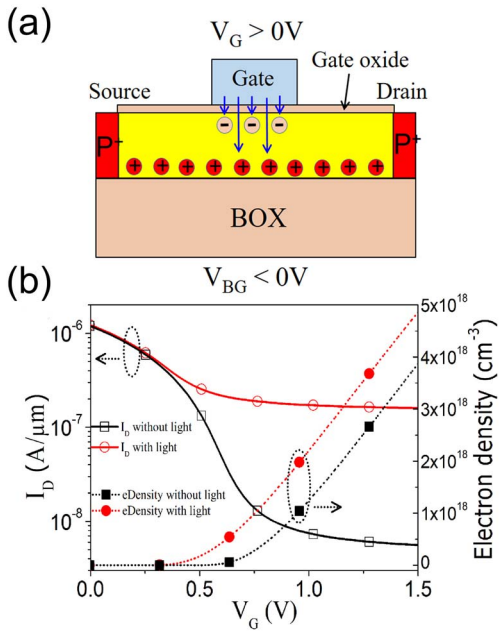

FIGURE 1. Schematic of the simulated ICPD with $V_D = -1$ V, $V_{BG} = -6$ V, $L_G = 1$ μm gate length, 2 μm gaps, 200 nm top silicon film and 500 nm BOX. (b) Simulation results comparing the evolution of drain current I_D and electron concentration *vs.* V_G in the dark and under illumination (50 μW/cm² intensity at $\lambda = 520$ nm).

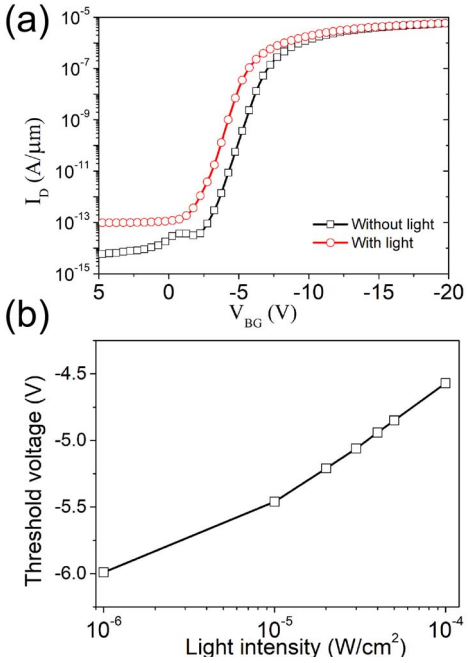

FIGURE 2. (a) $I_D - V_{BG}$ characteristics of the ICPD in cases with and without illumination. (b) Shift of back channel V_{th} as a function of optical illumination intensity.

an array ICPD architecture is proposed for image sensing. A simplified process flow is presented and the photoelectric characterization of fabricated unoptimized ICPDs agrees with simulations and shows a record responsivity of 3.3×10^4 A/W. The extremely high responsivity makes the device attractive for large-scale arrays, where the device area is restricted.

II. TCAD SIMULATION

A. OPERATING PRINCIPLE

TCAD simulation in Synopsys Sentaurus is performed to study the operating principle of the ICPD. The structure of the device is similar to a *p*-channel MOSFET except for the ungated regions between the gate and source/drain electrodes, see Fig. 1(a). The ungated regions are inserted to reduce the gate length while maintaining the total light reception area. This is helpful to improve the responsivity and response speed, as explained below in part Section II-C. A negative backgate bias ($V_{BG} < 0$) induces a hole conduction channel at the Si/buried oxide (BOX) interface (back interface). A positive bias applied on the top gate ($V_G > 0$) tends to deplete the hole channel through the interface coupling effect, and thus reduce the drain current I_D flowing at the back interface. This can be seen in Fig. 1(b) where increasing V_G reduces I_D dramatically (by two orders of magnitude for $0 < V_G < 1$V).

Figure 1(b) compares the electron density at the top interfacein the dark and under steady illumination (50 μW/cm² at wavelength $\lambda = 520$ nm).

The light generates extra electrons that accumulate at the top interface due to $V_G > 0$ and screen the electric field from the top gate, thereby reducing the interface coupling. With reduced interface coupling, the hole current at the back interface is restored, as shown in Fig. 1(b). Thanks to the high internal gain, the simulated photoresponsivity of the ICPD reaches 5.5×10^4 A/W under $V_G = 1.5$ V and $V_{BG} = -6$ V.

In the FD-SOI MOSFET, V_{BG} can be used to tune the threshold voltage V_{th} of the top channel by the interface coupling effect. In ICPD, the V_{th} of the back channel is affected by both front gate bias and light intensity. Figure 2(a) compares the $I_D - V_{BG}$ curves of the ICPD in dark and under illumination. The $|V_{th}|$ of the device with light is evidently reduced by the optical illumination. Figure 2(b) shows the shift in V_{th} as a function of light intensity, where the V_{th} is extracted at a constant $|I_D| = 10^{-8}$A/μm. We observe that $|V_{th}|$ shifts almost logarithmically with the light intensity.

The device configuration with front and back channels of opposite polarities is analogous to the capacitorless MSDRAM [19]. The operation of the ICPD is also similar to that of a *p*-type JFET. The electron layer induced by V_G at the top interface functions as the JFET gate controlling the bottom channel induced by V_{BG}. The photogenerated electrons accumulating at the top interface reduce the potential of the field-induced JFET's gate, see the comparison between Fig. 3(a) and (b). This is similar with applying a negative bias on the gate of a JFET, which would increase the hole current in the bottom channel, see Fig. 3.

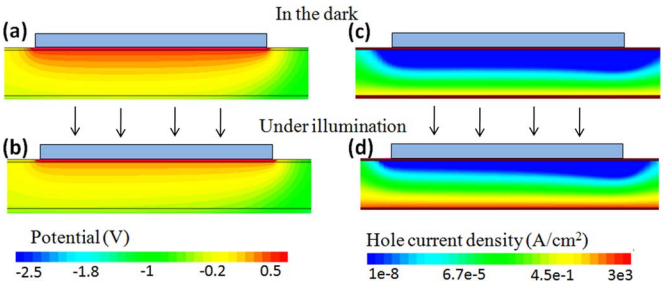

FIGURE 3. **Distribution of channel potential under the front gate in the dark (a) and under illumination (b), and the corresponding hole current densities (c), (d). The device biasing is $V_G = 1.5$ V, $V_{BG} = -6$ V and $V_D = -1$V.**

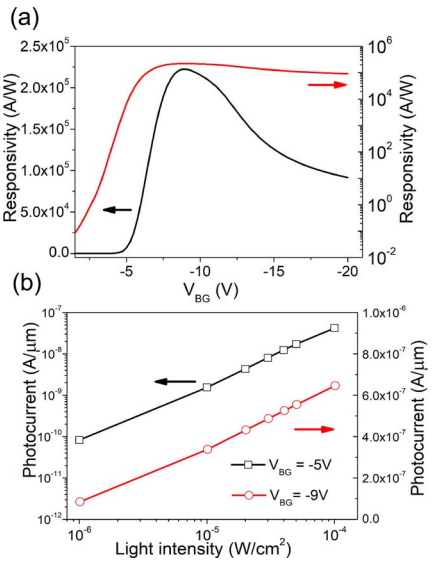

FIGURE 4. **(a) Relation between V_{BG} and responsivity of the ICPD. Note that the Y-axis is in linear and logarithmic scales on left and right sides respectively. (b) Relation between light intensity and output photocurrent.**

B. IMPACT OF BACKGATE VOLTAGE ON PERFORMANCE

As explained in Fig. 2, the threshold voltage V_{th} of the backgate MOSFET is shifted by the photogenerated electrons accumulating at the top interface. Thus, the photocurrent and responsivity can be strongly modulated by V_{BG}. The current of the device increases exponentially as V_{BG}decreases from 0 to −5 V in the subthreshold regime, which improves also exponentially the responsivity, see Fig. 4(a). As V_{BG} is reduced further below −5V, the backgate MOSFET operations in strong inversion (with linear dependence $I_D \sim (V_{BG} - V_{th})$), and thus the responsivity increases linearly and reaches a peak of 2.2×10^5 A/W at $V_{BG} = -9$ V. Further reduction of V_{BG} does not help, as the transconductance of the MOSFET begins to fall due to the mobility degradation.

Different photoresponse behaviors at different V_{BG} values translate into different relations between light intensity and photocurrent. Figure 4(b) plots light intensity *vs.* photocurrent at $V_{BG} = -5$ and –9 V. Since V_{th} falls logarithmically as light intensity increases, as seen in Fig. 2(b), we observe different behavior in subthreshold ($V_{BG} = -5$ V) and linear

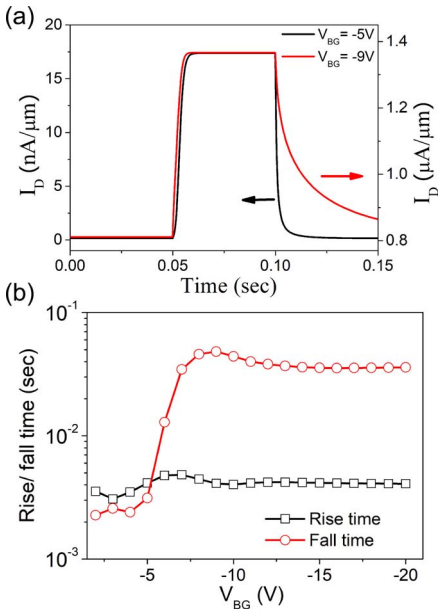

FIGURE 5. **(a) Comparison of the transient response under $V_{BG} = -5$ and −9 V; (b) Rise and fall times *vs.* V_{BG}.**

($V_{BG} = -9$ V) regimes. In the latter case, the nearly linear change in the photocurrent as the light intensity changes exponentially may be promising for high dynamic range applications.

Change of V_{BG} also impacts on the operation speed of the photodetector. Figure 5(a) compares the transient response of the device under an optical pulse. The fall time of the drain current under $V_{BG} = -5$ V is much shorter than that under $V_{BG} = -9$ V, whereas the rise times are equivalent.

In the subthreshold region, the photocurrent drops exponentially as the density of photoelectrons at the top interface decreases due to recombination. This is much faster than that in the linear region where the current falls linearly as the top electron density decreases. The relation between V_{BG} and rise/fall time in Fig. 5(b) clearly shows how the fall time evolves from subthreshold region to linear region. The rise time is determined by the photoelectron current charging the gate capacitance and is almost constant irrespective of V_{BG}.

C. IMPACT OF DEVICE DIMENSIONS ON THE PERFORMANCE

Device dimensions, such as gate length L_G and silicon channel thickness T_{si} are key parameters and can strongly affect the responsivity and rise/fall times. Figure 6(a) compares responsivity *vs.* V_{BG} for devices with three different L_G values and a fixed total length $L_{tot} = 5$ μm. As L_G is reduced from 2 to 1 μm, the responsivity improves significantly due to the increase of the trans- conductance, as in a conventional MOSFET. However, further reduction of L_G down to 0.2 μm degrades the responsivity because short channel effect reduces the gate control of the channel. Shorter gate length is helpful to reduce the rise/fall time, as the gate capacitance is reduced. Figure 6(b) shows the evolution of

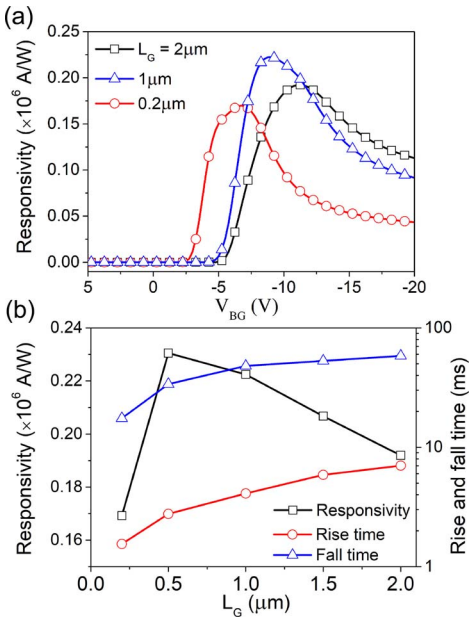

FIGURE 6. **(a) Responsivity *vs.* V_{BG} at three values of L_G for ICPDs with fixed $L_{tot} = 5$ μm. (b) Evolution of responsivity and rise/fall time with L_G. Note that the rise/fall time is extracted at V_{BG} where the responsivity reaches its peak.**

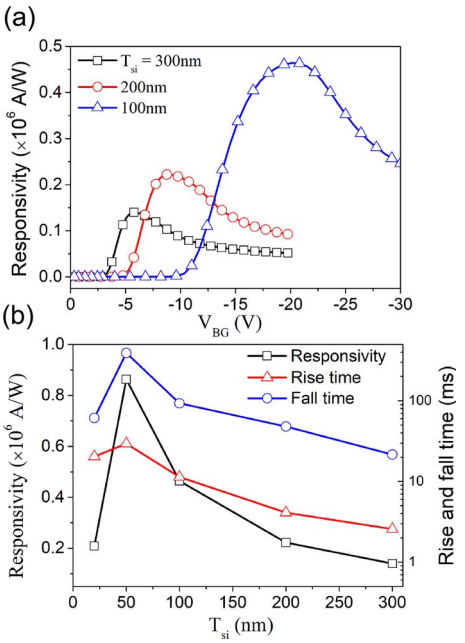

FIGURE 7. **(a) Responsivity *vs.* V_{BG} at various T_{Si}. (b) Evolution of responsivity and rise/fall times with T_{Si}. Note that the rise/fall times are extracted at V_{BG} where the responsivity reaches its peak.**

the responsivity and rise/fall times as a function of L_G. The responsivity reaches the maximum value (2.3×10^5 A/W) with $L_G = 0.5$ μm and then drops for smaller L_G due to short channel effects, whereas the rise and fall times decrease monotonically with L_G.

The change of film thickness T_{si} has an interesting impact on the device performance. It is well known that thinning down of top silicon layer in a SOI-based photodetector typically degrades the responsivity due to poor quantum efficiency. Conversely, in the ICPD, the reduction of T_{si} improves the responsivity, see Fig. 7(a). Though the photocurrent is reduced in a device with a thinner T_{si}, the interface coupling effect is strongly enhanced as in a normal FD-SOI MOSFET, which increases the internal gain and responsivity. Figure 7(b) shows that the responsivity trends up as T_{si} is decreased from 300 to 50 nm and reaches a maximum value about 0.9×10^5 A/W at $T_{si} = 50$ nm. The rise/fall times, however, degrade dramatically as T_{si} is reduced. This can be explained by the low photoelectron current charging the front gate capacitance. Further reduction of T_{si} to 20 nm drops the responsivity down to 0.2×10^5 A/W, which is due to the strong recombination between top electron and bottom hole layers in a thin Si film.

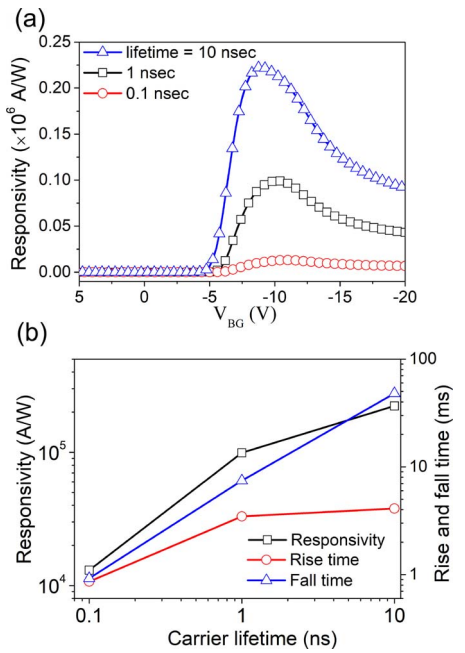

FIGURE 8. **(a) Responsivity *vs.* V_{BG} of ICPDs with various carrier lifetime. (b) Evolution of responsivity and rise/fall times with carrier lifetime.**

D. IMPACT OF CARRIER LIFETIME ON PERFORMANCE

Carrier lifetime also plays important role in determining the device performances. Figure 8(a) compares the simulated responsivity of the devices in which the carrier lifetime changes from 10 to 0.1 ns. The carrier lifetime determines the recombination rate of the top electron and bottom hole layer. A longer carrier lifetime reduces the recombination rate and thus increases the equilibrium photoelectron density at the top interface. This leads to a higher photocurrent and thus a higher responsivity. Conversely, shorter carrier lifetime is helpful to reduce the rise/fall time as shown in Fig. 8(b).

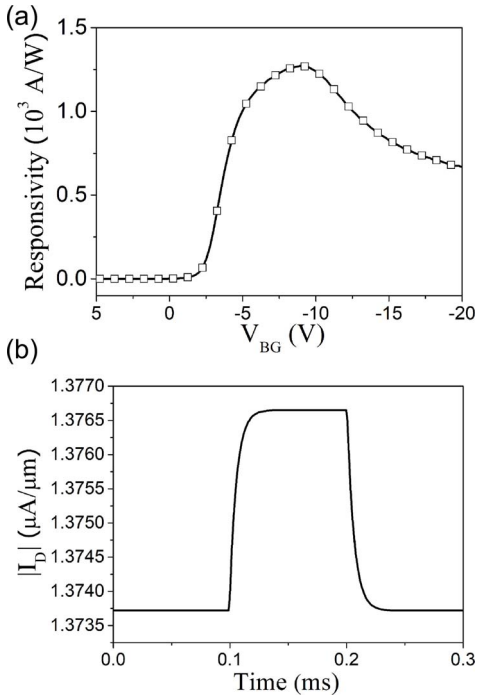

FIGURE 9. **(a) Relation between V_{BG} and responsivity of an ICPD based on a GeOI substrate under illumination of 50 μW/cm^2 at λ = 1550 nm. (b) The transient response of the GeOI ICPD.**

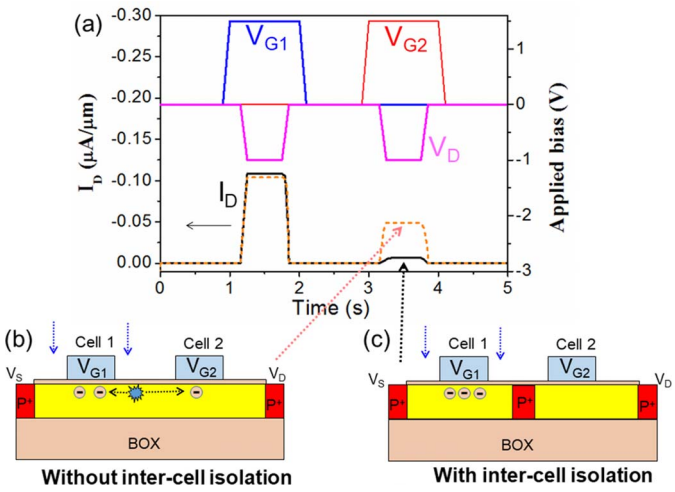

FIGURE 10. **(a) The operation of an ICPD array with 2 cells. (b) Schematic view of the simulated ICPD array with 2 cells and (c) the ICPD array with inter-cell isolation by p^+-doped regions.**

E. ICPDS ON GEOI SUBSTRATES FOR IR PHOTODETECTION

Germanium has been extensively used for IR detection due to its low bandgap and high quantum efficiency under illumination at long wavelengths [20]–[22]. On the other hand, Germanium-on-Insulator (GeOI) substrate offers high carrier mobility and attracts interests for large-scale CMOS application [23], [24]. Here, we have simulated ICPDs based on GeOI substrates for infrared detection by illuminating an ICPD on GeOI with the same dimensions as the SOI device (L_G = 1 μm, T_{si} = 200 nm) with 50 μW/cm^2 intensity at λ = 1550 nm. The carrier recombination rate in Ge is much higher than that in silicon due to the lower bandgap, which degrades the responsivity down to ∼1170 A/W, see Fig. 9(a). Due to stronger carrier recombination, the rise/fall times in the GeOI device are reduced to 12 μs, much lower than that in SOI device (4.1 ms rise time and 48.3 ms fall time), see Fig. 9(b).

F. SENSOR ARRAY OPERATION

A photodetector array, *i.e.*, an image sensor, is a very important device and has many applications. Conventional image sensors are based on CCD and CMOS architectures [25]–[27]. On one hand, the CCD sensor has a high fill factor and high quantum efficiency. However, the photoelectron charge in a CCD sensor is read out by charge transfer in series, which comes with a set of challenges, such as charge loss during transfer, complicated clock signaling, and no random access capability. On the other hand, the CMOS sensor has excellent compatibility with the CMOS fabrication process and random access of each pixel. But, the CMOS sensor has extra transistors in each pixel to facilitate random access. These extra transistors complicate the cell structure and reduce the fill factor and quantum efficiency.

Here, we propose an ICPD photodetector array, which combines the advantages of simple cell structure, high fill factor and random access capability. The ICPD sensor array has a similar layout to a CCD sensor, with the gate lines and active channels forming a crossbar structure requiring no extra transistor, see Fig. 10. The thin Si layer in SOI might reduce the internal quantum efficiency, whereas the external quantum efficiency is high thanks to the internal gain. Unlike a CCD sensor, in the ICPD array, photoelectrons accumulating under the gate are read out by the interface coupling effect instead of charge transfer. Random access is achieved by selecting a certain pixel with both gate and drain signals.

Figure 10(a) shows the simulation results on a simplified ICPD array with two cells (one row by two columns), where cell 1 is illuminated. Cells in the same row share the same back channel. The gate voltage selects column and drain voltage selects row. Thus, the V_{G1} pulse is applied on cell 1 followed by a V_D pulse to selectively read cell 1. Due to interface coupling under V_{G1}, the current in the back channel is determined by the top interface charge in cell 1. If cell 1 is illuminated, a high output current is observed. The readout of cell 2 is achieved by applying V_{G2} and V_D pulses, which outputs relatively low current. Due to crosstalk between cells, some photoelectrons in cell 1 can migrate to cell 2, so the readout of cell 2 shows an apparent photocurrent, dashed line in Fig. 10(a). Inter-cell isolation by p^+-doped regions between adjacent cells can be applied to suppress this crosstalk, solid line in Fig. 10(a).

Since cells in the same row share the same channel, the series resistance from the unselected cells also affects the

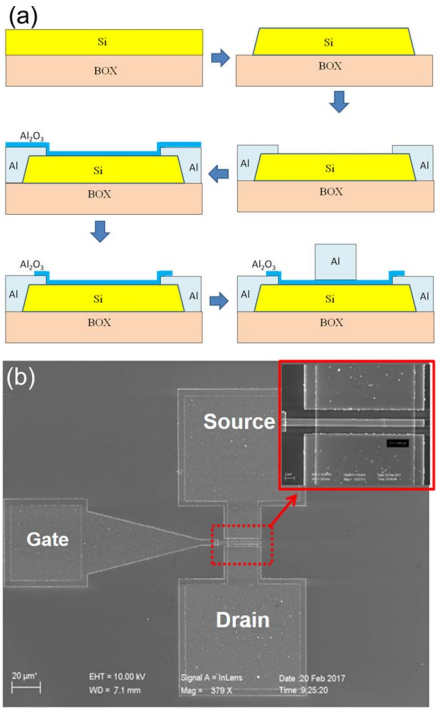

FIGURE 11. (a) Simplified process flow of the device. (b) Top-view SEM image of the fabricated device.

read current, especially in large array. Thus, the applied bias and structure of the array need to be further optimized in large sensor array.

III. EXPERIMENTAL RESULTS

A. DEVICE FABRICATION

Figure 11 (a) shows a simplified process flow to fabricate an ICPD sensor prototype. The fabrication starts with an SOI substrate with 500 nm BOX and $T_{si} = 200$ nm top Si layer. Mesa isolation is formed by photolithography followed by wet etching in 2.5% tetramethyl ammonium hydroxide (TMAH) at 50°C for 2 minutes. Subsequently, photolithography is performed to define the source and drain regions, followed by the deposition of 150nm Al by thermal evaporation. Then, a 30nm Al_2O_3 gate oxide is deposited by atomic layer deposition at 300 °C. Since Al can block light and mitigate sensitivity, a transparent gate such as ITO is expected to further improve the performance.

The structure was finally annealed at 500 °C for 30 minutes in nitrogen. This simplified process requires neither S/D implantation nor high-temperature annealing, and thus has good compatibility with novel materials, such as organic or 2D atomically thin semiconductors.

B. ELECTRICAL CHARACTERIZATION

Electrical characterization is first performed on a device without top gate, schematically shown in Fig. 12(a). This is essentially a conventional backgate-controlled Schottky barrier FET (SB-FET). As reported in [28], after annealing over 450°C, an Al-doped Si layer is formed at the

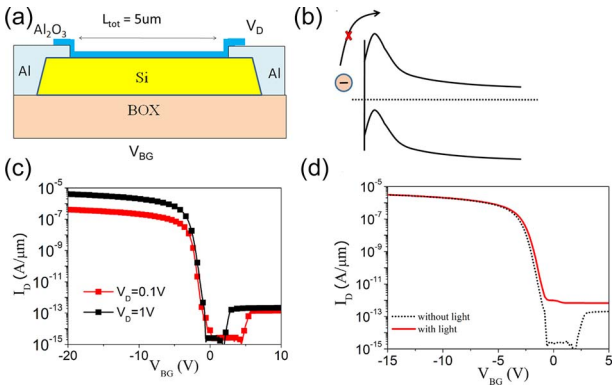

FIGURE 12. (a) Schematic view of the backgate-controlled SB-FET and (b) a schematic explanation of the interfacial layer improving the Schottky barrier height. (c) The $I_D - V_{BG}$ characteristics of the SB-FET with various V_D and (c) the photoresponse with $V_D = -1$ V.

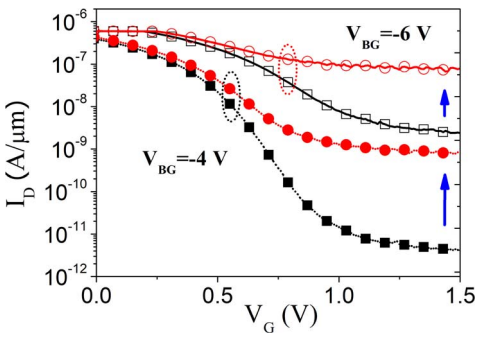

FIGURE 13. (a) $I_D - V_G$ characteristics of the fabricated ICPD at $V_{BG} = -4$ and -6 V, showing improved photoresponse similar to the simulation results.

Al/Si interface. Since the Al is a *p*-type dopant in Si, this interfacial layer can effectively increase the Schottky barrier of Al to the Si conduction band, and improve the hole contact resistance, as shown schematically in Fig. 12(b). Thus, the transfer curves ($I_D - V_{BG}$) of this device indicate *p*-type behavior with a low off current, see Fig. 12(c). Figure 12(d) shows the electrical characterization on this device under 50 $\mu W/cm^2$ illumination at $\lambda = 520$ nm. The device exhibits limited photocurrent and a relatively low photoresponsivity < 0.4 A/W near $V_{BG} = 0$ V, which are normal features for a photo-MOSFET without gain.

The characterization of an ICPD with the Al front gate shows a strong interface coupling effect, where the change of V_G modulates the current at the back interface, see Fig. 13. Illumination at the same intensity and wavelength as on the SB-FET of Fig. 12 now induces significant photocurrent under high V_G. It is worth noting that the V_{BG} can be used to tune the compromise between photoresponsivity and dark current. At $V_G = 1.5$ V, the $V_{BG} = -6$ V curve shows high responsivity up to 3.3×10^4 A/W, albeit with higher dark current compared to the $V_{BG} = -4$ V result. The experimental results in Fig. 13 agree well qualitatively with TCAD simulations shown in Fig. 1(b). The responsivity

is slightly lower than that predicted by TCAD, which is probably due to the overestimation of carrier lifetime.

IV. CONCLUSION

In this paper, we have described a novel photodetector built on an SOI substrate. The device is based on the interface coupling effect and shows extremely high responsivity. The impact of backgate voltage, device dimensions and carrier lifetime on the device performance have been studied in simulation. The operation of a GeOI-based device for IR detection and a sensor array have also be proposed, showing promising performance. A simplified fabrication flow has been developed for a proof-of-concept prototype device structure. Experimental photoelectric measurements show that the responsivity can reach as high as 3.3×10^4 A/W, a record value for a CMOS-compatible SOI photodetector despite an unoptimized fabrication process.

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REFERENCES

[1] R. Carter *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2016, pp. 2.2.1–2.2.4.
[2] S. Narasimha *et al.*, "22nm high-performance SOI technology featuring dual-embedded stressors, epi-plate high-K deep-trench embedded DRAM and self-aligned via 15LM BEOL," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2012, pp. 3.3.1–3.3.4.
[3] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling," *Solid-State Electron.*, vols. 65–66, pp. 226–233, Nov./Dec. 2011.
[4] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed dram using field effect-controlled charge regeneration," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 179–181, Feb. 2012.
[5] C. Sun *et al.*, "A 45nm SOI monolithic photonics chip-to-chip link with bit-statistics-based resonant microring thermal tuning," in *Proc. VLSI Circuits*, 2015, pp. C122–C123.
[6] C. Reimer, M. Nedeljkovic, D. J. M. Stothard, G. Z. Mashanovich, and T. F. Krauss, "Mid-infrared photonic crystal waveguides in SOI," *Opt. Exp.*, vol. 20, no. 28, 2012, Art. no. 29361.
[7] G. Li, K. Maekita, H. Mitsuno, T. Maruyama, and K. Iiyama, "Over 10 GHz lateral silicon photodetector fabricated on silicon-on-insulator substrate by CMOS-compatible process," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, 2015, Art. no. 04DG06.
[8] S. L. Tan, X. Zhao, K. Chen, K. B. Crozier, and Y. Dan, "High-performance silicon nanowire bipolar phototransistors," *Appl. Phys. Lett.*, vol. 109, no. 3, pp. 352–356, 2016.
[9] S. Sahni, X. Luo, J. Liu, Y.-H. Xie, and E. Yablonovitch, "Junction field-effect-transistor-based germanium photodetector on silicon-on-insulator," *Opt. Lett.*, vol. 33, no. 10, pp. 1138–1140, 2008.
[10] J. Wang, M. Yu, G. Lo, D.-L. Kwong, and S. Lee, "Silicon waveguide integrated germanium JFET photodetector with improved speed performance," *IEEE Photon. Technol. Lett.*, vol. 23, no. 12, pp. 765–767, Jun. 15, 2011.
[11] W. Zhang, M. Chan, and P. K. Ko, "Performance of the floating gate/body tied NMOSFET photodetector on SOI substrate," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1375–1384, Jul. 2000.
[12] A. Apsel, E. Culurciello, A. G. Andreou, and K. Aliberti, "Thin film pin photodiodes for optoelectronic silicon on sapphire CMOS," in *Proc. Int. Symp. Circuits Syst. (ISCAS)*, 2003, pp. IV-908–IV-911.
[13] M. A. Marwick and A. G. Andreou, "A UV photodetector with internal gain fabricated in silicon on sapphire CMOS," in *Proc. IEEE Sensors*, 2007, pp. 535–538.
[14] L. Grenouillet *et al.*, "Smart co-integration of light sensitive layers with FDSOI transistors for more than Moore applications," in *Proc. SOI 3D Subthreshold Microelectron. Technol. Unified Conf.*, 2014, pp. 1–2.
[15] L. Kadura *et al.*, "Extending the functionality of FDSOI N- and P-FETs to light sensing," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2016, pp. 32.6.1–32.6.4.
[16] T. Ouisse, S. Cristoloveanu, and G. Borel, "Influence of series resistances and interface coupling on the transconductance of fully-depleted silicon-on-insulator MOSFETs," *Solid-State Electron.*, vol. 35, no. 2, pp. 141–149, 1992.
[17] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983.
[18] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata, and G. Ghibaudo, "Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects," *Solid-State Electron.*, vol. 51, no. 2, pp. 239–244, 2007.
[19] M. Bawedin, S. Cristoloveanu, J. G. Yun, and D. Flandre, "A new memory effect (MSD) in fully depleted SOI MOSFETs," *Solid-State Electron.*, vol. 49, no. 9, pp. 1547–1555, 2005.
[20] L. Chong *et al.*, "High performance silicon waveguide germanium photodetector," *Chin. Phys. B*, vol. 24, no. 3, 2015, Art. no. 038502.
[21] H. Pan *et al.*, "High-speed receiver based on waveguide germanium photodetector wire-bonded to 90nm SOI CMOS amplifier," *Opt. Exp.*, vol. 20, no. 16, pp. 18145–18155, 2012.
[22] S. Siontas, P. Liu, A. Zaslavsky, and D. Pacifici, "Noise performance of high-efficiency germanium quantum dot photodetectors," *Appl. Phys. Lett.*, vol. 109, no. 5, pp. 11513–11534, 2016.
[23] W. H. Chang *et al.*, "Enhancement of mobility in ultra-thin-body GeOI p-channel metal–oxide–semiconductor field effect transistors with Si-passivated back interfaces," *Appl. Phys. Exp.*, vol. 9, no. 9, 2016, Art. no. 091302.
[24] L. Hutin *et al.*, "GeOI pMOSFETs scaled down to 30-nm gate length with record off-state current," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 234–236, Mar. 2010.
[25] B. Büttgen, T. Oggier, M. Lehmann, R. Kaufmann, and F. Lustenberger, "CCD/CMOS lock-in pixel for range imaging: Challenges, limitations and state-of-the-art," in *Proc. Range Imag. Res. Day*, 2005, pp. 21–32.
[26] P. Magnan, "Detection of visible photons in CCD and CMOS: A comparative view," *Nucl. Instrum. Methods Phys. Res.*, vol. 504, nos. 1–3, pp. 199–212, 2003.
[27] D. Litwiller, "CCD vs. CMOS: Facts and fiction," *Photon. Spectra*, vol. 35, no. 1, pp. 154–158, 2001.
[28] H. C. Card, "Aluminum—Silicon Schottky barriers and ohmic contacts in integrated circuits," *IEEE Trans. Electron Devices*, vol. ED-23, no. 6, pp. 538–544, Jun. 1976.

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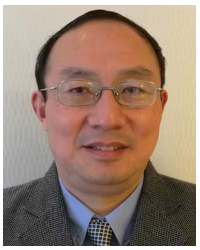

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