Received 18 October 2017; revised 14 December 2017 and 12 January 2018; accepted 17 January 2018. Date of publication 23 January 2018; date of current version 2 February 2018. The review of this paper was arranged by Editor A. G. U. Perera.

Digital Object Identifier 10.1109/JEDS.2018.2796238

Passivation of Poly-Si Thin Film Employing Si Self-Implantation and Its Application to TFTs

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This work was supported in part by the National Natural Science Foundation of China under Grant 61604057, in part by the National Key Technologies Research and Development Program under Grant 2016YFB0401303, in part by the Partner State Key Laboratory on Advanced Displays and Optoelectronics Technologies under Grant ITC-PSKL12EG02, and in part by the Science and Technology Program of Guangdong Province under Grant 2017A010101010.

ABSTRACT Silicon self-implantation technique is applied to passivate the defects in the grain boundaries of the polycrystalline silicon (poly-Si) thin film. The implantation of Si with low dose is a precise technique of introducing Si interstitials in the poly-Si thin film. Thin film transistors fabricated on the resulting poly-Si thin film exhibit improved device characteristics. The increased field-effect mobility is attributed to the incorporation of the injected silicon interstitials in the grain boundaries of the poly-Si thin film and reduction of defect density.

INDEX TERMS Silicon self-implantation, thin-film transistors (TFTs), polycrystalline silicon.

I. INTRODUCTION

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) technology is one of the most promising candidate to realize high resolution active-matrix flat-panel displays, particularly those based on organic light-emitting diodes [1], [2]. The higher mobility of poly-Si TFTs than that of amorphous silicon (a-Si) TFTs allows higher aperture ratio when used as switching and driving transistors in the pixels and offers the possibility of integrating peripheral circuits with the pixel matrix, thus realizing a system on panel. Metal induced crystallization (MIC) [3], [4] and solid phase crystallization (SPC) [5], [6] are two low-cost methods to produce low temperature poly-Si (LTPS) materials. The mobility of conventional SPC and MIC TFTs without plasma passivation is about 15 cm^2/Vs and 30 cm^2/Vs, respectively [3], [5]. Compared to single-crystalline silicon transistors, poly-Si TFTs show poorer performance due to the existence of defective grain boundaries. Much effort has been made to improve the material quality of the poly-Si [7], [8], since it is one of the key factors that determine the performance of a TFT.

Si self-implantation has been studied to enlarge the grain size of poly-Si. High-dose silicon implantation at normal incidence is used to induce nearly full amorphization of the as-deposited poly-Si thin film, with only <110> seeds surviving as a result of the ion-channeling effect. The Si thin film was subsequently recrystallized with annealing process, resulting in large grain size due to low seed density [9]. TFTs based on such Si-implanted and recrystallized poly-Si film demonstrated increased mobility [10]. The drawback of this method is that it complicates the process due to the requirement of both high dosage ion implantation ($\sim 3 \times 10^{15}/cm^2$) to induce amorphization and a recrystallization process. Moreover, random distribution of large grains is not preferred in the view of device uniformity. With the continuously scaling of the size of a TFT, it is reported that the device uniformity degrades dramatically [10]. Recently oxidation-induced injection of Si interstitial has been reported to result in improved performance of TFTs fabricated on poly-Si formed using metal-induced crystallization [11]. The oxidation takes place during the crystallization by replacing the commonly used N_2 with O_2 in the annealing atmosphere.

The implantation of Si is an alternative and more precise technique of introducing Si interstitials. In this paper, the effects of Si implantation, particularly their dose dependence, are studied by monitoring the change in the field-effect mobility of TFTs fabricated on Si-implanted poly-Si thin films. The highest mobility is obtained at a dose of

$\sim 6 \times 10^{14}/cm^2$. These findings are consistent with the mechanism of increased mobility attributed to O_2 annealing crystallization.

II. EXPERIMENTAL

The fabrication process began with 100 mm sized silicon wafers covered with 500 nm thick thermal oxide. Amorphous silicon (a-Si) thin film was deposited as active layer by low-pressure chemical vapor deposition (LPCVD). Poly-Si TFTs based on two different crystallization method, MIC and SPC are studied.

For the MIC TFTs, the thickness of the a-Si thin film is 50 nm. In the MIC process, a thin layer of Ni/Si was sputtered on top of the a-Si layer using a Ni/Si target with a composition ratio of Ni: Si=1:9. The sample was then annealed at 600 °C for 10 hours in N_2. After annealing, the unreacted nickel was removed using a mixture of hot H_2SO_4 and H_2O_2. The poly-Si thin film were then implanted with silicon through 25 nm thick SiO_2 buffer layer at an energy of 15 keV and various doses ranging from 0 to $1\times10^{16}/cm^2$. The SiO_2 buffer layer was deposited by LPCVD at 425 °C for 3 min. After implantation, the post-annealing process for implantation damage repair was carried out at 600 °C in N_2 for 4 hours. The poly-Si layer was then patterned to form the active islands. 50 nm thick SiO_2 was deposited by LPCVD at 425 °C as the gate dielectric. 300 nm thick Al was then deposited by sputtering and patterned as gate electrode. Self-aligned source and drain regions were implanted with boron at dose of $4\times10^{15}/cm^2$ and an energy of 20 keV. 500 nm thick SiO_2 was deposited by LPCVD as the passivation layer before the contact holes were defined. The dopant in the source/drain region was activated during the deposition of passivation layer. 700 nm thick Al-1% Si was sputtered and patterned as source/drain electrodes. Finally, the devices were sintered in forming gas for 30 min at 420 °C.

For the SPC TFTs, the thickness of the active layer was 100 nm. In order to reduce the source/drain series resistance of the SPC TFTs, the active layer is thicker as compared to that of the MIC TFTs. After a-Si deposition, the sample was annealed at 600 °C for 24 hours in N_2. Other steps of device fabrication are the same as the MIC TFTs except for a 12 hours post anneal process after Si implantation for the reduction of the source/drain series resistance. The cross-sectional schematic of the poly-Si TFTs is sketched in Fig. 1.

The electrical properties of the TFTs were measured at room temperature using an HP4156B semiconductor parameter analyzer. The respective channel length (L) and width (W) of the devices are 10 μm and 10 μm.

III. RESULTS AND DISCUSSION

The field effect mobility was extracted using the following equation at low V_{ds}:

$$\mu_{FE} = \frac{LG_m}{WC_{ox}V_{ds}}.$$

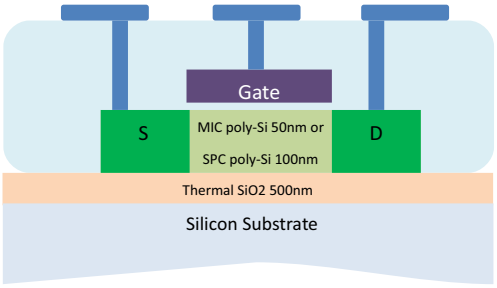

FIGURE 1. Cross-sectional schematic of the poly-Si TFTs with self-aligned structure.

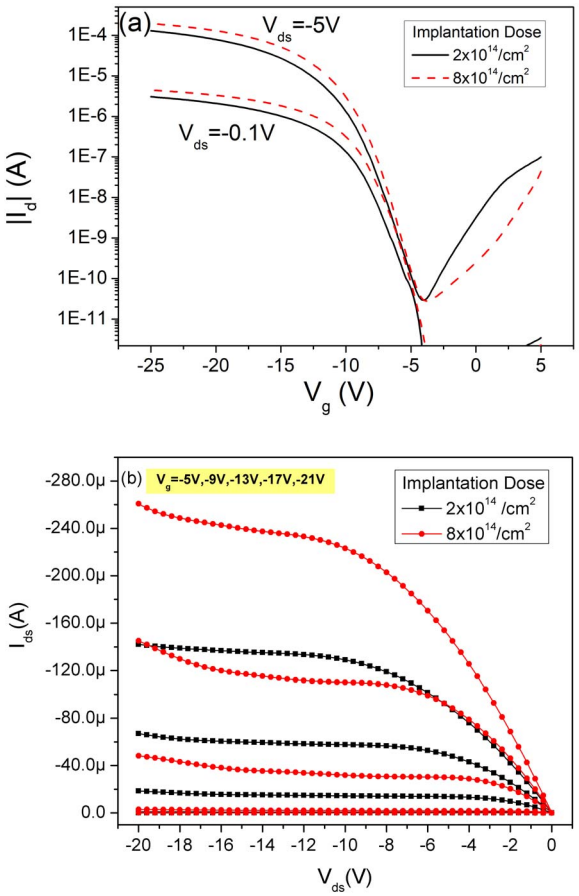

FIGURE 2. (a) Transfer and (b) output characteristics of MIC TFTs with different silicon implantation dose.

The transfer and output characteristics of the MIC TFT with the silicon implantation dose of $2\times10^{14}/cm^2$ and $8 \times 10^{14}/cm^2$ were compared in Fig. 2. The threshold voltage was changed from −7.5V to −6.8V with increase of the implantation dose. The subthreshold slope was also improved from 1.02 V/dec to 0.85V/dec. The comparison of the field-effective mobility of the MIC TFTs with silicon self-implantation dose up to $10^{16}/cm^2$ are shown in Fig. 3. The x-axis is plotted in logarithmic scale. Twenty devices are measured for each sample. For low to medium dose silicon implantation ($\leq 8 \times 10^{14}/cm^2$), a clear trend of

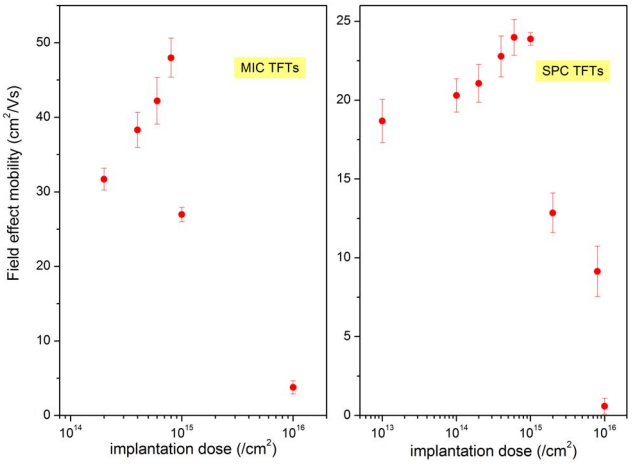

FIGURE 3. The field-effect mobility versus the silicon implantation dose for MIC TFTs and SPC TFTs.

mobility increase is observed with increased Si implantation dose. For devices with implantation dose of $8 \times 10^{14}/\text{cm}^2$, a field-effect mobility of 48.0 cm^2/Vs is obtained, which is 1.5 times of that of the devices without silicon implantation. The enhanced mobility of TFTs is attributed to the silicon interstitials injected in the poly-Si thin film during the silicon implantation process. These interstitials are incorporated in the grain boundaries, which reduce the defect density and enhance the mobility of the poly-Si thin film [12], [13].

Field effective mobility starts to drop for Si implantation dose higher than $1\times10^{15}/\text{cm}^2$. At the dose of $1\times10^{16}/\text{cm}^2$, the mobility drops to 3.8 cm^2/Vs. This indicates amorphization starts to take place for dose higher than $1\times10^{15}/\text{cm}^2$. Unlike previous works [9], [10], we didn't apply long-time post-anneal to recrystallize the amorphized poly-Si film. Therefore, the decrease of mobility with increased Si implantation dose is attributed to lowered crystallinity. The dose of amorphization is also in accordance with the report in [10]. The effect of Si-self implantation in SPC TFTs is also studied. The transfer and output characteristics of SPC TFTs with silicon implantation dose of $1\times10^{13}/\text{cm}^2$ and $6\times10^{14}/\text{cm}^2$ are shown in Fig. 4 (a) and (b), respectively. The distribution of field-effective mobility of the SPC TFTs versus implantation dose is also shown in Fig. 3. Similar trend of mobility improvement is observed. The SPC TFTs with implantation dose of $6\times10^{14}/\text{cm}^2$ demonstrated 28% of mobility improvement when compare with TFTs implanted at the dose of $1\times10^{13}/\text{cm}^2$. The threshold voltage of SPC TFTs were changed from -11.6V to -9.4V with increase of the implantation dose from $1\times10^{13}/\text{cm}^2$ to $6\times10^{14}/\text{cm}^2$. The subthreshold slope was also improved from 1.3V/dec to 1.2V/dec. In the output characteristics in Fig. 4(b), the device with implantation dosage of $6\text{x}10^{14}/\text{cm}^2$ showed higher current due to the increase of the field effect mobility and the decrease of the threshold voltage. The XRD pattern and the Raman

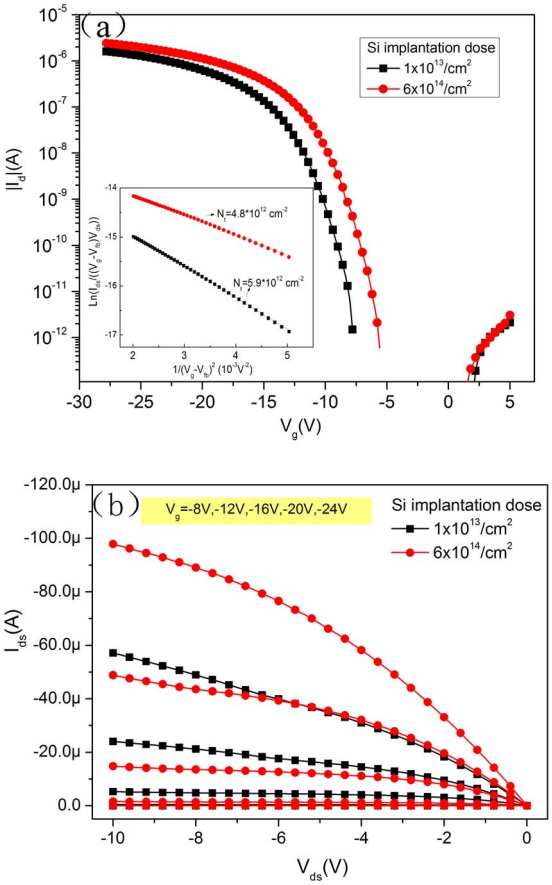

FIGURE 4. (a) Transfer ($V_{ds} = -0.1$V) and (b) output characteristics of SPC TFTs with different silicon implantation dose.

spectra of the SPC poly-Si thin film with silicon implantation dose of $1\times10^{13}/\text{cm}^2$ and $6\times10^{14}/\text{cm}^2$ are compared in Fig. 5 (a) and Fig. 5 (b), respectively. From the comparison, no obvious shift was observed with different implantation dose for both of the XRD pattern and the Raman spectra. The same behaviors were also observed for the MIC thin film. It indicates that the improvement of the mobility is not due to the grain size or the crystallinity but the decrease of the defect density, which is caused by the silicon interstitials injected in the poly-Si thin film. In our experiments, the thickness of the active layer of the SPC TFTs is 100 nm (twice of the thickness of the MIC TFTs). The thicker active layer is to reduce the series resistance of source/drain regions and ensure good crystallinity. As a result, higher dose of Si ions is required to amorphize the poly-Si layer. From Fig. 3, it can be seen that an obvious mobility decrease is also observed at a dose of $2 \times 10^{15}/\text{cm}^2$ for the SPC TFTs. The Raman spectra of the thin film with the silicon implantation dose of $6 \times 10^{14}/\text{cm}^2$ before-implantation, after-implantation, and post-annealing were investigated and shown in Fig. 6. Lower peak observed after-implantation indicated that there is damage inside the thin

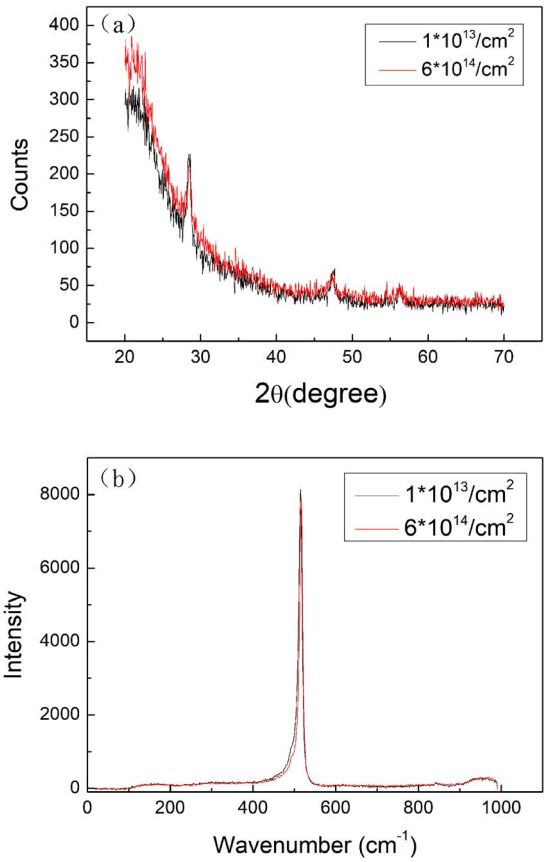

FIGURE 5. **(a) The XRD pattern and (b) the Raman spectra of the SPC poly-Si thin film with different silicon implantation dose.**

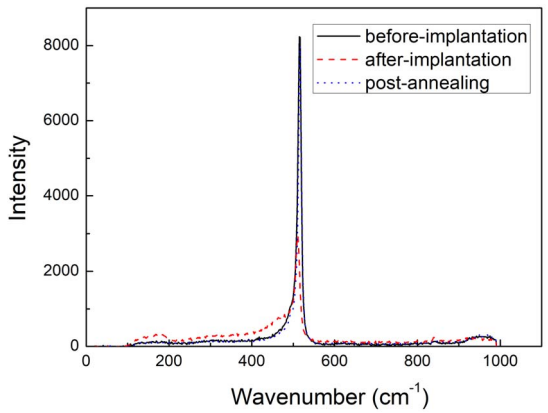

FIGURE 6. **The Raman spectra of the SPC poly-Si thin film before-implantation, after-implantation, and post-annealing.**

film. So post-annealing process was carried out to repair the damage.

The trap state density for the poly-Si TFTs can be obtained using the method proposed by Levinson *et al.* [14] and Proano *et al.* [15]:

$$\frac{I_{ds}}{\left(V_g - V_{fb}\right) V_{ds}} = \frac{WC_{ox}\mu}{L} exp\left(-\frac{q^2 t_{ox}}{C_{ox}\sqrt{\varepsilon_{ox}\varepsilon_{si}}} \cdot \frac{N_t^2}{\left(V_g - V_{fb}\right)^2}\right).$$

where V_{fb} is flat-band voltage, C_{ox} is gate dielectric capacitance per unit area, q is electron charge, t_{ox} is thickness of gate dielectric, $\varepsilon_{\mathrm{ox}}$ is dielectric constant of gate dielectric, $\varepsilon_{\mathrm{si}}$ is dielectric constant of silicon, and N_t is the trap state density. Extracted from the inset of Fig. 4 (a), using this model, the grain boundary trap state density for the SPC TFTs with implantation dose of $1 \times 10^{13}/\mathrm{cm}^2$ and $6 \times 10^{14}/\mathrm{cm}^2$ are $5.9 \times 10^{12}/\mathrm{cm}^2$ and $4.8 \times 10^{12}/\mathrm{cm}^2$, respectively. It indicates that the grain boundary trap state density was reduced by the silicon interstitials injected at the grain boundaries by the self-implantation process. The increased mobility indicates the decrease of potential barrier height in the grain boundaries due to the passivation of defects in the grain boundaries.

IV. CONCLUSION

The effect of Si self-implantation at non-amorphizing dose is studied. It is shown that the MIC and SPC TFTs fabricated on the resulting poly-Si thin film exhibit higher field-effect mobility. The improvement of mobility is attributed to the reduced defect density in the grain boundaries, due to the immigration of silicon self-interstitials to the grain boundaries.

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