Received 12 November 2017; revised 25 December 2017; accepted 10 January 2018. Date of publication 15 January 2018; date of current version 2 February 2018. The review of this paper was arranged by Editor M. Liu.

Digital Object Identifier 10.1109/JEDS.2018.2793902

# Negative Capacitance Enhanced All Spin Logic Devices With an Ultra-Low 1 mV Working Voltage

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This work was supported in part by the National Natural Science Foundation of China under Project 61471015, Project 61504006, and Project 51602013, in part by the Beijing Municipal

Commission of Science and Technology under Grant D15110300320000 and Grant Z161100000216149, in part by the International Mobility Project under Grant B16001, and in part by the National Key Technology Program of China under Grant 2017ZX01032101. Tianqi Gao and Lang Zeng contributed equally to this work.

**ABSTRACT** Since Internet of Things devices should ideally be self-powered, there is great demand for devices with ultra-low operating voltages that can run on energy harvested from a noisy environment. In this paper, a novel all spin logic (ASL) device with voltage controlled magnetic anisotropy (VCMA) effect amplified by negative capacitance (NC) is proposed for the first time. This novel device can operate at a working voltage as low as 1 mV. A three-step pulse scheme is also proposed. Based on simulations of the VCMA effect and the NC effect coupled with the spin modular approach, the feasibility of the proposed ASL device with a 1-mV working voltage and its immunity to variations in device parameters and supply voltage are analyzed.

**INDEX TERMS** Negative capacitance effect, voltage controlled magnetic anisotropy effect, all spin logic devices, ultra-low voltage, Internet of Things.

## I. INTRODUCTION

Because of their unique working environment, it is preferable for Internet of Things (IoT) devices to be self-powered [1]. The voltage collected by an antenna from environmental electromagnetic noise is in the range of  $\mu V \sim mV$  [2]. However, the threshold voltages of traditional CMOS devices are such that these devices cannot be driven by such low voltages because of the existence of 60 mV/dec sub-threshold slope. Among the beyond-CMOS options, all spin logic (ASL) devices based on lateral non-local spin valves with spin transfer torque (STT) effect are regarded as one of the most promising candidates for replacing CMOS devices [3]. The working voltage of an ASL device can be as low as tens of mV, but this is still too high [4] for self-powered IoT application. Thus, neither CMOS nor ASL devices can be directly driven by rectified environmental electromagnetic noise; instead, energy saving and voltage boosting parts are required. All of these additional parts increase the complexity and cost of IoT chips.

In our previous work, it was shown that by incorporating voltage-controlled magnetic anisotropy (VCMA) effect into ASL devices [5]–[7], the energy consumption per switch of such devices can be considerably improved, and the requirement for an external magnetic field accompanying the VCMA effect can be eliminated through the introduction of a negative capacitance (NC) effect [8]–[11]. In this work, we propose that by combination of a ferroelectric (FE) layer and a MgO insulator layer with carefully designed thicknesses, the voltage applied to the CoFeB layer can be amplified by a sufficiently large ratio to enable an ultra-low 1 mV working voltage for ASL devices. The feasibility of our proposed device and its immunity to variations in fabrication and environmental conditions are analyzed by means of physically based simulations.

## **II. DEVICE STRUCTURE**

As shown in Fig. 1a, the VCMA effect is a phenomenon in which the energy barrier between two stable positions



FIGURE 1. (a) Illustration of the voltage controlled magnetic anisotropy (VCMA) effect. (b) Proposed structure for amplifying the VCMA effect by means of negative capacitance (NC) effect. The metal between the ferroelectric (FE) and MgO layers is included to relax possible strain and can be removed. (c) Proposed NC-enhanced ASL device.

of the magnetic moment in a thin CoFeB layer with perpendicular magnetic anisotropy (PMA) can be lowered (enhanced) by applying a positive (negative) voltage to this thin ferromagnetic layer [12], [13]. This effect can be formulated as

$$K_{ani}(V) = K_{ani}(0) - \xi V/t_{ox}, \qquad (1)$$

where  $K_{ani}(0)$  is the anisotropy constant under zero voltage,  $\xi$  is the VCMA coefficient, and  $t_{ox}$  is the thickness of the oxide layer.

The magnetic moment in a thin PMA CoFeB layer becomes more stable in the  $\pm z$  direction under the application of a negative voltage. By contrast, a positive voltage will lower the energy barrier, thus causing the magnetic moment to become volatile in the z direction. A small perturbed inplane magnetic field will easily rotate the magnetic moment of the CoFeB layer to the in-plane direction. This finding has been employed by many researchers in proposals of memory and logic devices [14]–[16]. However, it is cumbersome to include a magnetic field on a chip [17]-[20]. Fortunately, more careful observation of Fig. 1 suggests that the energy barrier will become negative with a further increase in the applied positive voltage. With a negative energy barrier in the z direction, the z direction will become a hard axis instead of an easy axis, and the in-plane direction will be energy-favorable.

According to Eq. (1), to obtain a negative energy barrier, the product  $\xi V$  must be sufficiently large. As noted by K. L. Wang, the greatest obstacle hindering the VCMA effect in practice is an excessively small VCMA coefficient

 $\xi$  [21]. The VCMA coefficient is enhanced greatly to be around 300 fJ/Vm in recent years [22]–[25]. However, it is still far below the required value for stand alone MRAM devices smaller than 32 nm [21]. Consequently, to achieve a negative PMA field in a CoFeB layer, a voltage as high as  $3 \sim 4V$  is required, which is too high for practical use. In our previous work, we proposed the use of a negative capacitance to amplify the applied voltage to a sufficiently high value. The amplification structure is shown in Fig. 1b. The proposal is to add an FE layer and a MgO layer on top of the CoFeB layer, which is experimentally feasible [26]. As a result, a voltage  $V_{MgO}$  can be obtained as follows:

$$V_{MgO} = \frac{V_1 C_{FE} + V_2 C_{MgO}}{C_{FE} + C_{MgO}}.$$
 (2)

Through careful selection of the thicknesses of both the FE layer and the MgO layer such that  $C_{FE} + C_{MgO} \approx 0$ , the voltage applied to the CoFeB layer can be amplified to be much higher than the applied external voltage  $V_1 - V_2$ . The proposed ASL device design is shown in Fig. 1c.

## **III. SIMULATION RESULTS AND DISCUSSION**

For a 1 mV applied voltage to be sufficient to drive the magnetic moment in a CoFeB film from the z direction to the in-plane direction, the key is to amplify the applied voltage with a very large amplification ratio. For an applied voltage V<sub>FE</sub> of 1 mV, the voltage applied to the CoFeB layer after amplification with a 0.3 nm MgO layer and an FE layer of varying thickness was simulated based on Landau-Khalatnikov (LK) theory, and the results are shown in Fig. 2 [27]. Here P(Zr<sub>0.2</sub>Ti<sub>0.8</sub>) FE layer is used as an example material. Hf-based FE layer which is more attractive to the CMOS technology community also can be used as negative capacitance to amplify VCMA effect [28]-[30]. When the thickness of the PZT FE layer is in the range of 11.2~11.4 nm, the voltage applied to the CoFeB film can be higher than 0.15 V, which means that the amplification ratio is larger than 150. With an energy barrier of  $\Delta = 40 k_{\rm B} T$ and nanomagnet dimensions of  $160 \times 160 \times 1$  nm<sup>3</sup> in the ASL device input/output, the PMA field without the VCMA voltage is denoted by  $H_k$ . The voltages required to obtain PMA fields of  $-1 \times$ ,  $-3 \times$  and  $-5 \times H_k$  are plotted as horizontal lines in Fig. 2. It can be observed that an applied voltage of 1 mV can lead to a PMA field of  $-1\times$ ,  $-3\times$ or  $-5 \times H_k$  with a PZT layer thickness of 11.25, 11.35 or 11.45 nm, respectively.

The operation of the proposed NC enhanced ASL device can be divided into three stages, as shown in the inset of Fig. 3. In the preset stage, a 1 mV voltage is applied to terminal  $T_1$  in Fig. 1c, causing the magnetic moment of the CoFeB layer to rotate from the z direction to the in-plane direction. Then, in the pulse stage, a current is injected into terminal  $T_2$  of the ASL device at a 1 mV voltage, causing the magnetic moment to deviate from the in-plane direction. Finally, in the relaxation stage, a negative 1 mV voltage



FIGURE 2. Dependence of the amplified voltage on the thickness of the PZT FE layer when the applied voltage is 1 mV.



**FIGURE 3.** Simulation results for the NC enhanced ASL device. The inset shows the proposed novel three-step pulse scheme.  $V_{STT}$  is the voltage applied for injecting current into ASL device input to induce spin transfer torque at ASL device output. Positive  $V_{STT}$  corresponds to 'COPY' operation while negative  $V_{STT}$  correspond to 'INVERT' operation.

is applied to terminal T<sub>1</sub>, causing the magnetic moment to quickly rotate back to the stable  $\pm z$  position.

The operation of the NC enhanced ASL device was simulated using spin modular approach coupled with the additional VCMA and NC effects [27]. Since the applied voltage in the simulation was 1 mV, the influence of thermal fluctuations could not be neglected.  $V_{STT}$  is the voltage applied in the ASL device input during the pulse stage. The results show that for a positive voltage  $V_{STT}$ , the 'copy' operation is performed, whereas the 'invert' operation is executed with a negative  $V_{STT}$ . The two vertical blue dashed lines in Fig. 3 indicate the separation of the three operation stage. The time period between the two vertical blue dashed lines indicate the pulse stage when STT current is injecting into the ASL device input. Before this time period is the preset stage and after is the relaxation stage. The simulation results



**FIGURE 4.** Confirmation of correct function for NAND, NOR, AND and OR logic operations with all four different input combinations. "11" stands for the two inputs are both logic '1'.

clearly show that the proposed device can work correctly under 1 mV working voltage even with the consideration of thermal noise. The working frequency is about several MHz which is acceptable for IoT applications. In addition, the energy consumption of such one logic operation is 2.6 fJ.

The confirmation of the correct function for NAND, NOR, AND and OR logic operations with all four different input combinations is shown in Fig. 4. In all of there simulations, random thermal fluctuation noise is included. "11" means the two inputs for majority logic gate are both logic '1'. The correctness of the logic functionality is obvious.

As shown in Fig. 2, the amplified voltage is very sensitive to the thickness of the PZT FE layer. However, thickness variations will inevitably arise in the fabrication process. We consider the influence of these variations in Fig. 5a. For a PZT thickness of 11.35 nm, which corresponds to  $-3 \times H_k$ , Fig. 5a shows that a  $\pm 0.1$  nm variation in the PZT FE film thickness will not affect the correct operation of the ASL device. The intent is for the proposed NC enhanced ASL device to be directly driven by environmental electromagnetic noise. However, the amplitude of this electromagnetic noise will typically exhibit large variations, and we consider



**FIGURE 5.** (a) Variations of  $\pm 0.1$  nm in the FE layer thickness will not affect the correct operation of the proposed ASL device. (b) Variations of  $\pm 50\%$  in the supply voltage will not affect the correct operation of the device. (c) Simultaneous variations of  $\pm 0.1$  nm in the FE layer thickness and  $\pm 50\%$  in the supply voltage will not affect the correct operation of the device.

the influence of these variations in Fig. 5b.  $V_{FE}$  is the voltage applied in preset stage and relaxation stage between Terminal T1 and ground. V<sub>pulse</sub> is the voltage applied in pulse stage between Terminal T2 and ground. It can be seen that with 1 mV as the standard working voltage,  $\pm 50\%$  fluctuations in the supply voltage will not affect the correct operation of the ASL device. In Fig. 5c, we present the results of a statistical simulation of variations in both the PZT thickness and the supply voltage. For a PZT thickness of 11.25 nm and a 0.5 V supply voltage, the switching time is too long; therefore, we do not plot the corresponding results in Fig. 5c. The findings prove that our proposed NC enhanced ASL device is immune to  $\pm 0.1$  nm variations in PZT thickness and  $\pm 50\%$  variations in supply voltage. The  $\pm 0.1$  nm variations in PZT thickness is hard to achieve in fabrication process. Such small variation requirement comes from the ultra low 1 mV working voltage since an amplification ratio larger than 100 is demanded.

## **IV. CONCLUSION**

In this work, we proposed an NC enhanced ASL device that can operate under an ultra-low voltage of 1 mV. The feasibility of our proposed device and its immunity to variations in the FE layer thickness and supply voltage were analyzed by means of physically based simulations. Our proposed device represents an advance in the development of self-powered IoT devices driven by environmental electromagnetic noise.

#### REFERENCES

- Z. L. Wang, "Toward self-powered sensor networks," *Nano Today*, vol. 5, no. 6, pp. 512–514, 2010.
- [2] C. M. Nguyen et al., "Wireless sensor nodes for environmental monitoring in Internet of Things," in *Proc. IEEE MTT S Int. Microw. Symp.* (*IMS*), Phoenix, AZ, USA, 2015, pp. 1–4.
- [3] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory," *Nat. Nanotechnol.*, vol. 5, no. 4, pp. 266–270, 2010.
- [4] M.-C. Chen, Y. Kim, K. Yogendra, and K. Roy, "Domino-style spinorbit torque-based spin logic," *IEEE Magn. Lett.*, vol. 6, pp. 1–4, 2015.
- [5] T. Gao et al., "Low power all spin logic device with voltage controlled magnetic anisotropy," in Proc. IEEE Nanotechnol. Mater. Devices Conf. (NMDC), Toulouse, France, 2016, pp. 1–4.
- [6] Y. Zhang et al., "Partial spin absorption induced magnetization switching and its voltage-assisted improvement in an asymmetrical all spin logic device at the mesoscopic scale," Appl. Phys. Lett., vol. 111, no. 5, 2017, Art. no. 052407.
- [7] X. Lin *et al.*, "Gate-driven pure spin current in graphene," *Phys. Rev. Appl.*, vol. 8, no. 3, 2017, Art. no. 034006.
- [8] T. Gao et al., "High speed low power all spin logic devices assisted by negative capacitance amplified voltage controlled magnetic anisotropy effect," in Proc. IEEE Int. Conf. Simulat. Semicond. Processes Devices (SISPAD), Kamakura, Japan, 2017, pp. 305–308.
- [9] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.
- [10] A. Sharma and K. Roy, "Design space exploration of hysteresisfree HfZrOx-based negative capacitance FETs," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1165–1167, Aug. 2017.
- [11] L. Zeng *et al.*, "Novel magnetic tunneling junction memory cell with negative capacitance-amplified voltage-controlled magnetic anisotropy effect," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4919–4927, Dec. 2017.
- [12] T. Nozaki, Y. Shiota, M. Shiraishi, T. Shinjo, and Y. Suzuki, "Voltageinduced perpendicular magnetic anisotropy change in magnetic tunnel junctions," *Appl. Phys. Lett.*, vol. 96, no. 2, 2010, Art. no. 022506.
- [13] P. K. Amiri and K. L. Wang, "Voltage-controlled magnetic anisotropy in spintronic devices," *Spin*, vol. 2, no. 3, 2012, Art. no. 1240002.
- [14] K. L. Wang, H. Lee, and P. K. Amiri, "Magnetoelectric random access memory-based circuit design by using voltage-controlled magnetic anisotropy in magnetic tunnel junctions," *IEEE Trans. Nanotechnol.*, vol. 14, no. 6, pp. 992–997, Nov. 2015.
- [15] Z. Al Azim, A. Sengupta, S. S. Sarwar, and K. Roy, "Spin-torque sensors for energy efficient high-speed long interconnects," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 800–808, Feb. 2016.
- [16] S. Sharmin, A. Jaiswal, and K. Roy, "Modeling and design space exploration for bit-cells based on voltage-assisted switching of magnetic tunnel junctions," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3493–3500, Sep. 2016.
- [17] K. Munira, S. C. Pandey, W. Kula, and G. S. Sandhu, "Voltagecontrolled magnetization switching in MRAMs in conjunction with spin-transfer torque and applied magnetic field," *J. Appl. Phys.*, vol. 120, no. 20, 2016, Art. no. 203902.
- [18] G. Yu *et al.*, "Switching of perpendicular magnetization by spin–orbit torques in the absence of external magnetic fields," *Nat. Nanotechnol.*, vol. 9, no. 7, pp. 548–554, 2014.
- [19] Y.-C. Lau, D. Betto, K. Rode, J. M. D. Coey, and P. Stamenov, "Spin–orbit torque switching without an external field using interlayer exchange coupling," *Nat. Nanotechnol.*, vol. 11, no. 9, pp. 758–762, 2016.
- [20] Z. Zhao, M. Jamali, A. K. Smith, and J.-P. Wang, "Spin hall switching of the magnetization in ta/tbfeco structures with bulk perpendicular anisotropy," *Appl. Phys. Lett.*, vol. 106, no. 13, 2015, Art. no. 132404.
- [21] P. K. Amiri *et al.*, "Electric-field-controlled magnetoelectric ram: Progress, challenges, and scaling," *IEEE Trans. Magn.*, vol. 51, no. 11, pp. 1–7, Nov. 2015.

- [22] T. Nozaki et al., "Large voltage-induced changes in the perpendicular magnetic anisotropy of an MgO-based tunnel junction with an ultrathin fe layer," Phys. Rev. Appl., vol. 5, no. 4, 2016, Art. no. 044006.
- [23] C. Song, B. Cui, F. Li, X. Zhou, and F. Pan, "Recent progress in voltage control of magnetism: Materials, mechanisms, and performance," Progr. Mater. Sci., vol. 87, pp. 33-82, Jun. 2017.
- [24] T. Nozaki et al., "Highly efficient voltage control of spin and enhanced interfacial perpendicular magnetic anisotropy in iridiumdoped Fe/MgO magnetic tunnel junctions," NPG Asia Mater., vol. 9, no. 12, 2017, Art. no. e451.
- [25] S. Peng et al., "Giant interfacial perpendicular magnetic anisotropy in MgO/CoFe/capping layer structures," Appl. Phys. Lett., vol. 110, no. 7, 2017, Art. no. 072403.
- [26] D. Chien et al., "Enhanced voltage-controlled magnetic anisotropy in magnetic tunnel junctions with an MgO/PZT/MgO tunnel barrier," Appl. Phys. Lett., vol. 108, no. 11, 2016, Art. no. 112402.
- [27] A. I. Khan, "Negative capacitance for ultra-low power computing," Dept. EECS, Ph.D. dissertation, Univ. California at Berkeley, Berkeley, CA, USA, 2015.
- [28] M. H. Lee et al., "Ferroelectricity of HfZrO2 in energy landscape with surface potential gain for low-power steep-slope transistors," IEEE J. Electron Devices Soc., vol. 3, no. 4, pp. 377-381, Jul. 2015.
- [29] J. Zhou et al., "Hysteresis reduction in negative capacitance Ge PFETs enabled by modulating ferroelectric properties in HfZrOx," IEEE J. Electron Devices Soc., vol. 6, no. 1, pp. 41-48, Dec. 2018.
- [30] E. Ko, H. Lee, Y. Goh, S. Jeon, and C. Shin, "Sub-60-mV/decade negative capacitance FinFET with sub-10-nm Hafnium-based ferroelectric capacitor," IEEE J. Electron Devices Soc., vol. 5, no. 5, pp. 306-309, Sep. 2017.



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