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Deep Subthreshold TFT Operation and Design Window for Analog Gain Stages

XIANG CHENG[1] (Student Member, IEEE), SUNGSIK LEE[1,2] (Member, IEEE), AND AROKIA NATHAN[1] (Fellow, IEEE)

1 Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K.
2 Department of Electronics Engineering, Pusan National University, Pusan 46241, South Korea

CORRESPONDING AUTHORS: S. LEE and A. NATHAN (e-mail: sungsiklee@pusan.ac.kr; an299@cam.ac.uk)

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ABSTRACT The intrinsic gain (A_i), transconductance efficiency (g_m/I_{DS}) and cut-off frequency (f_T) are analysed for thin film transistors (TFTs) operating in the deep subthreshold region to assess the impact of device variations on the design window for analogue circuits. Results suggest that subthreshold operation could improve the A_i and g_m/I_{DS} at the cost of reduced f_T and increased sensitivity to bias and process variations. Interestingly, a less steep subthreshold slope (SS) could, to some extent, compensate for these shortcomings, which is in contrast to the general thinking of pursuing a steeper SS in TFT fabrication.

INDEX TERMS TFT, analog circuits, subthreshold operation, low power.

I. INTRODUCTION

Recent research has shown that by biasing indium gallium zinc oxide (IGZO) thin-film-transistors (TFTs) in the deep subthreshold region could improve the small signal gain and significantly reduce power consumption [1]. This is specifically useful in a new generation of low power applications including sensor networks, bio-medical sensing, and wearables in general [2], [3].

While subthreshold operation in silicon complementary metal-oxide-semiconductor (CMOS) devices had been intensively researched in 1970s with great success in the watch industry [4]–[9], the same has not been done for TFTs.

Due to the low effective carrier mobility of TFTs (perhaps low-temperature polycrystalline silicon (LTPS) being an exception), TFTs generally work in low current levels [10]–[12]. Although this could limit the speed of the device, TFTs can be naturally suitable for the plethora of low speed, low power applications. Biasing the TFT in subthreshold region could further reduce power consumption to sub-nW levels, which is particularly appealing for battery-less operation. However, as the subthreshold region is generally very narrow, the current levels become more sensitive to bias [13] compared with above threshold as illustrated in Fig. 1. If a TFT has a steep subthreshold slope (SS), the sensitivity of current to bias variations is higher. Circuit design in this region of operation could be challenging, although a steep SS provides a high intrinsic gain. A high intrinsic gain is important figure-of-merit (FoM) for circuit design, and many approaches to achieve this have been introduced in above-threshold operation [14]–[17]. Under subthreshold operation conditions, it is known that a TFT with a Schottky contact source/drain will have a steeper SS compared to the ohmic counterpart [1], [18], [19]. Thus while the Schottky TFT provides higher intrinsic gain, the subthreshold operation, can lead to narrowing of the design window for analogue circuits. The transfer curve and operating regions of a TFT are illustrated in Fig. 1, where deep subthreshold region is marked with specific background colour. The transition region between the exponential subthreshold behaviour and the power-law above-threshold behaviour has been excluded.

In this paper, we analyse the key FoMs for TFTs operating in deep-subthreshold region, and their impact in analogue circuits with the aim of establishing guidelines for the design window based on sensitivity analysis.

II. SUBTHRESHOLD MODEL FOR IGZO TFTS

A. DC MODEL

Similar to the CMOS counterpart, the transfer curve of Schottky TFTs in deep-subthreshold region is linear on a log-scale. Converting the model reported in [1] to a more macroscopic form, the equation for a drain voltage (V_{DS})

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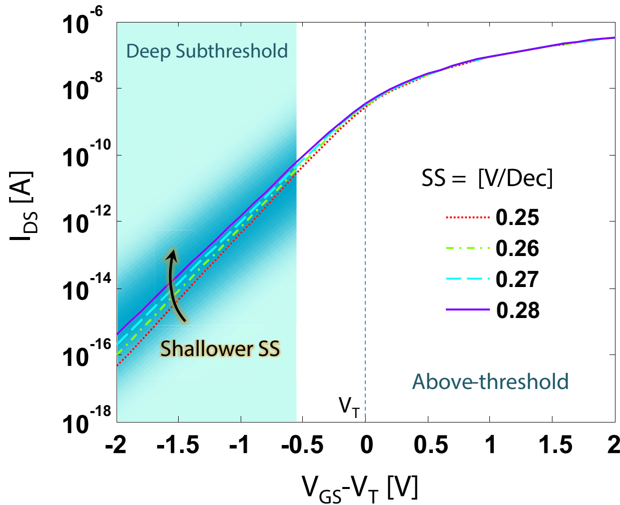

FIGURE 1. I-V curves used in the simulation and analysis of IGZO TFTs, where deep subthreshold region is marked with specific background colour.

larger than the (gate-voltage-independent) saturation voltage (V_{dsat}) is derived as follows [1], [13] with a slight change of notation:

$$I_{DS} = I'_0 \exp\left(\frac{V_{GS} - V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{DS}}{V_A}\right), \tag{1}$$

where I'_0 is the effective subthreshold reference current at V_T (normalized by W) and SS is the subthreshold slope. Here, V_T and V_A are the threshold voltage and the effective Early voltage, respectively. Maintaining consistency with the model reported in [1], we can derive expressions for I'_0 and the Early voltage V_A. The I'_0 can be derived as

$$I'_0 \equiv A_J J_0 \exp\left(\frac{V_T - V_{ref}}{SS/\ln 10}\right), \tag{2}$$

where J_0 is the reference current density at V_{ref}, A_J is the junction area of the Schottky contact at the source and drain. In a Schottky contact TFT, A_J is proportional to the channel width (W) [1].

The Early voltage can be expressed as

$$V_A \equiv n \cdot v_{th} \exp\left(\frac{V_{dsat}}{n v_{th}}\right), \tag{3}$$

where n is the ideality factor of the junction and v_{th} is the thermal voltage.

With the above equations we can easily connect the DC parameters to the important small signal parameters such as g_m and r_o.

B. SMALL SIGNAL MODEL

In previous publications, we reported a specific small signal model for TFTs working in saturation [20], [21]. We showed that the CMOS small signal model cannot describe TFT operation accurately due to the physical connection of the contact resistance and channel capacitance. However, in subthreshold region, the CMOS model could provide enough accuracy. This is due to the small channel capacitance in subthreshold region, which tends to be negligible compared with the TFT's overlap capacitances, C_{gs} and C_{gd}, at the source and drain [20].

The tranconductance and output resistance can be calculated as:

$$g_m = \frac{\ln 10}{SS} I'_0 \exp\left(\frac{V_{GS} - V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{DS}}{V_A}\right) = \frac{\ln 10}{SS} I_{DS}, \tag{4}$$

$$r_o = \frac{V_A}{I_{DS}}, \tag{5}$$

These equations take exactly the same form as the CMOS counterpart.

III. EVALUATION OF GAIN, TRANSCONDUCTANCE AND CUT-OFF FREQUENCY

In this section, we consider the key FoMs with emphasis in the subthreshold region. The model used in assessing the various FoMs is based on [1] with parameter values extracted using the same samples. The W/L of the TFT under test is 50µm/20µm.

A. INTRINSIC GAIN

The intrinsic gain is an important FoM as it reflects the highest achievable single stage gain for an amplifier. The behaviour of gain is shown in Fig. 2, where the simulation is done around the extracted values of the TFT under test, which shows n = 1.7 and SS = 280mV/Dec, respectively. As seen, the intrinsic gain in the subthreshold region is strongly influenced by the subthreshold slope and by the ideality factor n of the Schottky junction. A smaller n, which corresponds to a more ideal Schottky-barrier (SB), would yield a larger intrinsic gain.

The intrinsic gain can be approximated as:

$$A_i = g_m r_o = \frac{V_A \ln 10}{SS}, \tag{6}$$

which suggests that it is inversely proportional to the SS of the TFT. By pushing the SS to its theoretical limit (60mV/Dec, which is the left-most point of every curve in Fig. 2), one could, in principle, exceed a gain of 1000 even with a less ideal Schottky-barrier at the source-semiconductor contact. The expression (6) also suggests that the value of intrinsic gain is rather independent on the bias of the transistor as long as it is operating in subthreshold region. The contribution of the ideality factor n to the intrinsic gain stems from the effective Early voltage (V_A) which in-turn influences the output resistance of the TFT.

B. TRANSCONDUCTANCE EFFICIENCY

Transconductance efficiency (g_m/I_{DS}) is another important FoM, and represents the efficiency of converting the bias current into an equivalent transconductance. For analogue TFT

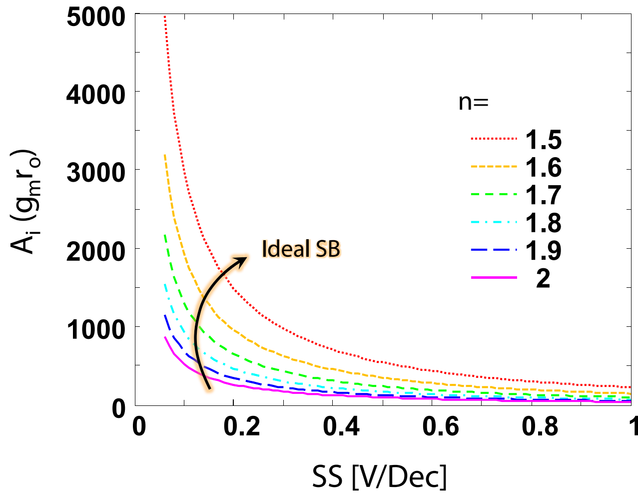

FIGURE 2. Simulation result for the intrinsic gain (A_i) of the Schottky-barrier (SB) IGZO TFT (Schottky TFT); n denotes the ideality factor of the source- semiconductor junction, smaller n corresponds to more ideal SB.

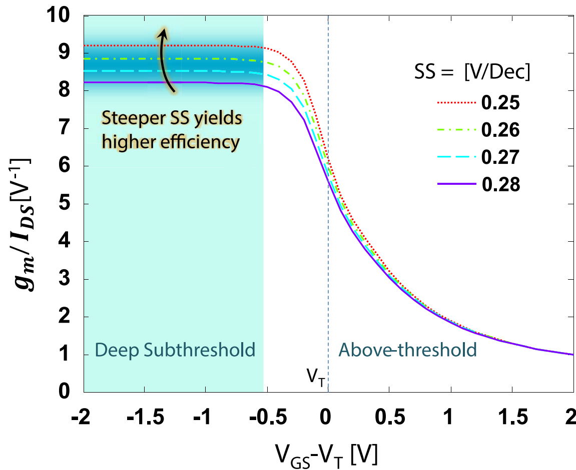

FIGURE 3. g_m/I_{DS} from deep subthreshold to above threshold regions. The value reaches a maximum at deep-subthreshold region and increases with steeper SS.

circuits, as the voltage bias is normally limited by the driving circuitry and the application, reducing the current bias while maintaining a high g_m also means reducing the power consumption without compromising the circuit performance.

As can be seen from Fig. 3, the highest g_m/I_{DS} can be obtained only when operating in deep-subthreshold region, before the transition to above-threshold, and its value remains a constant due to the TFT's exponential nature. The results also suggest that the g_m/I_{DS} value would be larger if the TFT has a steeper subthreshold slope.

The expression of the g_m/I_{DS} value can be estimated as:

$$\frac{g_m}{I_{DS}} = \frac{\ln 10}{SS}, \tag{7}$$

For the above-threshold region, the g_m/I_{DS} value drops, and the expression can be derived using the above-threshold saturation current relations [21], [22],

$$I_{DS} = K\frac{W}{L}\left(V_{GA} - V_T\right)^{\alpha+2}, \tag{8}$$

where α is the power law coefficient in the TFT model ($\alpha = 0$ for the case of MOSFET [21], [22]). Therefore, g_m can be derived as,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{1}{\alpha+2}K\frac{W}{L}\left(V_{GA} - V_T\right)^{\alpha+1}, \tag{9}$$

Dividing Eq. (9) by Eq. (8), we get,

$$\frac{g_m}{I_{DS}} = \frac{2+\alpha}{V_{GS} - V_T}, \tag{10}$$

Therefore, biasing a TFT at a high gate voltage would result in less efficient g_m conversion and thus higher power consumption.

C. CUT-OFF FREQUENCY

The cut-off frequency (f_T) is the frequency where a TFT's short circuit current gain drops to 1 [20]. This value will limit the actual gain bandwidth product of amplifiers. The results shown in Fig. 4 depict a small f_T since the overlap capacitance of the TFT under test is large. The overlap length here is 50µm, which is even bigger than the channel length of the device. Practically, this value can be reduced to a few µm or lower with a self-aligned process, giving increased f_T of one order or more.

Fig. 4 suggests that f_T rolls off quickly in the subthreshold region. As the small signal model for the subthreshold operating TFT takes the same form as that of the MOSFET, the expression of f_T can be derived as [23]–[25],

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} = \frac{I_{DS}\cdot\ln 10}{SS\cdot 2\pi\left(C_{gs} + C_{gd}\right)}, \tag{11}$$

where C_{gs} and C_{gd} are the gate-source capacitance and the gate-drain capacitance, respectively. As the channel capacitance has not been fully formed in subthreshold region, the total capacitance ($C_{gs} + C_{gd}$) is mainly dominated by overlap capacitance in most TFTs. The expression can be approximated as,

$$f_T \approx \frac{I_{DS}\cdot\ln 10}{SS\cdot 2\pi C_{ov}}, \tag{12}$$

where C_{ov} is the total overlap capacitance.

Eq. (12) shows that the value of f_T is proportional to I_{DS}, thus the quick roll off stems from the current roll off in subthreshold region. As I_{DS} and C_{ov} are both proportional to the channel width of the TFT, f_T would be independent of channel width. In addition, by reducing the overlap length, one could further reduce the overlap capacitance (C_{ov}) to increase the frequency response.

The expression also suggests that biasing the TFT with a V_{GS} much lower than V_T would proportionally decrease the cut-off frequency. Therefore, from the standpoint of speed in subthreshold operation, it is desirable to have a less steep subthreshold slope and bias the TFT with a V_{GS} closer to V_T.

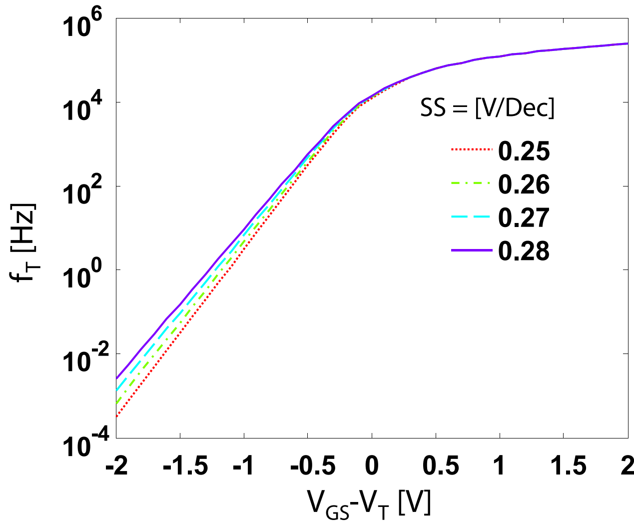

FIGURE 4. Cut-off frequency vs. voltage bias for different SS.

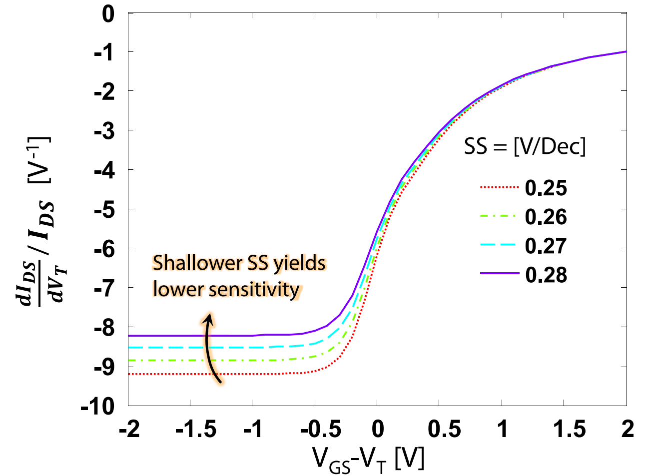

FIGURE 5. Normalized sensitivity to V_T shift for different subthreshold slopes.

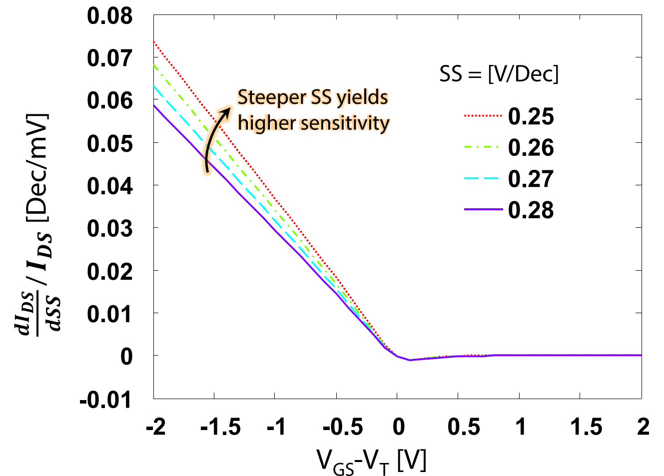

FIGURE 6. Normalized sensitivity to variations in subthreshold slope.

IV. SENSITIVITY TO PARAMETRIC VARIATIONS AND BIAS

A. CURRENT SENSITIVITY TO PARAMETRIC VARIATIONS

Process-induced parametric variations are another important aspect that would affect device performance in a circuit [26]. It is known that the current sensitivity to these variations may be different under different bias conditions [26]. Therefore, it is worth analysing the current sensitivity for different biases in subthreshold region. The main parameters to be considered in the subthreshold model of Eq. (1) are I_0', SS and V_T. The variations in I_0' will create the same percentage variations in current regardless of the bias point. Therefore, here, we consider the contribution of SS and V_T separately.

While analysing the current sensitivity to V_T variations, we kept the same SS value. Therefore, the variation of V_T would lead to a uniform shift of the I-V curve along the voltage axis. The uniform shift yields the sensitivity curve shown in Fig. 5. This curve can also be used for testing the sensitivity to bias voltage since this is also equivalent to a shift of gate bias.

Fig. 5 shows that at deep subthreshold region the normalized current sensitivity to V_T shift is a constant. The sensitivity becomes lower than when approaching and entering the above threshold region. As the V_T shift is equivalent to a bias shift, the sensitivity expression can be the same as that of the g_m/I_{DS} curve (since $g_m = dI_{DS}/dV_{GS}$ is also sensitive to bias) but with an opposite sign.

In deep-subthreshold region:

$$\frac{dI_{DS}}{dV_T}/I_{DS} = -\frac{\ln 10}{SS} \tag{13}$$

and in above-threshold region:

$$\frac{dI_{DS}}{dV_T}/I_{DS} = -\frac{2+\alpha}{V_{GS}-V_T} \tag{14}$$

While analysing the current sensitivity to SS variations, we kept the same V_T. Therefore, the subthreshold current for the different SS would meet at around V_T. This yields the results shown in Fig. 6, where the normalized current sensitivity would drop when the TFT is biased closer to V_T. In the above threshold region. The parameter SS does not contribute to I_{DS}.

The sensitivity is therefore zero. The curve also shows that a steeper SS would increase the current sensitivity.

The expression for the current sensitivity in subthreshold region is shown below:

$$\frac{dI_{DS}}{dSS}/I_{DS} = -\frac{(V_{GS}-V_T)\cdot \ln 10}{SS^2} \tag{15}$$

We see that the sensitivity is inversely proportional to SS^2. Therefore, a steeper SS would yield a high current sensitivity to any variation in SS.

In summary, TFTs with a less steep SS will be more immune to process-induced parametric variations.

B. ACCURACY REQUIREMENT FOR BIASING CIRCUITRY

As an example, we consider a common source amplifier with depletion load as depicted in Fig. 7(b). The load line and bias

conditions are shown in Fig. 7(a). As can be seen, the bias conditions should keep both transistors working in saturation, i.e., at the V_{GS} for the dash line in Fig. 7(a). The dot lines show the highest and lowest usable bias point. Therefore, due to the logarithmic nature of subthreshold operation, the usable bias range ($\Delta V_{bias} \equiv V_{bias_h} - V_{bias_l}$) can be narrow depending on the SS. As this range limits the design window of biasing circuitry, we need to analyze the relation between ΔV_{bias} and SS.

To maintain a high gain, the V_{DS} of both TFTs should follow $V_{DS} > V_{dsat}$. As the value of V_{dsat} for different V_{GS} stays the same in subthreshold region, the highest bias voltage for the circuit should follow:

$$\begin{cases} I_1 = I_0' \exp\left(\frac{V_{bias_h} - V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{dsat}}{V_A}\right) \\ I_1 = I_{load} + \left(\frac{V_{DD} - 2V_{dsat}}{V_A}\right) I_{load} \end{cases} \tag{16}$$

The corresponding current and voltage symbols are depicted in Fig. 7(a). Eq. (5) is used to estimate the output resistance of the load. The lowest bias voltage should follow:

$$\begin{cases} I_2 = I_0' \exp\left(\frac{V_{bias_l} - V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{dsat}}{V_A}\right) \\ I_2 = I_{load} - \left(\frac{V_{DD} - 2V_{dsat}}{V_A}\right) I_2 \end{cases} \tag{17}$$

where Eq. (5) is also applied to estimate the output resistance of the amplifying transistor.

Combining Eq. (16) and Eq. (17), the usable bias voltage range can be calculated as:

$$\begin{aligned} \Delta V_{bias} &= V_{bias_h} - V_{bias_l} \\ &= \frac{2 \cdot SS}{\ln 10} \log\left(1 + \frac{V_{DD} - 2V_{dsat}}{V_A}\right) \end{aligned} \tag{18}$$

As V_A is usually with a value greater than 100V and V_{DD} used in subthreshold operation is only a few volts, the logarithmic term can be further approximated using a 1st order Taylor expansion:

$$\Delta V_{bias} \approx \frac{2 \cdot SS\,(V_{DD} - 2V_{dsat})}{V_A \ln 10} \tag{19}$$

This is illustrated in Fig. 7(c) based on data extracted from an IGZO TFT, where $V_{dsat} = 0.48$V and V_{DD} is set to be 2V. It suggests that the input voltage range is very narrow when designing a common source amplifier stage (i.e., a few mV even when the SS is at 1V/Dec). Therefore, the design of biasing circuitry in TFTs becomes challenging, especially when the process and material variations become large. Here, the bias range is proportional to SS and $V_{DD} - V_{dsat}$. Therefore a less steep SS could improve the design window for biasing while maintaining the value of V_{DD}. Otherwise, a higher V_{DD} needs to be chosen to increase the usable bias range at the cost of increasing the power consumption.

V. CONCLUSION AND DISCUSSION

We examined the intrinsic current gain, transconductance efficiency, and cut-off frequency of the TFT in subthreshold operation, along with the design sensitivity of biasing circuitry on device variations. The results show that high A_i and g_m/I_{DS} can be achieved through subthreshold biasing of TFTs but at the cost of reduced f_T and increased sensitivity to bias- and process-induced parametric variations. We also find that TFTs with less steep subthreshold slope can still benefit from high A_i and g_m/I_{DS}, but with reduced sensitivity to variations and less strict requirement on accuracy of biasing circuitry. The results shown can benefit designers of circuits and systems intended for low power wearables for healthcare monitoring as they intrinsically operate at low frequencies.

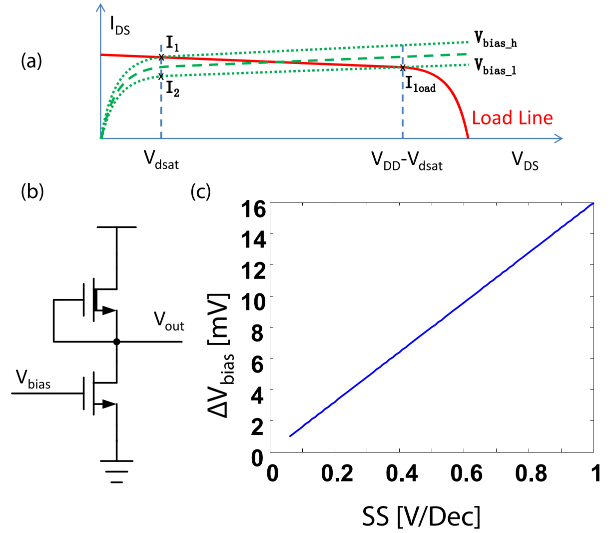

FIGURE 7. Useful bias range for a depletion load common-source amplifier. (a) Conceptual figure of the load line and transfer curve of the amplifier, where the green curve illustrates the correct bias condition and blue curves illustrates the one or the other TFT in non-saturation. (b) Circuit schematic of the amplifier indicating the useful bias range with respect to SS. (c) Useful bias range with respect to SS based on data extracted from IGZO TFT, where V_{DD} = 2V and V_{dsat} = 0.48V.

Comparing the silicon MOSFET with the TFT, the qualitative trend of FoMs under different bias range is similar, while quantitatively the TFT is unique due to its higher resistivity. The major difference lies in the extremely high intrinsic gain, even higher than the MOSFET as reported in [1], and the much lower cut-off frequency. In addition, as the TFT generally has a less steep SS, it might be beneficial in terms of reducing sensitivities to bias and process variations.

Although the analysis presented here has been done according to the extracted parameters of an IGZO TFT, the same can be applied to TFTs from other material families, given that TFTs have a similar structure. The model used here was derived from a Schottky TFT which has a V_{DS} independent saturation voltage, V_{dsat}. This may not be the case in other TFTs and thus should be tested a priory.

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XIANG CHENG received the bachelor's degree in electronic engineering from Shanghai Jiao Tong University in 2013. During the degree, he did his final year project for AMOLED pixel circuit design and simulation under the supervision of Prof. X. Guo. He is currently pursuing the Ph.D. degree with the University of Cambridge under the supervision of Prof. A. Nathan, where he is currently a Research Assistant/Associate with the Department of Engineering. His research focuses on TFT device modeling and TFT-based circuit and system designs.

SUNGSIK LEE received the Ph.D. degree from University College London, London, U.K., in 2013. From 2013 to 2017, he was a Research Associate with the University of Cambridge, Cambridge, U.K. Since 2017, he has been a Professor with the Pusan National University, Pusan, South Korea. His area of expertise is semiconductor devices and physics for futuristic electronics. He has published over 70 articles, including one science paper on the almost-off transistor, with an H-index of 16. He was a recipient of the IEEE EDS Ph.D. Student Fellowship in 2011 and the Best Teaching Prize 2017 from the Korean Society for Engineering Education, South Korea.

AROKIA NATHAN currently holds the Chair of photonic systems and displays with the Department of Engineering, Cambridge University. He was a Post-Doctoral Fellow with LSI Logic Corporation, USA, and ETH Zurich, Switzerland, for several years. He joined the University of Waterloo, ON, Canada, where he held the DALSA/NSERC Industrial Research Chair in sensor technology and, subsequently, the Canada Research Chair in nano-scale flexible circuits. In 2006, he became the Sumitomo Chair of nanotechnology with the London Centre for Nanotechnology, University College London. He has held Visiting Professor appointments with the Physical Electronics Laboratory, ETH Zürich, and the Engineering Department, Cambridge University, U.K. He has published over 500 papers in the field of sensor technology, CAD, and thin-film transistor electronics, and has co-authored four books. He has over 70 patents filed/awarded and has founded/co-founded four spin-off companies. He was a recipient of the Royal Society Wolfson Research Merit Award from University College London. He serves on technical committees and editorial boards in various capacities. He is a Chartered Engineer, U.K., a fellow of the Institution of Engineering and Technology, U.K., and an IEEE/EDS Distinguished Lecturer.