Importance of $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{on}}/I_{\mathrm{off}})$ in Evaluating the Performance of n-Channel Bulk FinFET Devices

YI-CHUEN ENG [1] (Member, IEEE), LUKE HU[1], TZU-FENG CHANG[1], STEVEN HSU[1], CHUN MAO CHIOU[1],
TED WANG[1], CHIH-WEI YANG[1], OSBERT CHENG[1], CHIH-YI WANG[1], C. S. TSENG[1], REN HUANG[1],
PO-HSIEH LIN[1], KUAN-YU LU[2], I-FAN CHANG[1], CHI-JU LEE[1], YEN-LIANG WU[1], AND MIKE CHANG[1]

1 Advanced Technology Development Division, United Microelectronics Corporation, Tainan 744, Taiwan
2 Reliability Technology and Assurance Division, United Microelectronics Corporation, Tainan 744, Taiwan

CORRESPONDING AUTHOR: Y.-C. ENG (e-mail: yi_chuen_eng@umc.com)

ABSTRACT This paper aims to investigate the recently proposed figure of merit, $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{on}}/I_{\mathrm{off}})$, in detail. Experimental results show that $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{on}}/I_{\mathrm{off}})$ represents the index of device immunity to short-channel effects in bulk FinFETs. The value of its numerator, $\Delta V_{\mathrm{DIBLSS}}$, accounts for the drain-induced barrier lowering and subthreshold swing. The value of its denominator, $I_{\mathrm{on}}/I_{\mathrm{off}}$, accounts for the transistor performance in transitioning between on and off states. Small $\Delta V_{\mathrm{DIBLSS}}$ and large $I_{\mathrm{on}}/I_{\mathrm{off}}$ are desirable, representing the improved gate control over the channel potential. We found that both ΔV_{DIBL} and ΔV_{SS} values are more correlated with the drain off-state current, I_{off}, than they are with the drain on-state current, I_{on}. A high-performance FinFET device exhibits $\Delta V_{\mathrm{DIBLSS}}$ of about 100 mV and $I_{\mathrm{on}}/I_{\mathrm{off}}$ of about 1×10^{6}. Thus, $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{on}}/I_{\mathrm{off}})$ in a high-performance FinFET device is expected to be around 1×10^{-4} mV. Using this figure of merit, along with the verification using conventional parameters such as $\Delta V_{\mathrm{DIBLSS}}$ and $I_{\mathrm{on}}/I_{\mathrm{off}}$, the proposed device shows better electrical characteristics than that in our previous work due to the optimized process conditions implemented.

INDEX TERMS $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{on}}/I_{\mathrm{off}})$, bulk FinFETs, drain–induced barrier lowering, short–channel effects, subthreshold swing.

I. INTRODUCTION

Fin field–effect transistors (FinFETs) are regarded as strong candidates for the sub–20 nm regime because of their excellent immunity to short–channel effects (SCEs) [1]–[3]. In the silicon industry, bulk FinFETs are preferred over silicon–on–insulator (SOI) FinFETs for enhanced heat dissipation, similar performance, and less cost [4]–[8]. Also, the number of required masks used for device fabrication heavily discourages the implementation of SOI FinFET technology in low–cost manufacturing of consumer electronics products. Hence, the implementation of bulk FinFET technology is still currently the most practical option even though SOI would provide a much better short–channel performance.

Recently, a new figure of merit (FoM), $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$, has been presented for the purpose of monitoring the performance of n–channel bulk FinFET devices [9]. Logic FoMs, such as drain–induced barrier lowering (DIBL), subthreshold swing (SS), saturation drive current, $I_{\mathrm{d,sat}}$, and source/drain (S/D) subthreshold off–state leakage current, $I_{\mathrm{sd,leak}}$, are merged into a single parameter to represent the overall device performance. Among them, ΔV_{DIBL} is defined as $V_{\mathrm{t,lin}} - V_{\mathrm{t,sat}}$, where $V_{\mathrm{t,lin}}$ is the linear threshold voltage, and $V_{\mathrm{t,sat}}$ is the saturation threshold voltage [10]. ΔV_{SS} is approximately the value of SS [9]. $\Delta V_{\mathrm{DIBLSS}}$ is defined as $\Delta V_{\mathrm{DIBL}} + \Delta V_{\mathrm{SS}}$, representing the gate voltage (V_{g}) domain covered by the combination of DIBL and SS. $I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}}$ represents the transistor performance in transitioning between on and off states. As more analysis regarding this new FoM is done, more interesting facts are found.

In our previous work, we utilized this new FoM, $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$, to characterize and compare the performance of n–channel bulk FinFET devices with and without the lightly–doped drain (LDD) implantation. The main purpose of this paper is to investigate in more detail the fundamental concepts of $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{on}}/I_{\mathrm{off}})$, where
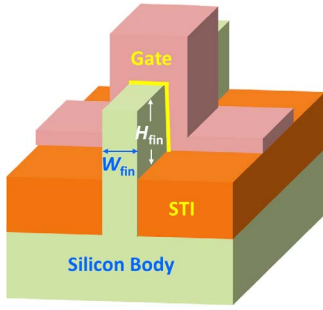
FIGURE 1. Bulk FinFET in this work.

$I_{\text{d,sat}}/I_{\text{sd,leak}}$ is replaced with $I_{\text{on}}/I_{\text{off}}$ for simplicity. It should be noted that by changing the term $I_{\text{sd,leak}}$ into I_{off}, other components of the leakage current such as gate leakage, band–to–band tunneling, and gate–induced drain leakage (GIDL) are also covered [11]. However, since the I_{off} of the proposed device in this work is sufficiently small (7×10^{-13} A) and is dominated by the subthreshold leakage current, these leakage currents can be ignored in our computation of $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$. Such low leakage current is attributed to the FinFET structure and the high–κ metal–gate process [1], [12]. Our findings show that the $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ parameter is a key index for reporting the device immunity to SCEs in bulk FinFETs. In general, this new FoM can be used for reporting the device immunity to SCEs in any metal–oxide–semiconductor (MOS) FETs (MOSFETs)–based devices. Detailed discussion and analysis of $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ are presented.

II. DEVICE FABRICATION

A silicon starting material was used for manufacturing FinFET devices with physical gate lengths between 16 nm and 20 nm. The major processes are described as follows. After p–well implantation (BF: 2.5×10^{19} cm^{-3} – 5×10^{19} cm^{-3}), the fin structure was formed. Fin widths were between 8.2 nm and 9.1 nm, and fin heights were between 40.1 nm and 42.3 nm. Definition of gate length and dry etching were then carried out. LDD implantation was absent in this work. Next, the sacrificial nitride layers were deposited on the silicon surface, followed by lithography and etching processes. The selective epitaxial growth of in–situ phosphorus–doped silicon was performed. The total oxide spacer thicknesses were between 4.2 nm and 4.4 nm. Rapid thermal processing was used for activating implanted dopants. Subsequent processes took place using standard high–κ complementary MOS (CMOS) technology. The gate dielectric thicknesses were between 1.8 nm and 2 nm. A schematic view of the proposed FinFET is shown in Fig. 1. The main structural parameters are shown.
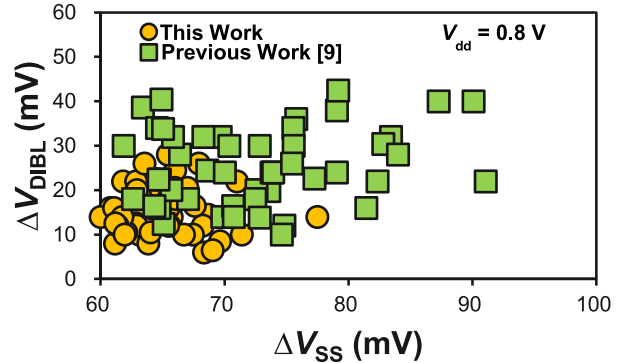
The previous work, presented in [9], is used for comparison with the proposed device in terms of electrical parameters such as $V_{\text{t,sat}}$, ΔV_{DIBL}, ΔV_{SS}, $I_{\text{on}}/I_{\text{off}}$, and $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$. Furthermore, the influence of $V_{\text{t,sat}}$ on
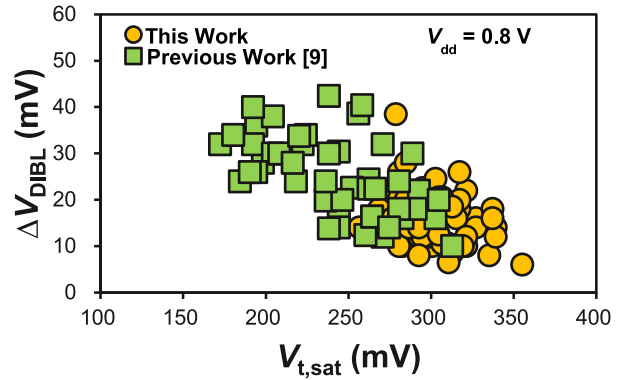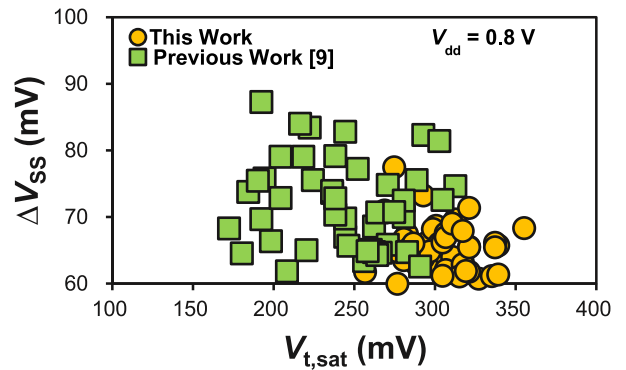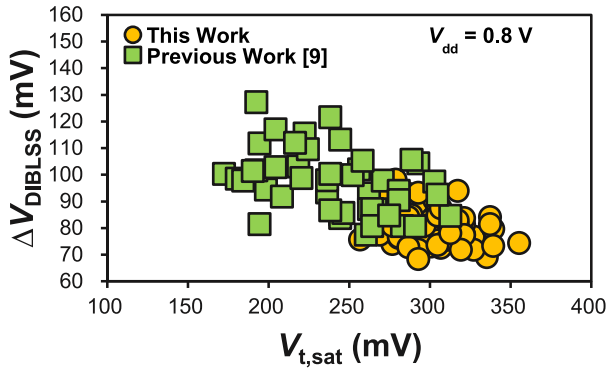

FIGURE 2. The (a) ΔV_{DIBL} and (b) ΔV_{SS} as a function of $V_{\text{t,sat}}$ in n–channel bulk FinFETs without lightly–doped regions. (c) The ΔV_{DIBL} as a function of ΔV_{SS} in n–channel bulk FinFETs without lightly–doped regions. Small $\Delta V_{\text{DIBLSS}}(= \Delta V_{\text{DIBL}} + \Delta V_{\text{SS}})$ is preferred, implying that the suppression of SCEs is observed. In addition, it is noted that the proposed device behaves better than the device from the previous work [9].
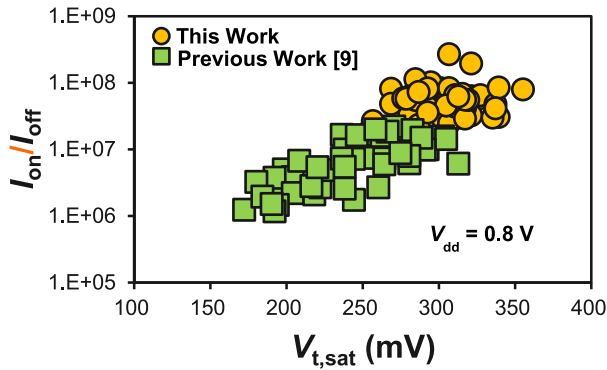
$\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ in bulk FinFETs is investigated under a given $V_{\text{t,sat}}$ range.

III. RESULTS AND DISCUSSION
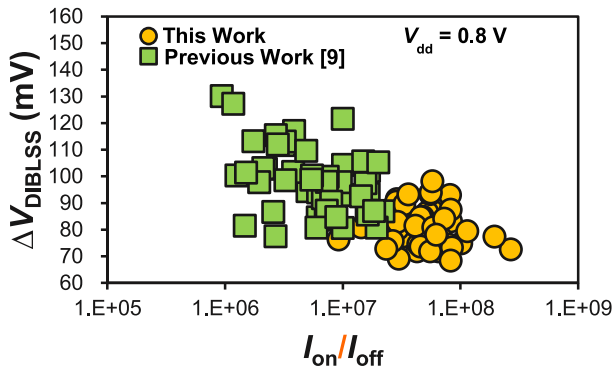
First, we investigate the influence of $V_{\text{t,sat}}$ on the device's ΔV_{DIBL} and ΔV_{SS} characteristics (Fig. 2(a) and Fig. 2(b)). Parameters are defined as follow: $\Delta V_{\text{DIBL}} = \text{DIBL} \times (V_{\text{dd}} - V_{\text{d,low}})$ and $\Delta V_{\text{SS}} \approx \text{SS} \times \Delta I_{\text{d}}$ [9]. Results show that when
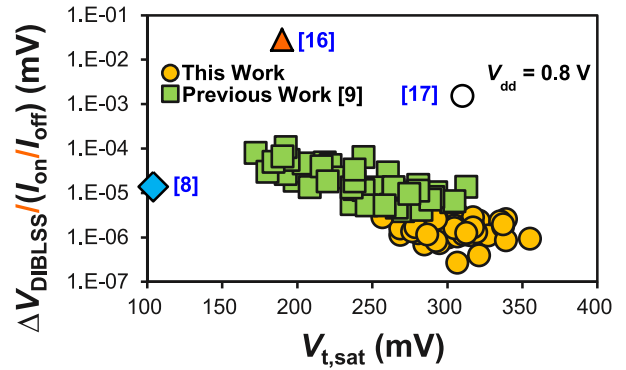
ENG *et al.*: IMPORTANCE OF $\Delta V_{DIBLSS}/(I_{ON}/I_{OFF})$ IN EVALUATING PERFORMANCE OF n–CHANNEL BULK FinFET DEVICES

JOURNAL OF THE
ELECTRON DEVICES SOCIETY

(a)

(b)

(c)

FIGURE 3. The (a) ΔV_{DIBLSS} and (b) I_{on}/I_{off} as a function of $V_{t,sat}$ in n–channel bulk FinFETs without lightly–doped regions. (c) The ΔV_{DIBLSS} as a function of I_{on}/I_{off} in n–channel bulk FinFETs without lightly–doped regions. Smaller value of ΔV_{DIBLSS} results in larger transistor on/off current ratio, which means a low–risk of SCEs in bulk silicon FinFETs.
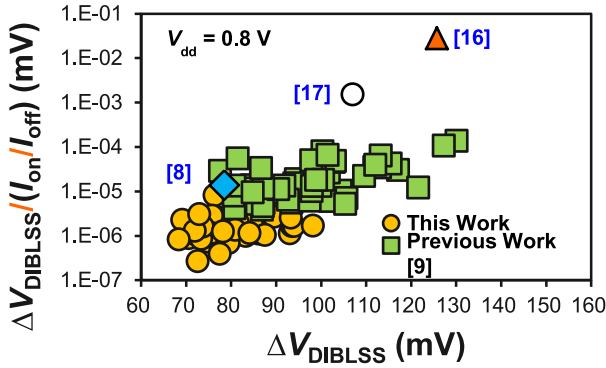

FIGURE 4. The $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ as a function of $V_{t,sat}$ in n–channel bulk FinFETs without lightly–doped regions. The $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ parameter exhibits a strong $V_{t,sat}$ dependence.
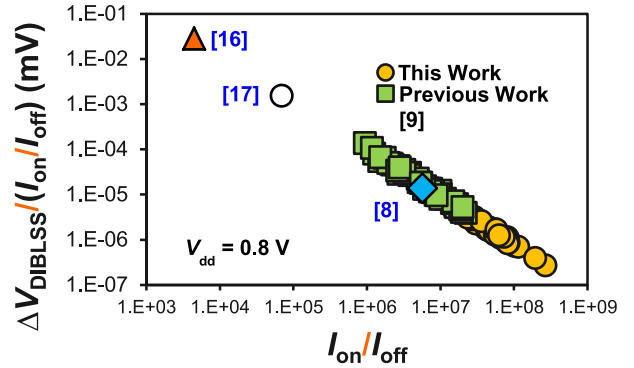
without lightly–doped regions. It is clear that smaller ΔV_{DIBL} corresponds to smaller ΔV_{SS}. ΔV_{DIBL} of 30 mV and ΔV_{SS} of 70 mV are desirable in a nanoscale device. This implies that the on and off states of a nanoscale device are almost completely controlled by the gate. The value of ΔV_{DIBLSS} is the sum of ΔV_{DIBL} and ΔV_{SS}. Smaller value of ΔV_{DIBLSS} in a nanoscale device assures that smaller DIBL and steeper SS values are achieved simultaneously, under which condition, I_{off} is not significantly affected by the DIBL effect and SS [13].

ΔV_{DIBLSS} is affected by the $V_{t,sat}$ due to the contribution of DIBL and SS (Fig. 3(a)). ΔV_{DIBLSS} of 100 mV is used to monitor and compare the characteristics of bulk FinFETs. Hence, the smaller values of ΔV_{DIBL} and ΔV_{SS} are simultaneously obtained. It is also interesting to note that I_{on}/I_{off} increases with increasing $V_{t,sat}$ (Fig. 3(b)). An I_{on}/I_{off} of 1×10^6 indicates that the V_g has much more control over the operation of the MOSFET than the drain voltage, V_d. The relatively flat trend of ΔV_{DIBLSS} (and I_{on}/I_{off}) vs. $V_{t,sat}$ is a result of the reduction of SCEs in this work. According to [4], [9], [10], and [14], when the charge sharing from the S/D to the channel is suppressed, a higher $V_{t,sat}$, which approaches the value of $V_{t,lin}$, can be obtained. Therefore, a negligible trend of ΔV_{DIBLSS} (and I_{on}/I_{off}) vs. $V_{t,sat}$ can be observed. We aim to minimize the value of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ and obtain a relatively flat trend of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ vs. $V_{t,sat}$. Such case indicates better short–channel performance. To further analyze the role of ΔV_{DIBLSS} in bulk silicon FinFETs, the ΔV_{DIBLSS} as a function of I_{on}/I_{off} is shown in Fig. 3(c). As seen in this figure, small ΔV_{DIBLSS} is almost always linked with large I_{on}/I_{off}. This again proves that the improvement of SCEs in bulk silicon FinFETs reduces the sensitivity of I_{off} to the DIBL effect and SS. In other words, a potential barrier between the source and the channel region is not significantly decreased when the V_d is high (0.8 V) [10], [14]. Small DIBL leads to small off–state leakage current. Steep SS results in good on/off switching performance. Hence, the value of ΔV_{DIBLSS} can be used to evaluate the overall performance of n–channel bulk FinFET devices.

the $V_{t,sat}$ is decreased further, both the ΔV_{DIBL} and the ΔV_{SS} become larger. This is attributed to the fact that the SCEs strongly influence the device performance in bulk FinFETs. We also observe that the $V_{t,sat}$ has little impact on the ΔV_{SS} characteristics. Under the same $V_{t,sat}$ condition, the proposed device has smaller values of ΔV_{DIBL} and ΔV_{SS} in comparison with that in the previous work [9] because optimized process conditions were implemented. Fig. 2(c) shows ΔV_{DIBL} as a function of ΔV_{SS} in n–channel bulk FinFETs

FIGURE 5. The $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ as a function of ΔV_{DIBLSS} in n–channel bulk FinFETs without lightly–doped regions. It is observed that when ΔV_{DIBLSS} is smaller than 100 mV, the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ parameter value becomes significant smaller than 1×10^{-4} mV. Hence, the device performance is quantified by $\Delta V_{DIBLSS}/(I_{on}/I_{off})$. Smaller $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ means stronger immunity to SCEs.

FIGURE 6. The $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ as a function of I_{on}/I_{off} in n–channel bulk FinFETs without lightly–doped regions. An I_{on}/I_{off} of larger than 1 $\times 10^6$ is achieved, eventually resulting in the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ parameter value smaller than 1×10^{-4} mV. Smaller $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ also means better switching performance.

The measured values of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ for n–channel bulk FinFETs without lightly–doped regions as a function of $V_{t,sat}$ are shown in Fig. 4. One important point to note is that $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ exhibits a strong $V_{t,sat}$ dependence. $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ decreases as $V_{t,sat}$ increases. This is due to the fact that SCEs occur in bulk FinFETs. This proves the usefulness of the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ parameter in analyzing SCEs for bulk FinFETs. Another important point is that the proposed device has smaller $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ than that in our previous work. As explained in Fig. 2, smaller ΔV_{DIBLSS} and larger I_{on}/I_{off} result in better device performance. Next, the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ as a function of ΔV_{DIBLSS} is investigated. It is demonstrated in Fig. 5 that the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ decreases as the ΔV_{DIBLSS} decreases. At the same time, the $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ decreases as the I_{on}/I_{off} increases, as

shown in Fig. 6. When the value of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ is around 1×10^{-4} mV, the values of ΔV_{DIBLSS} and I_{on}/I_{off} are 100 mV and 1×10^6, respectively. This behavior is due to the interrelated effects of ΔV_{DIBL} and ΔV_{SS} in a nanoscale device. Smaller ΔV_{DIBLSS}, which means reduced electric field in the drain region of a MOS transistor, indicates better on/off characteristics. Thus, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ becomes a key device parameter in evaluating the performance of n–channel bulk FinFET devices.

Some state–of–the–art devices in [8], [16], and [17] are used for comparison with the proposed device. These are shown in Fig. 4–6. Although it is difficult to compare apples to apples due to the differences in fabrication conditions, we observe a consistent trend: devices with reduced DIBL and SS eventually result in smaller $\Delta V_{DIBLSS}/(I_{on}/I_{off})$.
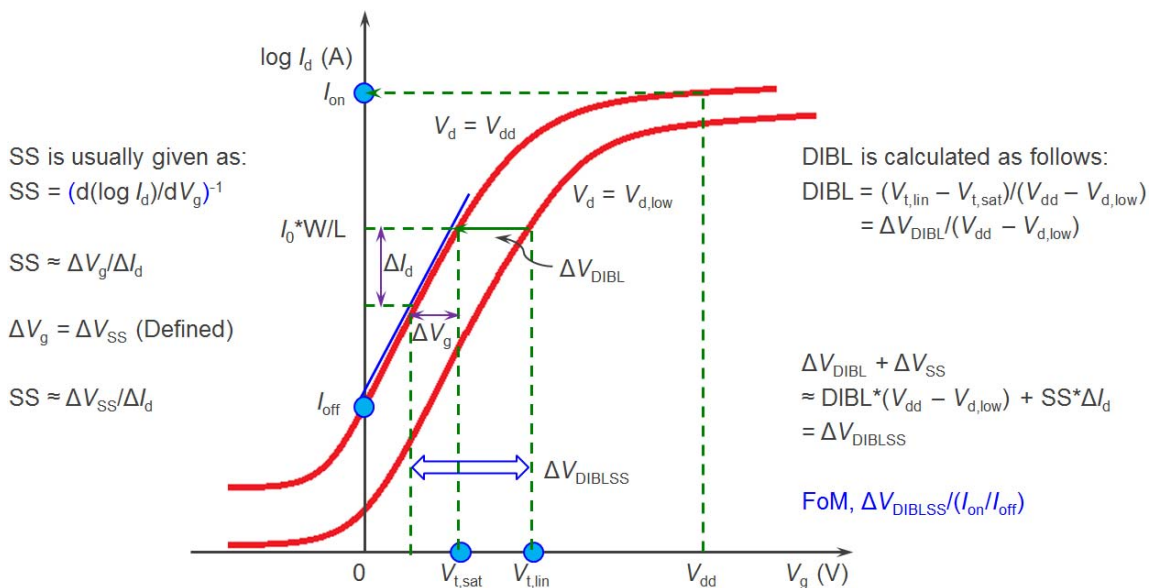
FIGURE 7. A physical explanation of $\Delta V_{DIBLSS}/(I_{on}/I_{off})$. Logic FoMs, such as DIBL, SS, I_{on}, I_{off}, are merged into a single parameter to analyze the overall device performance. Smaller $\Delta V_{DIBLSS}/(I_{on}/I_{off})$ is desirable implying a superior immunity to SCEs. I_0 is the I_d used for defining the V_t [15].

ENG *et al.*: IMPORTANCE OF $\Delta V_{\text{DIBLSS}}/(I_{\text{ON}}/I_{\text{OFF}})$ IN EVALUATING PERFORMANCE OF n-CHANNEL BULK FinFET DEVICES

JOURNAL OF THE
ELECTRON DEVICES SOCIETY

The physical meaning of $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ is summarized by redrawing the figure in [9] (Fig. 7). $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ contains information on the important performance parameters: The DIBL effect and SS in the x–axis of the I_d–V_g curve and the transistor on/off current ratio in the y–axis of the I_d–V_g curve. ΔV_{DIBLSS} refers to the V_g domain covered by the combination of DIBL and SS as depicted by the graph in Fig. 7. $I_{\text{on}}/I_{\text{off}}$ refers to the on/off transition performance. Small ΔV_{DIBL} results in small leakage current, increasing the separation between I_{off} and I_{on}. Steep SS exhibits fast on/off transition performance, which also increases $I_{\text{on}}/I_{\text{off}}$. Thus, ΔV_{DIBL} and ΔV_{SS} are interrelated. As a result, small $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ is a good indication that the SCEs are under control.

In general, the $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ parameter can also be utilized for special technologies such as of III–V MOSFETs and tunnel FETs (TFETs) [18]–[20]. These topics are beyond the scope of this paper. However, these technologies are nevertheless short–channel devices, so the $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ parameter can still be useful. Note that in a high–performance device, the $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ parameter should still always be smaller than 1×10^{-4} mV because it means that small ΔV_{DIBLSS} and large $I_{\text{on}}/I_{\text{off}}$ are being simultaneously obtained.

IV. CONCLUSION

We have demonstrated experimentally that the $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$ parameter can be used to evaluate the performance of n–channel bulk FinFET devices. The numerator corresponds to DIBL and SS, and the denominator indicates how well a nanoscale device performs under switching operation. Small ΔV_{DIBLSS} and large $I_{\text{on}}/I_{\text{off}}$ are desirable for a high–performance FinFET device. Thus, the smaller the value of $\Delta V_{\text{DIBLSS}}/(I_{\text{on}}/I_{\text{off}})$, the better the performance of a nanoscale device. Furthermore, for a given $V_{\text{t,sat}}$, the proposed device has better electrical characteristics compared to our previous work, including smaller ΔV_{DIBLSS} (<100 mV) and larger $I_{\text{on}}/I_{\text{off}}$ (>1 $\times 10^6$).

REFERENCES

[1] X. Huang *et al.*, "Sub 50-nm FinFET: PMOS," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 1999, pp. 67–70, doi: 10.1109/IEDM.1999.823848.

[2] D. Hisamoto *et al.*, "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000, doi: 10.1109/16.887014.

[3] S. Natarajan *et al.*, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm² SRAM cell size," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2014, pp. 71–73, doi: 10.1109/IEDM.2014.7046976.

[4] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Amsterdam, The Netherlands: Kluwer Acad., 1991.

[5] D. A. Dallmann and K. Shenai, "Scaling constraints imposed by self-heating in submicron SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 489–496, Mar. 1995, doi: 10.1109/16.368045.

[6] P. Su, K. Goto, T. Sugii, and C. Hu, "Self-heating enhanced impact ionization in SOI MOSFETs," in *Proc. IEEE Int. SOI Conf.*, Durango, CO, USA, Oct. 2001, pp. 31–32, doi: 10.1109/SOIC.2001.957970.

[7] D. Jang *et al.*, "Self-heating on bulk FinFET from 14nm down to 7nm node," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2015, pp. 289–292, doi: 10.1109/IEDM.2015.7409678.

[8] A. B. Sachid, M.-C. Chen, and C. Hu, "Bulk FinFET with low-κ spacers for continued scaling," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1861–1864, Apr. 2017, doi: 10.1109/TED.2017.2664798.

[9] Y.-C. Eng *et al.*, "A new figure of merit, $\Delta V_{\text{DIBLSS}}/(I_{\text{d,sat}}/I_{\text{sd,leak}})$, to characterize short-channel performance of a bulk-Si n-Channel FinFET device," *IEEE J. Electron Devices Soc.*, vol. 5, no. 1, pp. 18–22, Jan. 2017, doi: 10.1109/JEDS.2016.2626464.

[10] S. M. Sze, *Semiconductor Devices, Physics and Technology*, 2nd ed. New York, NY, USA: Wiley, 2001.

[11] (2007). *International Technology Roadmap for Semiconductors*. [Online]. Available: www.itrs.net

[12] R. Chau, S. Datta, M. Doczy, J. Kavalieros, and M. Metz, "Gate dielectric scaling for high-performance CMOS: From SiO₂ to High-K," in *Proc. Extended Abstracts Int. Workshop Gate Insulator*, Toyko, Japan, Nov. 2003, pp. 124–126, doi: 10.1109/IWGI.2003.159198.

[13] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors," *Nature*, vol. 479, no. 11, pp. 310–316, Nov. 2011, doi: 10.1038/nature10676.

[14] D. A. Neamen, *An Introduction to Semiconductor Devices*. New York, NY, USA: McGraw-Hill, 2005.

[15] H.-G. Lee, S.-Y. Oh, and G. Fuller, "A simple and accurate method to measure the threshold voltage of an enhancement-mode MOSFET," *IEEE Trans. Electron Devices*, vol. ED-29, no. 2, pp. 346–348, Feb. 1982, doi: 10.1109/T-ED.1982.20707.

[16] G. Tsutsui *et al.*, "Technology viable DC performance elements for Si/SiGe channel CMOS FinFTT," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 17.4.1–17.4.4, doi: 10.1109/IEDM.2016.7838439.

[17] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *VLSI Symp. Tech. Dig.*, Kyoto, Japan, Jun. 2017, pp. T230–T231, doi: 10.23919/VLSIT.2017.7998183.

[18] J. A. Del Alamo *et al.*, "Nanometer-scale III-V MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 205–214, Sep. 2016, doi: 10.1109/JEDS.2016.2571666.

[19] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014, doi: 10.1109/JEDS.2014.2326622.

[20] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88–95, May 2015, doi: 10.1109/JEDS.2015.2390591.

YI-CHUEN ENG (M'16) received the B.S. and Ph.D. degrees in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2005 and 2012, respectively. In 2012, he joined United Microelectronics Corporation, Tainan, Taiwan, where he has been engaged in the field of semiconductor device physics, simulation, and reliability of nonclassical nano-MOSFET architectures.

LUKE HU was born in Tainan, Taiwan, in 1989. He received the B.Eng. and M.Eng. degrees in electrical engineering from the University of Toronto, ON, Canada, in 2011 and 2013, respectively, specializing in photonics and semiconductor physics. He is currently with the Research and Development Division, United Microelectronics Corporation, Tainan, where he has been engaged in the development and qualification of the fabrication, device physics, simulation, and reliability of 3-D IC processes.

TZU-FENG CHANG received the M.S. degree in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2010. From 2011 to 2014, he was with the Department of Technology Development and Product Engineer in Rexchip (Micron), Taichung, Taiwan. He is currently with the Research and Development Division, United Microelectronics Corporation, Tainan, Taiwan. His research interests include semiconductor device physics and SRAM cell operation.

OSBERT CHENG received the M.S. degree from National Tsing Hua University, Hsinchu, Taiwan and the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu. As the Associate Vice President of the Advanced Technology Development Division, United Microelectronics Corporation, Hsinchu, his main focus is on the device development in the Research and Development Team. He has been involved in defining the technology for foundry application for over seven technology nodes. He also leads the SRAM, mixed-signal, reliability, and TCAD in the Research and Development Team.

STEVEN HSU received the M.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan. He was with United Microelectronics Corporation (UMC), Hsinchu, Taiwan, for over 17 years, where he has had experience with semiconductor fabrication from the 0.18 um architecture all the way to the 14 nm architecture. He is currently the Associate Vice President with the Advanced Technology Development Division, UMC, where he is in charge of the 14 nm process and beyond.

CHIH-YI WANG received the Ph.D. degree in physics from National Taiwan University, Taipei, Taiwan, in 2015. In 2016, he joined United Microelectronics Corporation, Tainan, Taiwan, where he has been engaged in the field of semiconductor device physics and new process improvement.

CHUN MAO CHIOU was born in Chiayi, Taiwan. He received the B.S. and Ph.D. degrees in materials science and engineering from National Cheng Kung University, Tainan, Taiwan. In 2003, he joined United Microelectronics Corporation, Hsinchu, Taiwan, where he is currently the Director of the Advanced Technology Development Division. He led the 14 nm FinFET platform development in the Research and Development Team.

C. S. TSENG received the B.S. degree in electrical engineering from Feng Chia University, Taichung, Taiwan. In 1999, he joined United Microelectronics Corporation, Hsinchu, Taiwan. As a Technical Department Manager of the Advanced Technology Development Division, he is devoted to the 14-nm FinFET process development.

TED WANG received the M.S. degree in chemical engineering from Tunghai University, Taichung, Taiwan, in 2001. In 2001, he joined United Microelectronics Corporation, Hsinchu, Taiwan, where he is the Deputy Director of the Advanced Technology Development Division. His main focus is on the 14 nm FinFET process research and development with the Research and Development Team.

REN HUANG received the M.S. degree from the Department of Materials Science, National Sun Yat-sen University, Kaohsiung, Taiwan, in 1997. In 2000, he joined United Microelectronics Corporation, Hsinchu, Taiwan, where he was responsible for the process development of integration. He is currently a Manager focusing on FinFET process development.

CHIH-WEI YANG was born in Kaohsiung, Taiwan. He received the B.S. and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan. In 2003, he joined United Microelectronics Corporation, Hsinchu, Taiwan, where he was responsible for the process development of high-κ and metal gate integration as well as reliability characterization for 28 nm process. He is currently a Manager focusing on FinFET process development.

PO-HSIEH LIN received the B.S. and Ph.D. degrees in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2008 and 2015, respectively. He joined United Microelectronics Corporation, Tainan, Taiwan, in 2015. His research interests include semiconductor device physics and memory technologies for non-classical MOSFET architectures.

ENG *et al.*: IMPORTANCE OF $\Delta V_{DIBLSS}/(I_{ON}/I_{OFF})$ IN EVALUATING PERFORMANCE OF n-CHANNEL BULK FinFET DEVICES

JOURNAL OF THE
ELECTRON DEVICES SOCIETY

KUAN-YU LU was born in Nantou, Taiwan, in 1987. He received the M.S. degree in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2011. He is currently with the Department of Reliability Technology and Assurance Division, United Microelectronics Corporation, Tainan, Taiwan, where he has been engaged in the field of semiconductor device physics and electrostatic discharge protection design in CMOS integrated circuits.

YEN-LIANG WU received the M.S. degree in chemical engineering from National Taiwan University, Taipei, Taiwan. He has been with United Microelectronics Corporation since 2011, and joined 14-nm FinFET process development team since 2013.

I-FAN CHANG received the M.S. degree in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2014. In 2014, she joined United Microelectronics Corporation, Tainan, Taiwan, being engaged in 14-nm FinFET process research and development.

CHI-JU LEE received the M.S. degree in chemical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2006. From 2006 to 2012, she was with UMC, TSMC, and nVIDIA and took charge of the projects ranging from 0.11 um to 28 nm HKMG architecture. She returned to UMC in 2012. As a Technical Department Manager of the Advanced Technology Development Division, she is devoted to the 14-nm FinFET process research and development.

MIKE CHANG received the M.S. degree in electronic engineering from Chang Gung University, Taoyuan, Taiwan, in 2008. He joined United Microelectronics Corporation, Tainan, Taiwan, in 2011, being engaged in 14-nm FinFET process research and development.