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High-Performance Normally Off p-GaN Gate HEMT With Composite AlN/$Al_{0.17}Ga_{0.83}N$/$Al_{0.3}Ga_{0.7}N$ Barrier Layers Design

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ABSTRACT In this paper, a novel normally off p-gallium nitride (GaN) gate high electron-mobility transistor (HEMT) with composite AlN/$Al_{0.17}Ga_{0.83}N$/$Al_{0.3}Ga_{0.7}N$ barrier layers is proposed. Compared to the standard (STD) p-GaN/AlGaN/GaN HEMT structure, the composite barriers (CB) with AlN etch-stop layer can effectively improve the uniformity of the device threshold voltage (V_{TH}) and reduce the leakage current. The CB p-GaN gate HEMT achieved a V_{TH} of 1.7 $\pm$ 0.06 V; this value was 2.1 $\pm$ 0.2 V for STD HEMT. In addition, the off-state drain leakage current was suppressed one order of magnitude by adopting a composite barrier design.

INDEX TERMS Gallium nitride (GaN), high electron mobility transistor (HEMT), normally-off, pulse measurement.

I. INTRODUCTION

Gallium nitride (GaN)-based high electron-mobility transistors (HEMTs) are promising for high switching speed and high-power semiconductor device applications because of their high electric field strength, high mobility, and good thermal stability [1]. The channel modulation mechanism of traditional AlGaN/GaN HEMTs is inherently normally-on because a high-density two-dimensional electron gas (2DEG) is formed by the polarization-induced charges in the AlGaN/GaN interface. Therefore, normally-off behavior of AlGaN/GaN HEMTs with a sufficiently large and stable V_{TH} is highly desirable owing to single voltage supply consideration. Thus, several researches have been proposed to realize the normally-off operation characteristics of the AlGaN/GaN HEMTs such as ultra-thin barrier (UTB) [2], gate-recessed structures [3], [4], the fluorine treatment [5], [6]. Recently, GaN HEMTs with a p-GaN gate stack (p-GaN gate HEMTs) have been demonstrated commercially in a MHz-switching power device, in which a p-GaN layer on top of an AlGaN barrier depletes 2DEG carriers in the channel [7]–[10]. The two major challenges of p-GaN gate HEMTs are the etching depth uniformity of the nongated active region and the plasma-induced damage during the p-GaN removal process. In this study, we overcame the drawbacks of the conventional p-GaN removal process by developing a new transistor barrier structure comprising composite 1-nm AlN/12-nm $Al_{0.17}Ga_{0.83}N$/1-nm $Al_{0.3}Ga_{0.7}N$ on top of the GaN channel [11]. With a BCl_3+ CF_4 gas mixture highly selective dry-etching process that stops at the AlN layer, the 60-nm p-GaN layer of the nongated area can be removed. The selectivity can be attributed to the nonvolatility of aluminum fluoride (AlF_3) [12], which generates a wide process window with a wide etching control tolerance. Moreover, the AlN layer beneath the p-GaN layer achieves a high energy barrier layer to suppress the leakage current induced by thermionic emission; the gate

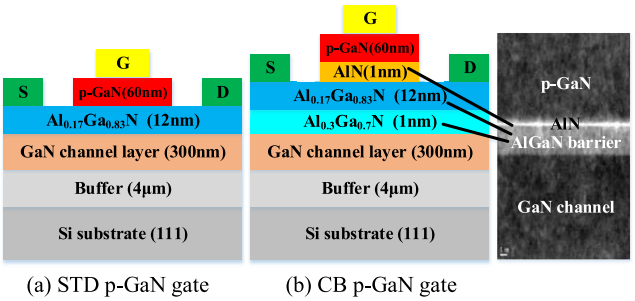

FIGURE 1. Cross-sectional structure of the p-GaN gate HEMT with (a) standard barrier and (b) composite barrier layers design and TEM photography.

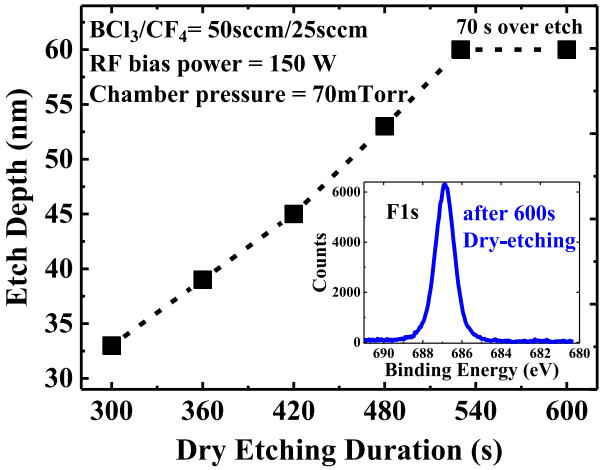

FIGURE 2. p-GaN removal depth as a function of etch duration and XPS F1s signal of a sample dry etched for 600 s.

voltage swing range and the gate lags were improved simultaneously. Therefore, this novel composite Schottky barrier design of normally-off p-GaN gate GaN HEMT exhibits a high potential for high-switching-speed power-electronic applications.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1 shows the cross-sectional schematic and transmission electron microscopy (TEM) profile of the proposed CB p-GaN gate device and its corresponding epitaxial structure. For the proposed CB p-GaN gate HEMT, the epitaxy wafer was grown by metal-organic chemical vapor deposition on 6-in Si (111) p-type substrates. A 300-nm-thick undoped GaN channel layer was grown on top of a 4-μm-thick undoped AlGaN/GaN/AlN buffer transition layer. A 14-nm-thick undoped composite barrier (1-nm-AlN/ 12-nm-$Al_{0.17}Ga_{0.83}N$/ 1-nm-$Al_{0.3}Ga_{0.7}N$) layer was sandwiched between the GaN channel layer and a 60-nm p-type GaN cap layer. The Mg concentration is 3×10^{19} cm^{-3} and the active Mg concentration is 1×10^{18} cm^{-3}, which was confirmed by Hall measurement. This structure exhibited a sheet charge density of 7.2×10^{12} cm^{-2} and a Hall mobility of 1252 $cm^2/V{\cdot}s$ at 300 K after removing the p-GaN cap layer. The STD structure exhibited a sheet charge density of 6.5×10^{12} cm^{-2} and a Hall mobility of 1133 $cm^2/V{\cdot}s$ with the same characterization. For device fabrication, the active region was protected by photoresist and the mesa isolation region was etched to 200-nm depth in a reactive ion etching chamber using BCl_3+ Cl_2 mixed gas plasma. A 3-μm-long p-type GaN gate finger was formed by selective dry etching because of the p-GaN/AlN interface design. A mixture of BCl_3+ CF_4 gas plasma was adopted to remove p-GaN for 530 s to form the gate terminals. The CF_4 plasma reacted with Al atoms and formed a thin AlF_3 etching stop layer when the mixed gas plasma reached the AlN barrier layer. As shown in Fig. 2, the p-GaN removal depth was measured using an atomic force microscope. The AlN layer was fluorinated by CF_4 plasma after the p-GaN removal process, and AlF_3 signal was detected through X-ray photoelectron spectroscopy (XPS) measurements.

To ensure uniform and complete removal of the p-GaN layer, a 600 s etch was used with 70 s over etching, and an obvious etching stop function was achieved by adopting AlN layer design [12]. Subsequently, the sample was immersed into diluted HF/NH_4OH chemical solution to remove the newly formed AlF_3 and AlOx compounds. Ohmic contacts were prepared through electron beam evaporation to form a multilayered Ti/Al/Ni/Au (25/120/25/150 nm) structure sequentially, followed by rapid thermal annealing at 875 °C for 30 s in a nitrogen-rich atmosphere. After the formation of the ohmic contacts, the gate region of Ni/Au (25/120 nm) metal layer was deposited using an electron beam evaporator. Finally, a-200 nm-thick SiO_2surface passivation layer was deposited using an electron beam evaporator. The lengths of gate-to-source (L_{GS}), gate (L_G), gate-to drain (L_{GD}) are 2, 3 and 7μm, respectively. The width of device (W) is 50μm. For comparison, a STD p-GaN gate HEMT with 12 nm $Al_{0.17}Ga_{0.83}N$ barrier layer was also grown and fabricated with an identical process flow.

The schematic band diagrams of the CB and STD p-GaN gate HEMTs are shown in Fig. 3. Because of the large bandgap (3.4 eV) of GaN and the Fermi level (E_F) close to the valence band (E_V), The p-GaN cap can decrease the potential and thus increase the energy barrier in the channel to realized 2DEG depletion, and thus, resulting in normally-off operation [13], [14]. The gate leakage current under positive gate operation is controlled by thermionic emission and affected by the direct tunneling or trap assisted tunneling [15], [16]. When the gate bias was switched from 0 V to a positive bias, the holes were emitted from reverse-biased Schottky junction; thus, the electrons and holes are injected and some of the carriers are trapped in the AlGaN layer during the transient process in STD p-GaN/AlGaN/GaN HEMT [17]. For the composite barrier p-GaN design, the 1-nm-$Al_{0.3}Ga_{0.7}N$/GaN channel behaves similar to a 2DEG channel with good carrier confinement. The main purpose of 12-nm-$Al_{0.17}Ga_{0.83}N$ layer is to improve the epitaxial quality and suppress the lattice mismatch induced dislocation compared to the traditional

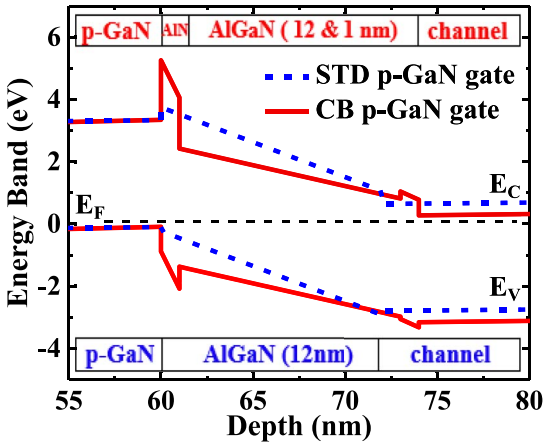

FIGURE 3. Energy band structure at the gate position for CB and STD p-GaN gate HEMT.

high Al mole fraction (20-30%) barrier layer design of GaN HEMT. Finally, the AlN layer forms a high barrier between p-GaN and $Al_{0.17}Ga_{0.83}N$ to minimize the leakage current induced by thermionic emission together with an etching stop layer function.

III. DEVICE PERFROMANCE AND DISCUSSION

Fig. 4(a) shows the $I_{DS}-V_{GS}$ and $I_{GS}-V_{GS}$ transfer curves of the STD and CB p-GaN gate HEMT. The maximum output current density was 272 mA/mm at a gate bias of 8 V and the on-resistance was 5.65 Ω·mm for the STD p-GaN gate HEMT. These results were respectively 320 mA/mm and 5.05 Ω·mm for the CB device. The average subthreshold slope (*S.S*) for the STD device was 375 mV/dec; this value was improved to 167 mV/dec for the CB device. The better *S.S* of the CB p-GaN HEMT was attributed to its better 2DEG carrier confinement and lower leakage current induced by thermionic emission [18]. Meanwhile, the forward gate leakage of the STD device increased rapidly at a V_{GS} of 6 V, and the gate swing range was increased by 1 V in the CB design. The inset in Fig. 4(a) plots the I-V output of both devices to demonstrate the correct characteristic. Fig. 4(b) shows the distribution of V_{TH} (defined by the I_{DS} = 1mA/mm) for 30 devices on the wafer with the same gate length of 3 μm using 1 mA/mm as the criteria. For the STD device, the mean value of V_{TH} was 2.1 V and the standard deviation was 0.2 V. These values were 1.7 V and 0.06 V for the CB device, suggesting good uniformity of the AlN etching stop layer design as a result of the self-terminated p-GaN removal process. However, the composite $AlN/Al_{0.17}Ga_{0.83}N/Al_{0.3}Ga_{0.7}N$ design raised the Fermi level slightly compared with the traditional $Al_{0.17}Ga_{0.83}N$ barrier design, and the V_{TH} was thus reduced. Compared to others published results, CB p-GaN HEMT performed a good current density and low leakage current simultaneously [13], [14].

To investigate the improvement in electrical characteristics of the CB p-GaN gate design, the three-terminals I–V (I_{GS})

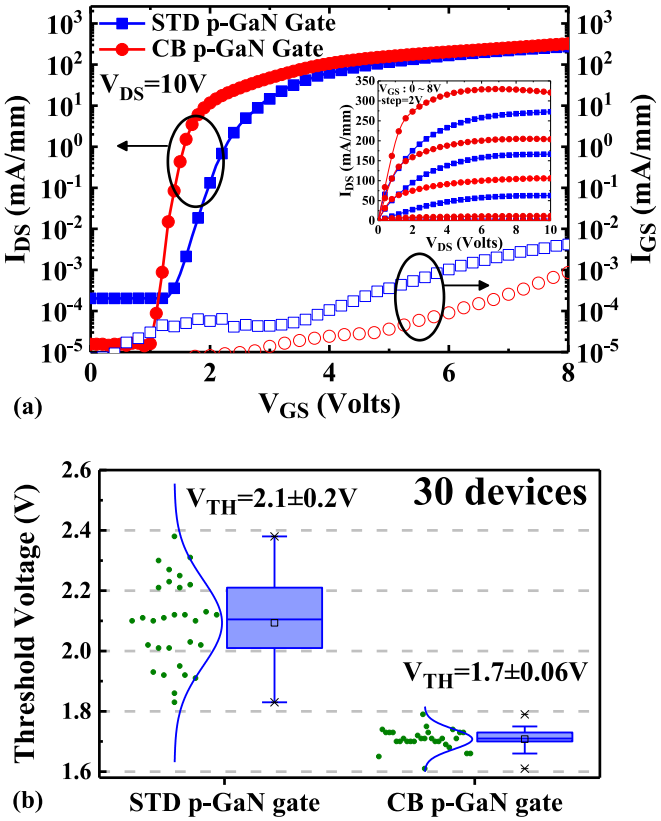

FIGURE 4. (a) $I_{DS}-V_{GS}$ & $I_{GS}-V_{GS}$ transfer and $I_{DS}-V_{DS}$ output characteristics of both devices, (b) V_{TH} distribution of 30 samples for STD and CB p-GaN HEMT.

curves of the device were measured. The gate turn-on voltage (V_{ON}) was determined when the gate leakage current reached +1μA/mm. The V_{ON} of CB p-GaN gate HEMT improved to 7.8 V, and this value was 6.3 V for the STD one owing to the suppression of the thermionic-emission-induced leakage current. The higher V_{ON} is also beneficial for improving the gate voltage swing range and driver voltage dynamic range. Moreover, the AlN barrier layer in the CB p-GaN barrier suppresses the reverse gate leakage current by one order of magnitude (see inset Fig. 5), resulting in an improvement in the off-state breakdown voltage (V_{BR}, I_D = 1mA/mm) from 218 V to 256 V compared to the STD device are shown in Fig. 5.

Fig. 6 shows the dynamic R_{ON} recovery transients from 10 μs up to 1ms with an OFF-state (V_{GSQ} = 0 V and V_{DSQ} = 50 V, duration = 20 ms) stress condition. Then the device was switched on with V_{GS} = 8 V and V_{DS} = 1 V bias conditions and the $R_{ON,D}$ is thus extracted under a duty cycle of 10% for both devices. The value of $R_{ON,S}$ was extracted from the slope of pulse I-V output at V_{GS} = 8 V and V_{DS} = 1 V, which quiescent bias point are with V_{GSQ} = 0 V and V_{DSQ} = 0 V. The degradation in dynamic switching performance was determined by calculating the ratio of $R_{ON,D}/R_{ON,S}$. It reasonably suggests that the $R_{ON,D}/R_{ON,S}$ ratio close to 1 of the CB

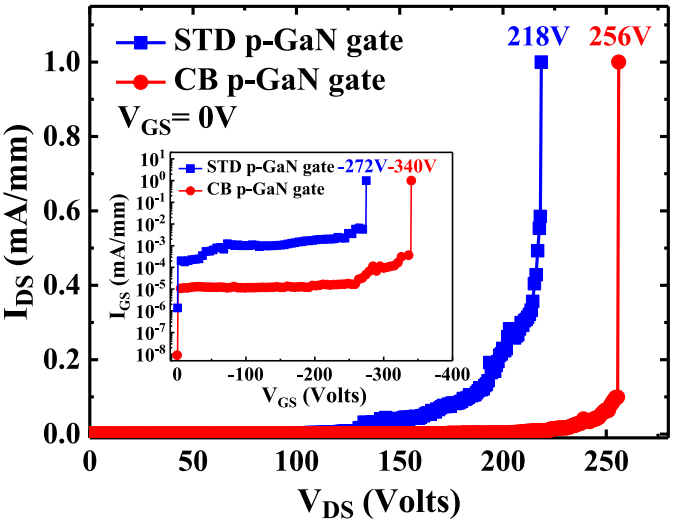

FIGURE 5. Off-state breakdown characteristic and reverse gate leakage for STD and CB p-GaN HEMT.

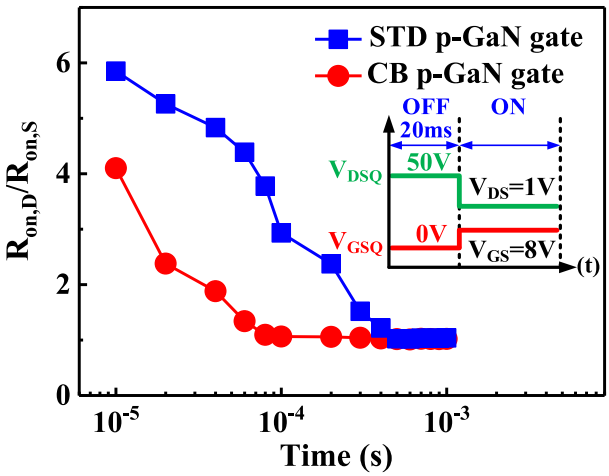

FIGURE 6. Dynamic R_{ON} transients from 10 μs up to 1ms after OFF-state (V_{GSQ} = 0 V, V_{DSQ} = 50 V, duration = 20 ms) to ON-state (V_{GS} = 8 V, V_{DS} = 1 V) switching for STD and CB p-GaN HEMT.

p-GaN gate device was improved from the recovery time of 500 to 80 μs compared to the STD device, which was dominated by low device surface leakage and shallow trap density [19], [20]. In other words, the reduction in the leakage current induced by thermionic field emission in the CB p-GaN HEMT is beneficial for mitigating the performance degradation.

Fig. 7 shows the pulsed I–V characteristics of both devices measured with static quiescent biases (V_{GSQ}, V_{DSQ}) of (0 V, 0 V) at room temperature with an ON-state gate bias of 8 V [21], [22]. The device is switched with 10 μs pulse width and 1 ms period, respectively. The quiescent drain bias (V_{DSQ}) was swept from 0 to 200 V with 50-V increments. Clearly, the current collapse of the STD device is worse than that of the CB device, and the high drain lag of the STD device under relatively high stress lead to I-V slope

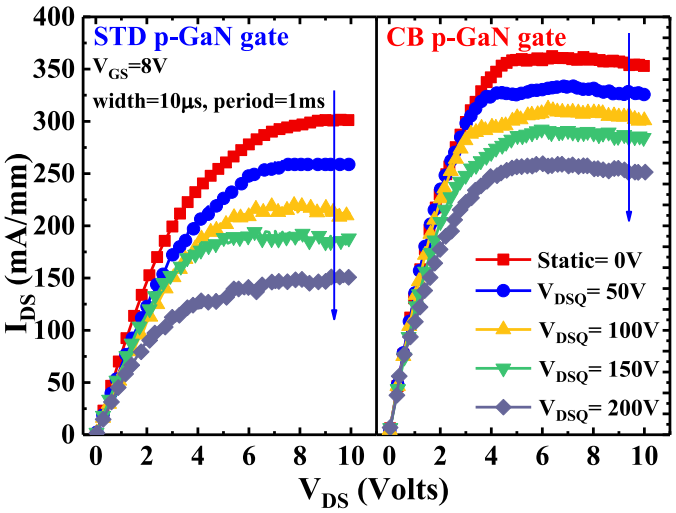

FIGURE 7. Pulsed I_{DS} – V_{DS} characteristics from quiescent gate bias (V_{GSQ}) point of 0 V with 10μs pulse width and 1 ms pulse period. Afterward, the quiescent drain bias (V_{DSQ}) was swept from 0 to 200 V (in 50 V increments).

decreases, indicating that the surface defect trap density is higher than that of the CB device. Therefore, the AlN etching stop layer provides a uniform etching profile of p-GaN removal and thus reduces the surface damage. Moreover, the superior carrier confinement of the CB p-GaN HEMT achieves a better dynamic operation than the traditional design does.

IV. CONCLUSION

In summary, composite 1-nm-AlN/12-nm-$Al_{0.17}Ga_{0.83}N$/1-nm-$Al_{0.3}Ga_{0.7}N$ p-GaN gate HEMTs were successfully fabricated and studied. With a 1-nm AlN etching stop layer design, a better V_{TH} uniformity was obtained in the CB p-GaN HEMT. In addition, the superior surface etching uniformity improved the drain lag, especially at higher drain bias stress. This composite barrier design also had a lower leakage current induced by thermionic emission and a better 2DEG carrier confinement, which are beneficial for suppressing the gate leakage current and gate-lag characteristics compared with those of the STD design. Therefore, the as-developed design exhibits a high potential for repeatable and manufacturable normally-off p-GaN gate HEMT application.

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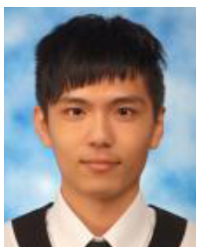

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