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# Design Considerations for 4H-SiC Lateral BJTs for High Temperature Logic Applications

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**ABSTRACT** 4H-silicon carbide (SiC)-based bipolar integrated circuits (ICs) are suitable alternatives to silicon (Si)-based ICs in high temperature applications, owing to superior properties of 4H-SiC and the robust performance of SiC bipolar junction transistors (BJTs). However, cost, size, and manufacturability of 4H-SiC ICs remains inferior to the prevalent Si-based ICs, due to large footprint and high number of epilayers in conventional SiC BJTs. An alternative to overcome these limitations is to use lateral BJTs (LBJTs). Though Si LBJTs have been demonstrated, this is the first time they are explored in 4H-SiC. This paper proposes a symmetric, self-aligned 4H-SiC LBJT design, which is relatively easier and cheaper to manufacture, has fewer epilayers, and is >90% smaller than existing structures. Extensive device simulations and optimization is performed to achieve optimal current gains, at a range of temperatures (27 °C–500 °C). The results suggest current gains of over 100 in devices with base width of 1 $\mu$m, at room temperature. The applicability of the structure is validated by designing a 4H-SiC LBJT-based emitter-coupled logic inverter, which shows stable operation and good speeds (∼3 ns) up to 500 °C, while having high integration density and lower cost.

**INDEX TERMS** 4H-SiC, high temperature operation, lateral bipolar junction transistor (LBJT), symmetric, self-aligned, emitter-coupled logic (ECL).

## I. INTRODUCTION

Small sized silicon (Si)-based integrated circuits (ICs) have become possible today primarily due to the scalability of CMOS technology. However, the applications of these ICs are limited in extreme and hostile environments due to the fundamental limits of Si as a material, especially beyond 300 °C. Compound wide bandgap semiconductors such as silicon carbide (SiC), especially 4H-SiC, has the capability to withstand temperatures well beyond that limit (∼600 °C), due to its low intrinsic carrier concentration and high thermal conductivity [1], [2]. The material can also operate at high speeds, thanks to its high saturation velocity, which is twice as high as that of Si [2]. Several researchers have developed 4H-SiC based circuits that can operate at temperatures well beyond 300 °C, including digital logic circuits [3]–[10], analog circuits [11], and even memories [12]. Since the presence of a critical gate oxide in 4H-SiC metal-oxide–semiconductor field-effect transistors (MOSFETs) is associated with unreliable operation at high temperatures, substantial work is geared towards using devices, without a critical oxide, such as a bipolar junction transistor (BJT) [13]. Thus far, the BJT structures [3]–[10], [14]–[16], currently used in 4H-SiC ICs, are an adaptation of the vertical power BJT structure, which is not really an optimal solution for small-scale ICs. The existing signal level 4H-SiC BJTs are not only unnecessary large (widths > 40 $\mu$m) which escalates the cost per die, but can also be expensive to fabricate due to the highly customized fabrication process. The vertical SiC BJT structures also require several epitaxially grown layers which significantly increases the cost of the base wafers. These issues make it difficult for the current 4H-SiC ICs to achieve high levels of integration density or cost viability, and prove to be a major roadblock in the widespread adoption of the 4H-SiC logic technology.

Therefore, it is imperative to investigate alternate designs for SiC BJTs that overcome these limitations and are

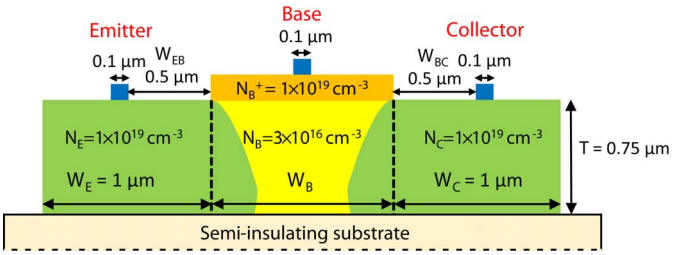



**FIGURE 1. Cross-section of the proposed 4H-SiC lateral BJT with a self-aligned extrinsic base, where the lithographic base width ($W_B$) is indicated by the vertical dashed lines. The effect of lateral straggle on the actual base width is also shown.**

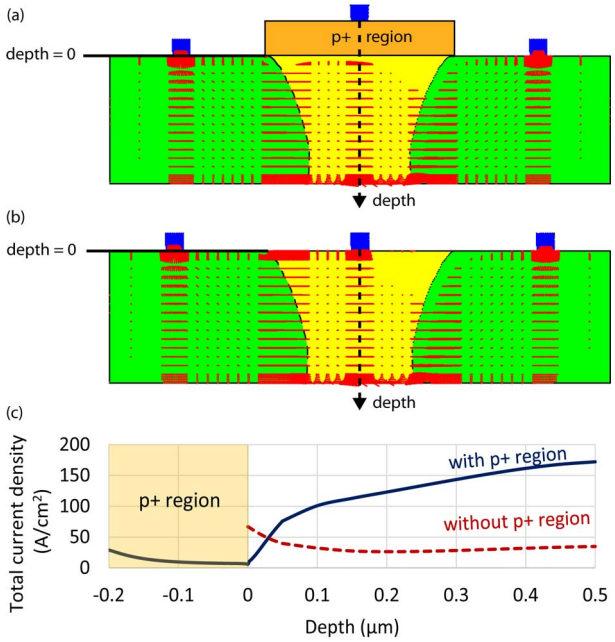



**FIGURE 2. (a) Vector plots showing the current density in the device with p+ and (b) without the p+ extrinsic base. (c) Total current density measured vertically under the base contact (along the dotted arrow in Fig. 2 (a) and (b)) for the LBJT structures with and without the p+ region.**

well-suited for high temperature digital logic applications. Silicon on insulator-based lateral BJTs (LBJT) have been successfully demonstrated in the past [17]–[21], though no previous efforts have been made to investigate the potential of LBJTs in 4H-SiC. Hence, this paper presents for the first time, a symmetric and self-aligned, npn 4H-SiC LBJT structure, that has fewer epilayers, exhibits similar performance, and is substantially smaller in size than the conventional designs. Though only an npn transistor is shown, the pnp counterpart can be made using the same design methodology. To demonstrate the viability of the proposed design, an inverter based on emitter-coupled logic (ECL) technology is designed and optimized using the 4H-SiC LBJT and compared to a conventional 4H-SiC BJT-based ECL inverter.

## II. 4H-SiC LATERAL BJT SIMULATION AND DESIGN

Fig. 1 shows the 4H-SiC LBJT structure, with a self-aligned extrinsic base, aligned to the intrinsic device. A semi-insulating substrate is used to achieve high speed operations by reducing the substrate parasitic capacitances [22]. On top of the substrate, is a lightly doped p-epilayer, which forms the intrinsic base region of the device. To realize the n-type emitter and collector regions, the p-type layer is suitably doped by ion implantation to produce two n+ regions, separated by the intrinsic base. The intrinsic base is self-aligned using a thin ($\sim 0.1 - 0.2$ μm) p+ extrinsic base epilayer, which serves multiple purposes. It helps in achieving narrow base widths, while providing direct low resistivity ohmic contact to the intrinsic base. It also helps in improving the device's performance by creating a vertical electrical field that repels electrons in the base [17] away from the metal base contact, as shown in Fig. 2 (a) and Fig. 2 (c). The highly doped p-epilayer acts as an additional 'barrier' that the electrons need to cross, in order to reach the base contact, thereby reducing the base current and increasing the current gain.

Design rules of 0.1 μm/0.2 μm (minimum feature size/misalignment tolerance) are used for the BJT design. The proposed structure is studied using a 2D device simulator, Taurus$^{TM}$ Medici (provided by Synopsys Inc.) [23], to primarily achieve high peak current gains (measured at $V_{BC} = 0$), for a wide range of temperatures (27 °C – 500 °C). For device modeling purposes, the cut-off frequency is also determined for the proposed structure. The speed performance of the proposed design is gauged by its performance in the circuits [24], as demonstrated in Section IV.

All relevant models such as Auger recombination, bandgap narrowing, incomplete ionization, surface recombination, and others, are considered in the simulations. The 4H-SiC material and model parameters used in the simulations are obtained from experimental results available in [25]–[36]. A partial list of these parameters at room temperature, is summarized in Table 1. The effect of temperature on all the model and material parameters is also accounted for in the simulations. For instance, the mobility value in the simulation is changed with temperature due to the temperature dependent term in the analytic mobility and field-dependent mobility models [23]. Similarly, the effect of temperature on carrier lifetime is modeled, based on [33].

Surface recombination and carrier lifetime are two key parameters that have a significant impact on the performance of the BJT. Surface recombination velocity (SRV) in 4H-SiC typically ranges from $10^3$ cm/s to $10^5$ cm/s and a value of $10^5$ cm/s [36], which indicates substantial surface recombination, is used in the simulations, so that the LBJT is optimized for optimal current gains even when the effect of surface recombination is severe. The carrier lifetime in 4H-SiC is in the range of a few hundred ns to a few μs for devices with epitaxial layers [36], [37], whereas it

**TABLE 1. Partial list of 4H-SiC material and model parameters (at 27 °C) [25]–[36].**

| Parameter name | Value |
|---|---|
| Bandgap | 3.26 eV |
| Permittivity | $9.7\varepsilon_0$ F/cm |
| Electron and hole saturation velocity | $2.2\times10^7$ cm/s |
| Effective density of states for electrons/holes | $1.699\times10^{19}/2.459\times10^{19}$ cm$^{-3}$ |
| Maximum electron/hole mobilities* | 950/108 cm$^2$/Vs |
| Impact ionization coefficients for electrons/holes | a = $1.69\times10^6/3.32\times10^6$ cm$^{-1}$<br>b = $9.69\times10^6/1.07\times10^7$ V/cm |
| Surface recombination velocity | $1\times10^5$ cm/s |
| Bulk carrier lifetime of electrons/holes | 260/300 ns |
| Carrier lifetime in implanted regions | 15 ns |
| Resistivity for contacts on n-/p- type 4H-SiC | $2\times10^{-5}/2\times10^{-3}$ Ωcm$^2$ |

*in the analytic mobility model.

is substantially lesser (<100 ns) for devices with regions formed by ion-implantation [38]–[43], owing to the damage induced by the implants. This damage causes defects which then act as recombination centers, thereby degrading current gain. As the emitter and collector regions in the proposed structure are to be formed by ion-implantation, the lifetime in those regions is set to 15 ns [38], [39] in the simulations, and a higher value (260 ns [33]) is used for the rest of the structure. A detailed discussion on the effect of lifetime and surface recombination on the device performance is provided in Section II-D. Finally, the resistivity for contacts to n- and p-type 4H-SiC is set to $2\times10^{-5}$ and $2\times10^{-3}$ Ωcm$^2$ [35] in the simulations, respectively.

The rest of this section investigates the effect of the various design parameters in the proposed structure and their effect on the performance of the LBJT, at room temperature. The effect of temperature on the LBJT performance is discussed in Section IV.

### A. EMITTER AND COLLECTOR (E/C) CHARACTERISTICS

In order to obtain a symmetric and self-aligned structure with high emitter injection efficiency, the doping of the emitter and collector regions in the proposed structure is set to $10^{19}$ cm$^{-3}$. Though, high emitter doping is desired for better gains and high electron injection efficiency, but for emitter doping ($N_E$) greater than $10^{19}$ cm$^{-3}$, the performance of the transistor degrades, due to the band gap narrowing effect that becomes more pronounced at higher $N_E$. Moreover, in lateral BJTs, the collector doping is kept higher than the base doping ($N_B$), to reduce the effect of current gain degradation caused by the base push out effect [20].

The symmetric nature of the 4H-SiC LBJT not only self-aligns the extrinsic base to the internal device, but also simplifies the fabrication process substantially, as both emitter and collector regions can be achieved via a single implantation step. This makes the emitter and collector regions interchangeable, and hence the transistor operates equally fast in both forward-active and reverse-active modes [20]. The shape of the implant profile and the depth of the emitter and collector regions determines the thickness of the transistor. Fig. 3 shows the effect of increasing the thickness of the transistor on the performance of the proposed design. As evident from the figure, the performance improves when the thickness is increased, because it allows more current to flow away from surface, reducing the surface recombination effect and increasing the gain. However, the thickness is practically limited by the maximum depth of n+ region that can be formed in a 4H-SiC epilayer. The usual maximum implant energy in 4H-SiC is ~600 – 650 keV, with a typical dose of $\sim10^{14}$ cm$^{-2}$, where 3-6 successive implants are generally needed to form a 'box-profile' [44]. Keeping these practical considerations in mind, extensive SRIM [45] simulations are performed to determine the optimal set of implants and their dose and energy.

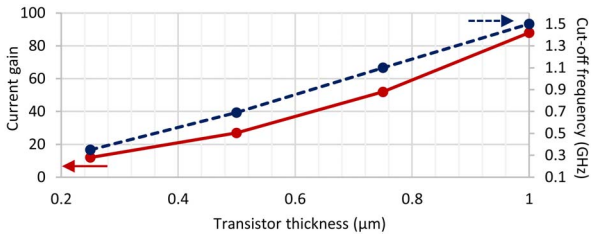
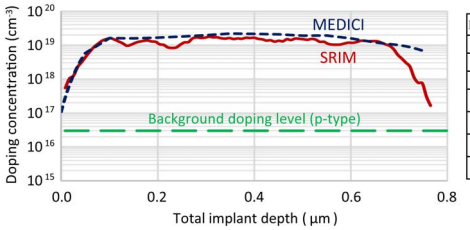



**FIGURE 3. Simulation results showing the effect of varying the transistor thickness on the current gain and the cut-off frequency (at $V_{BC} = 0$) of the proposed structure (with $W_B = 1.1$ μm).**

Fig. 4 shows the optimized implant profile for the emitter and collector regions, which also dictates the depth and the overall transistor thickness to be 0.75 μm. The profile shown in Fig. 4 is used in all simulations, and the effects of vertical and lateral straggle caused by the implantation are also included, as shown in Fig. 1, where the effect of lateral straggle is obtained directly from the simulation output, and is modeled by using the x.char and y.char parameters for horizontal and vertical straggle, respectively. The data for the maximum range and straggle for each implant is obtained from SRIM simulations, which corroborates with experimental results present in [46]. In addition, it is ensured that the doping concentration near the surface is sufficiently high so that low-resistivity ohmic contacts could be achieved in the emitter and collector regions. Ohmic contacts on n-type 4H-SiC with similar doping profiles and doping density, have been demonstrated successfully in the past [47], [48] with good specific contact resistivities (~$10^{-6}$ Ωcm$^2$).




| Energy (keV) | Dose (cm$^{-2}$) |
|---|---|
| 50 | $8.3\times10^{13}$ |
| 100 | $1\times10^{14}$ |
| 180 | $1.4\times10^{14}$ |
| 250 | $1.6\times10^{14}$ |
| 350 | $1.8\times10^{14}$ |
| 500 | $2\times10^{14}$ |
| **Total dose** | **$8.63\times10^{14}$** |

**FIGURE 4. n+ implant profile for the emitter and collector regions simulated in SRIM and modeled in the simulations.**

### B. BASE CHARACTERISTICS

Fig. 5 shows the effect of $N_B$ on the performance of the proposed structure. The speed of the LBJT improves as $N_B$ is reduced, owing to the decrease in the junction capacitance of the device. Decreasing $N_B$ also reduces the holes diffused into the emitter region, which increases emitter injection efficiency, and in turn, improves the current gain. However, it is observed that reducing $N_B$ beyond $3\times10^{16}$ cm$^{-3}$ increases the reverse-bias base-collector junction leakage current, which reduces the $I_{ON}/I_{OFF}$ ratio of the device, as shown in Fig. 6. This is undesirable for BJT operation as the $I_{ON}/I_{OFF}$ ratio should ideally be very high for a switching device [49]. The $I_{ON}/I_{OFF}$ ratio of the proposed design is $\sim10^4$ for an $N_B$ of $3\times10^{16}$ cm$^{-3}$, compared to only $\sim8$ when $N_B = 2\times10^{16}$ cm$^{-3}$. With this tradeoff in mind, $N_B$ is optimized at $3\times10^{16}$ cm$^{-3}$, to achieve maximum performance while maintaining adequate $I_{ON}/I_{OFF}$ ratio. However, having $N_B < N_C$ causes the base-collector depletion region to extend further into the base with increasing $V_{CE}$, and if the base is not wide enough, the BJT might punch-through at high $V_{CE}$ values. This phenomenon can be avoided by operating the BJT at lower $V_{CE}$ values, which is limited by the base width, as discussed next.

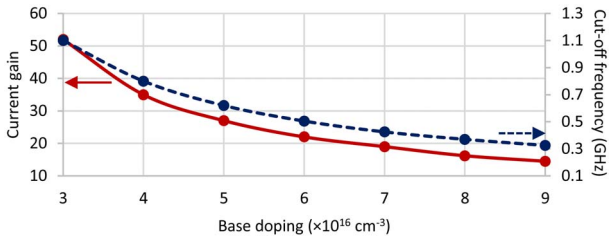



**FIGURE 5.** Simulation results showing the effect of varying the base doping on the current gain and the cut-off frequency (at $V_{BC} = 0$) of the proposed structure (with $W_B = 1.1$ μm).

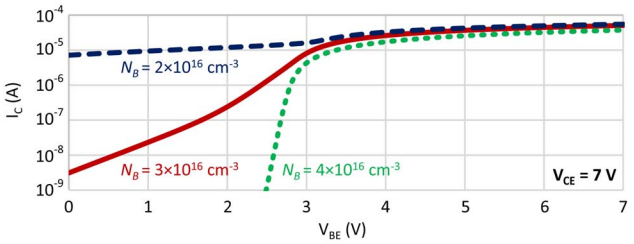



**FIGURE 6.** $I_C$-$V_{BE}$ (at $V_{CE} = 7$ V) plot for $N_B = 2$ - 4 $\times10^{16}$ cm$^{-3}$.

With regards to the base width, the current gain is a strong function of base width, where the proposed structure with a lithographic base width ($W_B$) of 1 μm exhibits a current gain of 102 while a design with $W_B = 1.1$ μm has a gain of 52, at room temperature. Reducing the latter improves the former by reducing the base current. It should be noted that the actual metallurgical base width (where $N_D - N_A = 0$) in the device is less than the lithographic base width ($W_B$), due to the lateral straggle caused by the ion implantation, as evident in Fig. 1. For instance, the metallurgical base width at the surface of the transistor is close to $W_B$, which reduces to $\sim(W_B - 0.4$ μm) towards the bottom of the device. Reducing $W_B$ also lowers the maximum open-base $V_{CE}$ ($V_{CEO}$) that the transistor can operate at, as shown in Fig. 7. $V_{CEO}$ is the highest $V_{CE}$ value before the base-collector junction breaks down and the transistor starts conducting due to an emitter-collector punch-through. The dependence of gain and $V_{CEO}$ on $W_B$, presents a parameter for circuit designers to integrate devices with different sizes on the same chip, depending on the application. For example, 4H-SiC SRAM memory circuits that operate at a supply voltage of 5 V [12], can be made using the LBJT with $W_B = 1$ μm ($V_{CEO} = 5$ V), while achieving high integration (due to small-size) and high-speeds. Other complex circuits with higher operating voltages can be made with devices that have a wider base.

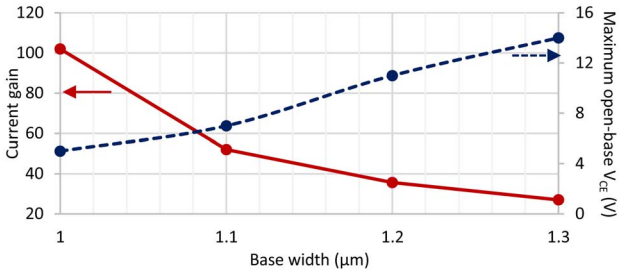



**FIGURE 7.** Simulation results showing the effect of reducing the lithographic base width on the maximum open-base $V_{CE}$ and the current gain (at $V_{BC} = 0$) of the proposed 4H-SiC LBJT.

### C. OTHER DESIGN PARAMETERS

With regards to the lateral dimensions, i.e., the placement of contacts ($W_{EB}$ and $W_{BC}$), increasing the contacts spacing improves the LBJT performance due to the reduction in surface recombination [50], but the effect is not as significant when compared to other parameters such as base width and base doping. This is because, in the proposed LBJT design, the recombination effect is mitigated by the vertical electrical field repelling electrons away from the base contact (as discussed in Section II), hence the current tends to flow away from the surface, and the structure is less susceptible to the surface recombination effect, when compared to vertical SiC BJTs. For instance, when the SRV value for the LBJT is reduced by a factor of $10^5$, the current gain increases by $\sim2.6\times$. Whereas, for the same decrease in SRV, the current gain of vertical BJTs increases by $\sim20\times$ [51].

Similarly, the contact widths do not affect the device performance substantially, hence these dimensions can be tailored according to the capabilities of the lithography technique used. If the resolution of the lithography tool is limited, the contact width can be increased further (but staying within alignment tolerances) without compromising on the device performance. Increasing the contact widths significantly would require the base width to be increased, which would in turn degrade the LBJT performance, as discussed in Section II-B. Furthermore, the gain of the transistor increases

slightly (by ∼6%) when the emitter width ($W_E$) is varied from 0.5 μm to 1 μm, after which it tends to saturate. Hence, $W_E$ and $W_C$ are optimized to be 1 μm, though the total device width can be reduced even further by decreasing them to 0.5 μm, with minimal sacrifice in the performance. This sets the width of the proposed structure to <3.5 μm which is >90% smaller than vertical SiC BJTs [3]–[8], [14]–[16], demonstrating the area-efficiency of the design.

### D. EFFECT OF SURFACE RECOMBINATION AND CARRIER LIFETIME IN IMPLANTED REGIONS ON THE CURRENT GAIN

The gain of 4H-SiC BJTs is limited by surface recombination, owing to a high density of defects at the oxide-semiconductor interface, which create recombination centers or traps at the surface of the transistor. These traps severely reduce the carrier lifetimes in SiC BJTs causing the base recombination current to increase, and the current gain to decrease. The amount of surface recombination is quantified by SRV, which can be reduced by improving the quality of the 4H-SiC/$SiO_2$ interface. Fig. 8 shows the effect of SRV on the current gain of the 4H-SiC LBJT structure. As observed in the figure, the current gain is a strong function of SRV and although a value of $10^5$ cm/s is used for all device simulations in this work, the SRV in the actual device is estimated to be lower, owing to the recent advancements in passivation techniques of 4H-SiC devices. Therefore, the actual current gain values for the proposed structure can be improved by using nitridation based optimal surface passivation methods [52], such as the one proposed in [53] and [54] and briefly described in Section III.

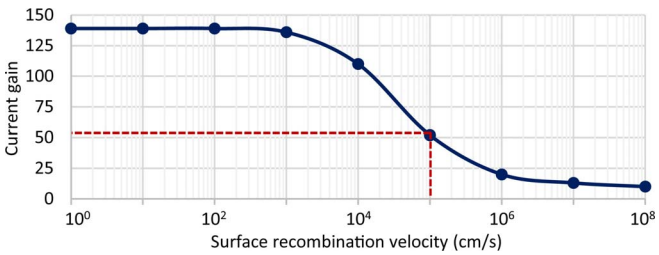



**FIGURE 8. Effect of surface recombination velocity on the current gain of the proposed 4H-SiC LBJT design (with $W_B$ = 1.1 μm). The value of surface recombination velocity used in the simulations and the corresponding current gain is marked with a dashed line.**

Surface recombination is not the only current gain limiting factor in 4H-SiC BJTs. Carrier lifetime also plays a significant role in determining the performance of the BJT. The emitter and collector regions in the proposed structure are formed by ion-implantation, a process that introduces defects due to lattice damage and creates recombination centers, consequently reducing the lifetime and the current gain. The effect of carrier lifetime in the implanted regions on the gain is shown in Fig. 9. As evident from the figure, the current gain deteriorates almost linearly for lifetimes <10 ns, however, experimental lifetime values for 4H-SiC PiN diodes

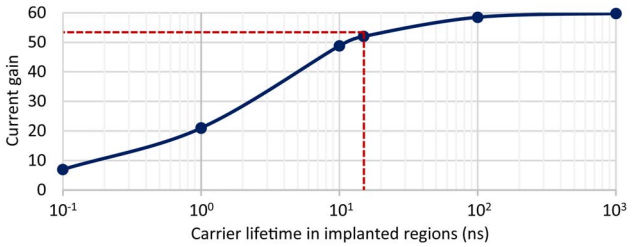



**FIGURE 9. Effect of carrier lifetime in the implanted regions on the current gain of the proposed structure (with $W_B$ = 1.1 μm). The carrier lifetime value used in the simulations and the corresponding current gain is marked with a dashed line.**

formed by ion-implantation are typically in the range of 10 ns – 100 ns [39]–[43], suggesting that good current gains could be achieved for the actual device.

It is also important to note that unlike the carrier lifetime in the implanted regions, the bulk lifetime has negligible effect on the performance of the proposed LBJT. This indicates that surface recombination and carrier lifetime in implanted regions are the dominating performance limiting factors in the proposed structure, which are known to affect all SiC-based devices.

## III. PROPOSED FABRICATION PROCESS OF THE 4H-SiC LBJT

The proposed fabrication process begins with a 4H-SiC wafer with epitaxally grown p+/p epilayers (0.2 μm - $1\times10^{19}$ $cm^{-3}$/0.75 μm - $3\times10^{16}$ $cm^{-3}$) on a semi-insulating substrate. The active regions on the wafer are covered with a masking material followed by the isolation reactive ion etch (RIE) of SiC. The RIE is to be performed in a forming gas such as $SF_6$ and an etch with a depth of 0.95 μm is required to etch SiC all the way down to the semi-insulating substrate. This isolation etch is to be followed by another RIE (0.2 μm deep) to etch the p+ layer, consequently forming the extrinsic base region. The masking material after the p+ etch must be kept intact, as it will serve as a mask for the subsequent ion implantation step. Next the emitter and collector regions are to be formed by ion implantation using the profile described in Section II-A. Finally, a high temperature post-implantation anneal is needed to activate the dopants.

Once the emitter, base, and collector regions are formed, a passivation layer is needed to cover the entire wafer. A nitridation based surface passivation recipe for 4H-SiC [52]–[54] can be used for the 4H-SiC LBJT. The recipe includes oxide deposition, which can be performed using plasma etched CVD (PECVD) or atomic layer deposition (ALD), at a temperature of 300-400 °C, followed by a two-step post-oxidation anneal – NO/1175-1300 °C/2 h and $N_2$/1175-1300 °C/30 min, to suppress the interface states. Finally, contacts are patterned using e-beam lithography, followed by a traditional lift-off process. Ni/Ti/Al [55] or Ti/$TaSi_2$ [56] are suitable contact metals for both p-type and n-type 4H-SiC, and can be used to simultaneously form the

emitter, base, and collector contacts in the transistor. Several research groups have already demonstrated patterning SiC by e-beam lithography with features down to tens of nanometers, and have proposed devices and circuits with features in the sub-micron regime, confirming the viability of the proposed structure in SiC [57]–[59].

**TABLE 2. Comparison of the major process steps required to fabricate the proposed LBJT structure and a conventional SiC BJT [3].**

| Masks | SiC LBJT | Conventional SiC BJT |
|---|---|---|
| 1 | Isolation RIE | Emitter mesa RIE |
| 2 | p+ RIE and emitter/collector implant | p+ base implant |
| 3 | Emitter, base, and collector contacts | Collector window RIE |
| 4 | | Isolation RIE |
| 5 | | Emitter and collector contacts |
| 6 | | Base contact |

Table 2 compares the major process steps required to fabricate the 4H-SiC LBJT and a conventional SiC BJT. As evident from the table, the fabrication of the proposed self-aligned 4H-SiC LBJT requires only three masks (up to the contact formation step), which translates to substantial savings in terms of manufacturing cost and fabrication complexity. Also, since the proposed design is lateral, it requires only two epilayers, compared to $\geq 4$ in a vertical structure [3]–[8], [14]–[16] which further reduces cost and complexity.

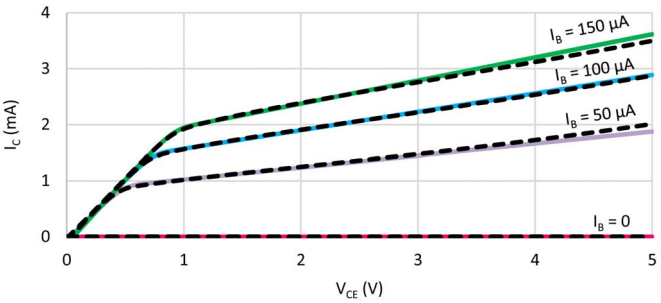



**FIGURE 10.** $I_C$-$V_{CE}$ **fitting results of the proposed structure for** $I_B$ **= 50μA – 150 μA at room temperature (SPICE: solid, MEDICI: dashed), assuming a transistor length of 100 μm.**

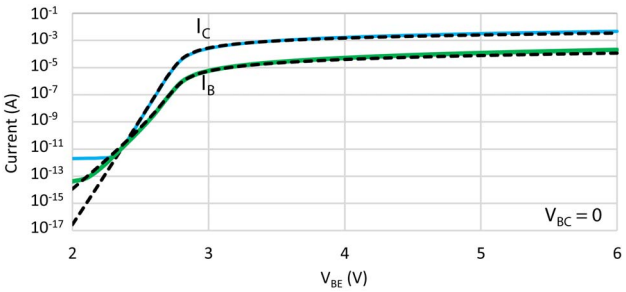



**FIGURE 11. Gummel fitting results of the proposed structure at room temperature (SPICE: solid, MEDICI: dashed), assuming a transistor length of 100 μm.**

## IV. DEMONSTRATING VIABILITY THROUGH CIRCUIT DESIGN

In order to verify the usability of the proposed 4H-SiC BJT structure, it is used to design an ECL based inverter optimized for good noise margins and high speeds. A supply voltage of 10 V is used, to account for the large voltage drop in SiC devices. To withstand the voltage drop over the transistors in the circuit, the 4H-SiC LBJT structure with $W_B$ = to 1.1 μm is used, which has a $V_{CEO}$ of 7 V at room temperature (Fig. 7). At elevated temperatures (500 °C), the $V_{CEO}$ reduces to 6 V due to the increase in the reverse saturation current of the base-collector junction diode. The LBJT also exhibits current gain/cut-off frequency of 52/1.1 GHz at room temperature, which reduce to 35/0.75 GHz and 24/0.5 GHz at 250 °C and 500 °C, respectively. The negative temperature coefficient of current gain is due to the increase in the active acceptor ion concentration in the base with temperature [35]. This phenomenon is accounted for in the device simulations by including the temperature-dependent incomplete ionization model.

### A. DEVICE MODELING AND DESIGN CONSTRAINTS

SPICE, a circuit simulation software, is used to design and optimize the 4H-SiC LBJT based ECL inverter. To achieve this, the Gummel-Poon SPICE model parameters for the LBJT are obtained using graphical and numerical methods and later adjusted so that the SPICE results fit the MEDICI results. Figs. 10 and 11 show the $I_C - V_{CE}$ and Gummel fitting results, respectively, at room temperature, assuming a transistor length of 100 μm.

For simulations at different temperatures (27 °C, 250 °C and 500 °C), a separate SPICE model parameter set is created using the MEDICI data for that temperature. The change in resistivity at high temperatures is also taken into account by changing all resistance values in the circuit at each temperature. An additional constraint for the circuit design is to keep $V_{CE}$ for all the LBJTs in the circuit below 7 V at all times, as discussed in Section II-B. The ECL inverter is optimized for good noise margins (NMs) – measured using a fan-out of ten configuration, and high speeds – measured using an 11-stage ring oscillator, at a wide range of temperatures.

### B. ECL INVERTER DESIGN AND OPTIMIZATION

Fig. 12 illustrates the 4H-SiC LBJT based ECL circuit, where its design is optimized for the finger length of the BJTs and resistors values. The ECL technology is based on a differential amplifier that compares the input voltage to a fixed reference voltage ($V_R$) set at the middle of its voltage swing ($V_R = -1.5 \times V_{BE(ON)}$) [51]. $V_R$ is set by the reference voltage circuit through its resistors $R_{1,2,3}$. The sizes of its LBJTs ($Q_{1,D1,D2}$) are not critical to the performance of the ECL gate, hence they are set to the minimum size of 25 μm, to maintain a small footprint. However, this length is not suitable for the output stage LBJTs ($Q_{INV,\ BUFF}$), as they do not provide adequate NMs due to insufficient current to the load. Their size is optimized to be 300 μm, since

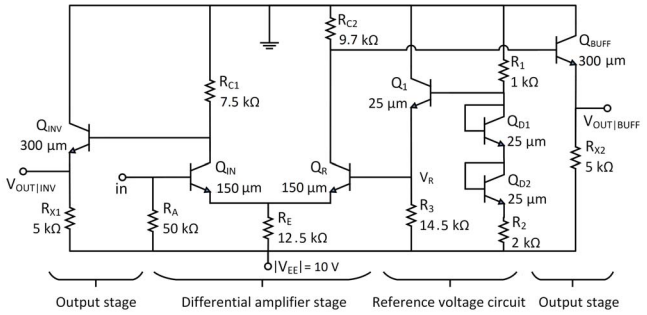



**FIGURE 12. Circuit diagram of the ECL inverter based on the proposed 4H-SiC LBJT, indicating the optimized length of the BJTs and the sizes of the resistors.**

no significant improvements in NMs is observed if the size is increased further. Similarly, the sizes of the differential amplifier LBJTs ($Q_{IN,R}$) are increased to improve the speed of the inverter. Their sizes are set to 150 µm, as further increase in size does not improve the speed performance. Similar design considerations for high speed and adequate NMs are made while optimizing the resistor values.

**TABLE 3. Comparison of ECL circuits (at $|V_{EE}| = 10$ V) designed and optimized using 4H-SiC LBJT and conventional SiC BJT.**

| Circuit | Temp. (°C) | Avg. noise margins (V) | Propagation delay (ns) | Active area (µm²) | Static power consumption (mW) |
|---|---|---|---|---|---|
| (1) SiC LBJT | 27 | 0.72 | 2.92 | 3,027 | 13.6 |
| | 250 | 0.87 | 2.73 | | 12 |
| | 500 | 0.83 | 3.34 | | 12.2 |
| (2) Conventional SiC BJT* | 27 | 0.96 | 3.07 | 9,103 | 37.8 |
| | 250 | 0.96 | 2.95 | | 34.9 |
| | 500 | 0.79 | 2.38 | | 36.8 |
| (3) Conventional SiC BJT† | 27 | 0.87 | 18.2 | 14,955 | 14.9 |
| | 250 | 0.77 | 23.7 | | 12.7 |
| | 500 | 0.75 | 26.4 | | 13.4 |

*using the BJT structure as presented in [4].
†using the BJT structure as presented in [4] but with LBJT design rules.

Table 3 summarizes the stability, speed, active area, and static power consumption of the LBJT based ECL inverter (henceforth called circuit 1) and shows a comparison to conventional SiC BJT ECL inverters – circuits 2 and 3, where circuit 2 has all vertical BJTs, as presented in [4] (sized at 25 µm with design rule of 3 µm/2 µm), whereas circuit 3 is designed using the same vertical device presented in [4] but with the application of LBJT design rules instead. Though it should be noted that for the vertical BJT used in circuit 3, the emitter width and the distance of base contact to emitter mesa remain unchanged [4], to mitigate emitter size effect and surface recombination effect, whereas all other dimensions are scaled according to the LBJT design rules. Consequently, the width of the transistor is comparatively bigger than LBJT, but smaller than the transistor used in circuit 2. The application of smaller design rules reduced the transistor width in circuit 3, thereby reducing the device current. Therefore, BJTs with large finger size and higher resistor values had to be used in circuit 3 to get adequate noise margins, thereby making the overall area much larger. The area is measured to the first order, as the active area of the circuit, and is defined as the sum of the area occupied by all the BJTs and all the resistors present in the circuit. However, the actual area of a cell maybe greater due to practical considerations such as alignment tolerances, minimum overlaps, critical dimensions, interconnect metals and dielectric layers, which will affect the actual area factor for all the circuits.

As can be seen from table 3, the speed for circuit 1 and circuit 2 is comparable because even though the junction capacitance of the LBJT is smaller, the smaller currents in the LBJT negates the effect of lower capacitances on the circuit speed. On the other hand, circuit 3 suffers from both smaller currents and relatively higher capacitance (since the width of the transistor in circuit 3 is bigger than that in circuit 1), hence it shows considerably higher delays. The static power consumption of both circuit 1 and 3 is lower than that of 2 (by ∼64%), due to smaller device currents.

Hence, the analysis in table 3 shows that the proposed 4H-SiC LBJT based ECL inverter occupies a much smaller active area (67% and 80% reduction when compared to circuit 2 and 3, respectively), consumes low static power, and can operate at high speeds, while having adequate noise margins. The smaller size, which translates to low cost per die, and low power for the SiC LBJT design are achieved without any sacrifice on the performance of the circuit; validating the potential of the proposed 4H-SiC LBJT for small scale logic applications.

## V. CONCLUSION

In conclusion, a small-sized, symmetric, self-aligned, and easy to manufacture, lateral BJT in 4H-SiC is proposed featuring high current gains and speeds at a wide range of temperatures. The design is >90% smaller and requires half the number of epilayers and process steps when compared to vertical BJTs. The performance of the LBJT is a function of the base width, where a design with $W_B = 1$ µm has a current gain of 102 at 27 °C. The performance can be further improved by using optimal surface passivation methods to lower the surface recombination effects. An ECL inverter based on the proposed 4H-SiC LBJT shows a 67% - 80% reduction in active area and 64% less power consumption when compared to a conventional 4H-SiC BJT based ECL inverter, without sacrificing the operation stability and speed. The high performance, simple fabrication, and small geometry of the proposed design is a significant step towards realizing robust, and small sized 4H-SiC ICs, potentially catapulting them from niche to mainstream applications.

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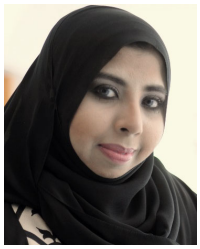

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