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Multiple-Submicron Channel Array Gate-Recessed AlGaN/GaN Fin-MOSHEMTs

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ABSTRACT In this paper, the multiple-submicron channel array gate-recessed AlGaN/GaN fin-metal-oxide-semiconductor high-electron mobility transistors (fin-MOSHEMTs) were fabricated using the photoelectrochemical oxidation method, the photoelectrochemical etching method, and the He-Cd laser interference photolithography method. The multiple-submicron channel array was formed using the He-Cd laser interference photolithography system. The gate-recessed structure and the directly grown gate oxide layer were performed using the photoelectrochemical etching method and the photoelectrochemical oxidation method, respectively. The subthreshold swing and the extrinsic transconductance were improved in the resulting devices with a narrower channel width. Furthermore, the unit gain cutoff frequency and the maximum oscillation frequency were also enhanced using a narrower channel width in the multiple-submicron channel array AlGaN/GaN fin-MOSHEMTs.

INDEX TERMS AlGaN/GaN metal-oxide semiconductor high electron mobility transistors, fin-channel structure, laser interference photolithography method, multiple-submicron channel array, photoelectrochemical method.

I. INTRODUCTION

In the past decades, the two-dimensional electron gas (2 DEG) induced in the AlGaN/GaN heterostructure was widely utilized in GaN-based high-electron mobility transistors (HEMTs) due to its inherent advantages of high electron density and high electron mobility. Consequently, the Schottky-structured GaN-based metal-semiconductor high-electron mobility transistors (MESHEMTs) were demonstrated in various applications, previously [1], [2]. However, the performances of the GaN-based MESHEMTs suffered from the small breakdown voltage and the large gate leakage current. To improve the high voltage operation and the high power-handling capability, the GaN-based metal-oxide semiconductor high-electron mobility transistors (MOSHEMTs) were fabricated by depositing dielectric insulators or directly growing oxide insulator between the gate metal and the GaN-based layer [3]–[5]. Recently, in view of gate control capability and improved performances of fin structure in Si-based devices, the fin-type structure was also utilized in GaN-based HEMTs and ZnO-based MOSFETs [6]–[8]. Since the multiple channel structure was verified to improve the resulting performances, the multiple-mesa-channel structure was fabricated on GaN-based HEMTs and the other MOS devices [9]–[13]. In this work, the multiple-submicron channel array was fabricated on the gate-recessed AlGaN/GaN MOSHEMTs using a laser interference photolithography system which was a simple and low cost instrument compared with the electron-beam writer. Besides, the gate-recessed structure was formed using a photoelectrochemical (PEC) etching method and the gate oxide insulator was directly grown using a PEC oxidation method. The damage of the gate-recessed surface could be avoided by using the PEC etching method. Furthermore, as like the direct growth of SiO_2 on the Si wafer, the interface state density could be reduced by the direct growth of the gate oxide layer on the GaN-based films using the PEC oxidation method. To study the function of the width of the submicron channel, various channels were fabricated on the AlGaN/GaN MOSHEMTs by directly adjusting the interference photolithography period.

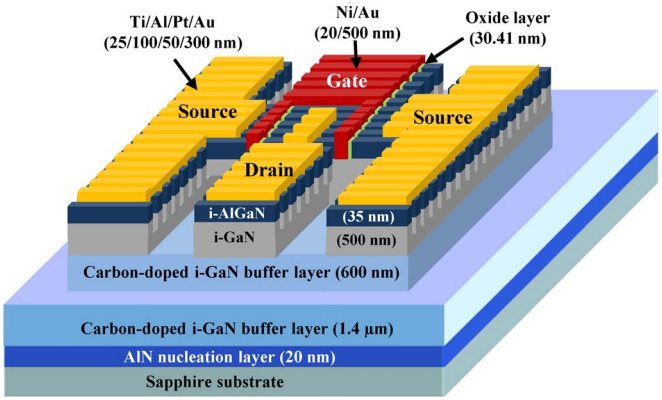

FIGURE 1. Schematic configuration and epitaxial structure of multiple-submicron channel array gate-recessed AlGaN/GaN fin-MOSHEMTs.

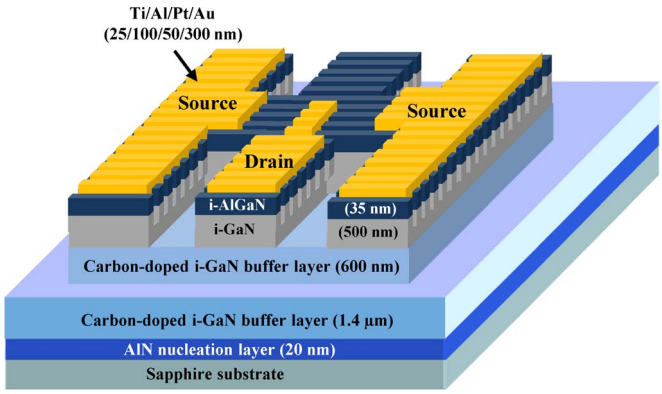

FIGURE 2. Schematic configuration of the fabrication process after forming drain electrode and source electrode.

II. EXPERIMENT

The schematic configuration and the used epitaxial structure of the multiple- submicron channel array gate-recessed AlGaN/GaN fin-MOSHEMTs are illustrated in Fig. 1. The ammonia molecular beam epitaxial system was used to grow the epitaxial layers on c-plane sapphire substrates. The epitaxial layers included a 20-nm-thick AlN nucleation layer, a 2.0-μm-thick carbon-doped i-GaN buffer layer, a 500-nm-thick undoped i-GaN layer, and a 35-nm-thick undoped $Al_{0.15}Ga_{0.85}N$ layer. The $Al_{0.15}Ga_{0.85}N$ layer was referred as AlGaN layer, hereafter. The electron density and the electron mobility of the 2 DEG induced in the AlGaN/GaN heterostructure measured by a Hall measurement system were $1.1 \times 10^{13} cm^{-2}$ and 1700 cm^2/Vs, respectively. The associated sheet resistance was 368 Ω/sq.

After cleaning the sample using acetone and methanol, two-intersected He-Cd laser beams illuminated on the AZ6112 photoresist-spread whole sample to pattern interference fringes. Adjusting the incident angle of the two-intersected He-Cd laser beams in the laser interference photolithography system, the interference photolithography period could be changed. Therefore, the channel width of the resulting multiple-submicron channel array could be adjusted. When the illuminated photoresist in the interference fringe pattern was completely removed using the developer, the Ni/Au metal mask was deposited on the patterned AZ6112 photoresist using an electron beam evaporator system. After the Ni/Au metal above the photoresist strips was lifted off, the multiple-submicron channel array was formed by etching the undoped AlGaN layer down to a 70 nm depth using the PEC etching method. The PEC etching method was reported, previously [14]. After a 500-nm-thick Ni metal was deposited using an electron-beam evaporator system, the mesa region (310 μm × 320 μm) was patterned using a standard photolithography method. Using the Ni mask, the mesa region was formed by etching the carbon-doped i-GaN buffer layer down to the depth of 600-nm using a BCl_3 etchant in a reactive-ion-etching system. After removing the Ni metal mask, the sample was dipped into an $(NH_4)_2S_x$ solution to completely remove the native oxide resided on the surface of the undoped AlGaN layer [15]. The Ti/Al/Pt/Au (25/100/50/300 nm) metals of the drain electrode and the source electrode were deposited using an electron-beam evaporator system and were then patterned using a lift-off process of the standard photolithography method. The separation distance between the drain electrode and the source electrode was 6 μm. Because the following directly grown PEC gate oxide layer should be stabilized and annealed at 700 °C for 2 hours, the long term thermal stability Ti/Al/Pt/Au metals were utilized as the ohmic metals of the drain and source electrodes [16]. After making ohmic contacts of the drain electrode and the source electrode in a rapid-thermal-annealing system at 850 °C for 2 minutes, the resulting schematic configuration was shown in Fig. 2. Using the measurement of transmission line method, the contact resistance of the ohmic contact was 7.0×10^{-6} Ω-cm^2. To make gate-recessed structure, two-finger gate region (1 μm × 50 μm) was opened on the deposited 500-nm-thick SiO_2 mask using a standard photolithography method and a lift-off process. By using the PEC etching method, the two-finger gate region was etched about 10 nm down to the undoped AlGaN layer as the gate-recessed structure. After completely removing the native oxide using the $(NH_4)_2S_x$ surface treatment [15], an oxide layer was directly grown to form the fin gate oxide layer and the channel passivation layer using the PEC oxidation method. The PEC oxidation method was reported, previously [17]. A 30±2-nm-thick gate oxide layer was obtained, when the sample was then annealed in a N_2ambient furnace at 700 °C for 2 hours. The annealed oxide layer was the stable β-Al_2O_3 and Ga_2O_3 mixed film [18]. Because the native oxide was completely removed using the $(NH_4)_2S_x$ surface treatment, the performances of the grown oxide layer could not be affected by the possible introduction of the native oxide. Using photoassisted capacitance-voltage measurement, the interface state density was $5.1 \times 10^{11} cm^{-2}eV^{-1}$ [18]. The off-state breakdown voltage was larger than −100 V. The gate

metal of Ni/Au (20/500 nm) was then deposited using an electron-beam evaporator system. After removing the SiO_2 mask using a 0.5 % BOE chemical solution, the multiple-submicron channel array gate-recessed AlGaN/GaN fin-MOSHEMT was fabricated as shown in Fig. 1. In the multiple-submicron channel array, two kinds of channel width of 210 nm and 450 nm were fabricated, respectively. Figure 3 (a), (b), and (c) respectively shows the transmission electron microscope (TEM) images of the top view, cross-sectional view and the extended cross-sectional view of the multiple-submicron channel array with a channel width of 210 nm, in which the width of one channel period was 640 nm, the channel number of the multiple-submicron channel array was 78 within a gate width of 50 μm, and the total channel width was 16.4 μm. On the other hand, for the fin-MOSHEMTs with a channel width of 450 nm, the width of one channel period was 1.18 μm, the channel number of the multiple-submicron channel array was 42 within a gate width of 50 μm, and the total channel width was 18.9 μm. For the comparison purpose, the 50-μm-wide single channel was also fabricated in the fin-MOSHEMTs.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The performances of the various AlGaN/GaN fin-MOSHEMTs were measured using an Agilent 4156C semiconductor parameter analyzer. Figure 4 (a), (b) and (c) respectively shows the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) under various gate-source voltages (V_{GS}) of the single channel fin-MOSHEMTs and the multiple-submicron channel array fin-MOSHEMTs with channel width of 450 nm and 210 nm. The associated saturation drain-source current (I_{DSS}) of the various fin-MOSHEMTs operated at $V_{DS} = 10$ V and $V_{GS} = 5$ V was 493 mA/mm, 292 mA/mm, and 406 mA/mm, respectively.

Figure 5 shows the drain-source current and the extrinsic transconductance (g_m) as a function of the gate-source voltage of the various AlGaN/GaN fin-MOSHEMTs operated at a drain-source voltage of 10 V. The threshold voltage (V_{TH}) was -2.3 V, -0.7 V, and -0.4 V for the single channel fin-MOSHEMTs, the multiple-submicron channel array fin-MOSHEMTs with the channel width of 450 nm and 210 nm, respectively. It could be found that the threshold voltage of the fin-MOSHEMTS was reduced and shifted toward the positive direction with a narrower channel width. This phenomenon was attributed to that the 2 DEG channel could be more effectively depleted by the surrounding lateral electric field from the side wall of the fin gate in a narrower channel. As shown in Fig. 5, the extrinsic transconductance g_m was 93 mS/mm, 128 mS/mm, and 197 mS/mm for the single channel fin-MOSHEMTs and the multiple-submicron channel array fin-MOSHETs with a channel width of 450 nm and 210 nm operated at $V_{DS} = 10$ V, respectively. Since the gate control capability could be enhanced in a narrower channel width under the same total channel width, it was worth to note that the extrinsic transconductance could be significantly enhanced using the multiple-submicron channel array with a narrower channel width.

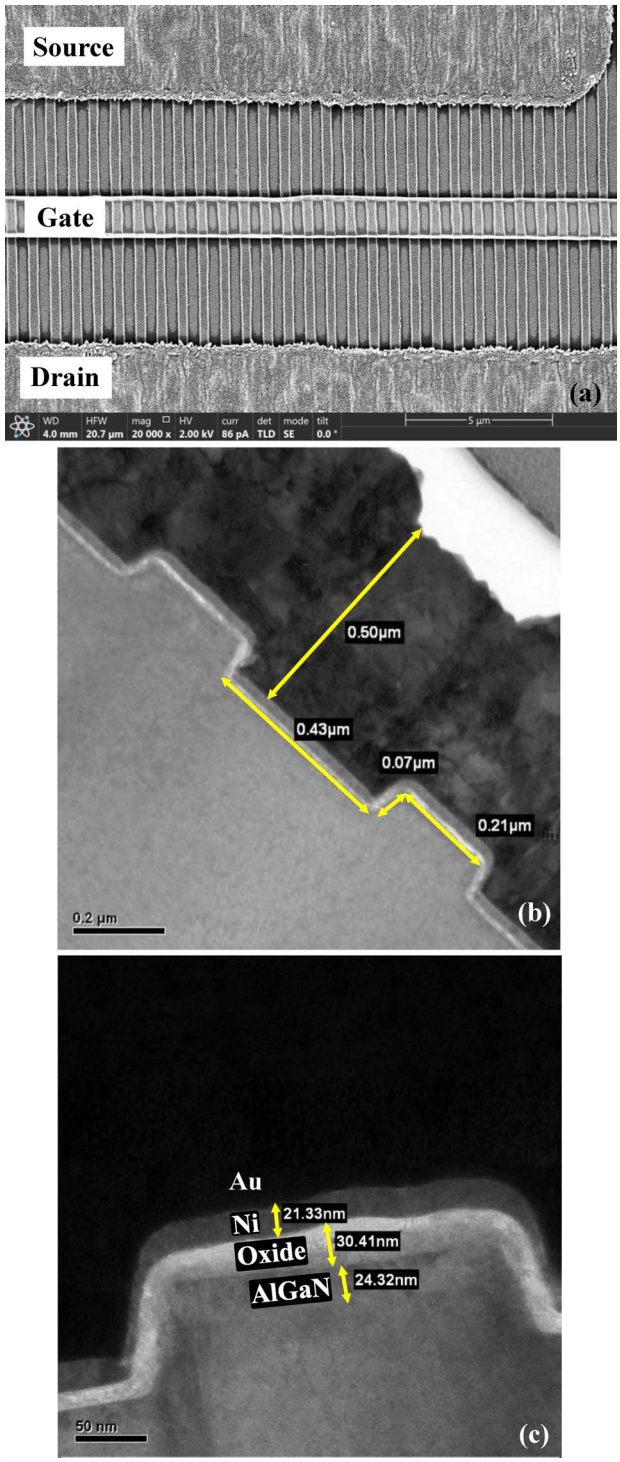

FIGURE 3. Transmission electron microscope images of (a) top view, (b) cross-sectional view and (c) extended cross-sectional view of multiple-submicron channel array with a channel width of 210 nm.

Figure 6 shows the drain-source current-gate-source voltage ($I_{DS} - V_{GS}$) characteristics of the various

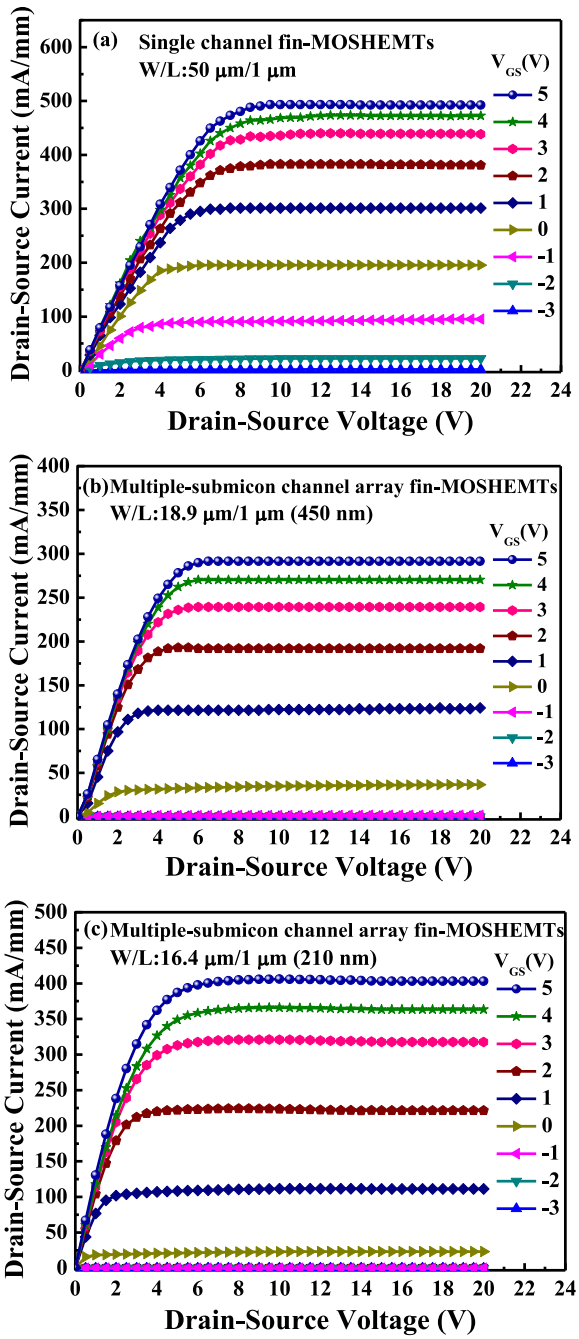

FIGURE 4. Drain-source current-drain-source voltage characteristics of (a) single channel fin-MOSHEMTs, and multiple-submicron channel array fin-MOSHEMTs with channel width of (b) 450 nm and (c) 210 nm.

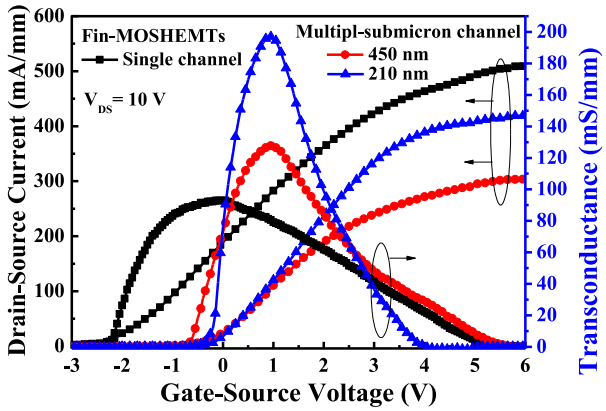

FIGURE 5. Drain-source current and transconductance as a function of gate-source voltage of various AlGaN/GaN fin-MOSHEMTs.

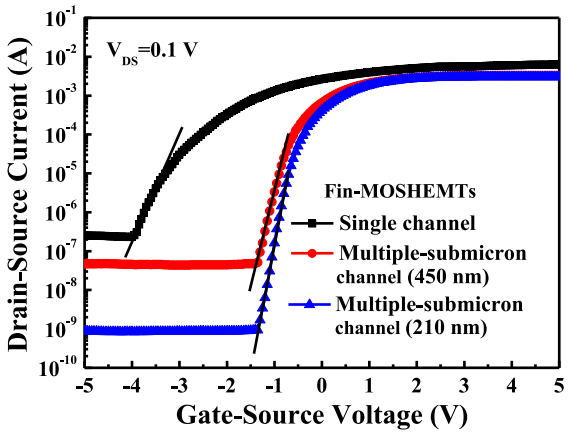

FIGURE 6. Drain-source current-gate-source voltage characteristics of the various AlGaN/GaN fin-MOSHEMTs operated at V_{DS} of 0.1 V.

fin-MOSHEMTs operated at $V_{DS} = 0.1$ V. The subthreshold swing (S) was defined as $S = dV_{GS}/d(\log I_{DS})$ [19]. The subthreshold swing of 370 mV/decade, 189 mV/decade, and 116 mV/decade was derived for the single channel fin-MOSHEMTs, and the multiple-submicron channel array fin-MOSHEMTs with a channel width of 450 nm and 210 nm, respectively. The subthreshold swing decreased with a reduction of the channel width. To study the gate leakage current, the gate-source leakage current as a function of the gate-source voltage of the various fin-MOSHEMTs operated at a V_{GS} of −50 V was measured using a 4156C semiconductor parameter analyzer. The gate leakage current of 500 nA, 280 nA and 255 nA was obtained for the single channel fin-MOSHEMTs, and the multiple-submicron channel array fin-MOSHEMTs with a channel width of 450 nm and 210 nm, respectively.

To study the high frequency performances, the Agilent 8510C network analyzer was used to measure the various fin-MOSHEMTs. Figure 7 shows the short-circuit current gain and the maximum available power gain as a function of frequency derived from the measured S-parameters. The unit gain cutoff frequency (f_T) was 5.6 GHz, 6.0 GHz, and 6.4 GHz, and the maximum oscillation frequency (f_{max}) was 10.9 GHz, 12.0 GHz, and 12.9 GHz for the single channel fin-MOSHEMTs and the multiple-submicron channel array fin-MOSHEMTs with a channel width of 450 nm and 210 nm, respectively. It was worth to note that the maximum oscillation frequency was improved with a narrower channel width. This improvement phenomenon was attributed to the smaller output conductance of the narrower

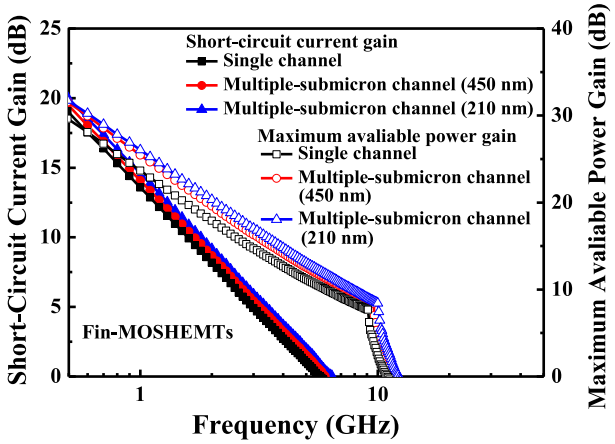

FIGURE 7. Short-circuit current gain and maximum available power gain as a function of frequency of various AlGaN/GaN fin-MOSHEMTs.

channel width [20], [21]. For the same channel width of 50 μm, the effective total channel area was increased in the multiple-submicron channel array with a narrower channel width due to the added channel area caused from the side wall area of the fin structure. Consequently, the parasitic capacitance, including the gate-source capacitance and the gate-drain capacitance, was increased in the structure of the narrower channel width. However, since the side wall area of the gate was very small compared with the 50-μm-wide gate area, the parasitic capacitance was kept at a similar value. In general, the unit gain cutoff frequency was proportional to the inverse parasitic capacitance and proportional to the extrinsic transconductance. Therefore, the unit gain cutoff frequency was enhanced in the multiple-submicron channel array structure with a narrower channel width, in which exhibited a larger extrinsic transconductance and a similar parasitic capacitance.

IV. CONCLUSION

In this work, to study the function of the channel width under the same channel width, the multiple-submicron channel array gate-recessed AlGaN/GaN MOSHEMTs were fabricated using PEC oxidation method, PEC etching method and the He-Cd laser interference photolithography method. To compare the performances of 50-μm-wide single channel structure, two kinds of multiple-submicron channel array with a channel width of 450 nm and 210 nm were fabricated, respectively. The width of the one channel period was 1.18 μm and 640 nm in the multiple-submicron channel array with a channel width of 450 nm and 210 nm, respectively. Under the same 50-μm-wide gate width, the channel number of 42 and 78 in the multiple-submicron channel array with a channel width of 450 nm and 210 nm, respectively. The associated total effective channel width was 18.9 μm and 16.4 μm, respectively. Since the total effective gate area was a little increased with a narrower channel width, the parasitic capacitance was expected to be increased, but still kept at a similar value. Furthermore, the extrinsic transconductance of 93 mS/mm, 128 mS/mm, and 197 mS/mm was obtained for the single channel fin-MOSHEMTs and the multiple-submicron channel array fin-MOSHEMTs with a channel width of 450 nm and 210 nm, respectively. In view of the similar parasitic capacitance and the enhancement of the extrinsic transconductance, the unit gain cutoff frequency of the fin-MOSHEMTs was improved using a multiple-submicron channel array structure with a narrower channel width. Since the output conductance was smaller in a narrower channel width, the maximum oscillation frequency was also enhanced in the multiple-submicron channel array gate-recessed fin-MOSHEMTs with a narrower channel width. In this work, the subthreshold swing was improved with a narrower channel width in the multiple-submicron channel array gate-recessed AlGaN/GaN fin-MOSHEMTs. It is expected that the multiple-submicron channel array is a promising structure in MOS devices. The performances of the multiple-submicron channel array AlGaN/GaN fin-MOSHEMTs can be further improved by reducing the channel width from submicron scale into nanometer scale using a shorter wavelength laser interference photolithography system or using an electron-beam writer system.

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