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Demonstration of Symmetric Lateral NPN Transistors on SOI Featuring Epitaxially Grown Emitter/Collector Regions

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This paper is based on a paper entitled "First Demonstration of Symmetric Lateral NPN Transistors on SOI Featuring Epitaxially-Grown Emitter/Collector Regions," presented at the 2017 IEEE S3S Conference.

ABSTRACT Symmetric lateral NPN bipolar junction transistors on Si-on-insulator having epitaxially grown emitter/collector regions are demonstrated, for the first time. A novel notch-assisted epitaxy scheme has been developed using faceted Si epitaxial (epi) layers as reactive-ion-etch mask to expose the vertical intrinsic-base epi-seeding surfaces and the epi emitter and collector are automatically connected to the extension regions for metal contact and/or for electrical probing. Functional transistors with good quality device *I-V* characteristics were obtained with post-epi rapid thermal annealing. The results suggest a path forward for devices suitable for low-cost THz electronics applications. Some learning about the fabrication, as revealed from measured device characteristics, are discussed.

INDEX TERMS SOI lateral BJT, epitaxially grown emitter.

I. INTRODUCTION

Asymmetric Si-on-insulator (SOI) lateral bipolar transistor (LBJT) with a quasineutral base width, W_B, of about 2 mm was first demonstrated about thirty years ago (Fig. 1) [1]. With the advanced lithography in CMOS manufacturing today, it should be possible to fabricate SOI LBJT with quasineutral base widths of about 10 nm. It should be noted that for a device with W_B of 10 nm, the emitter-collector (E/C) spacing (or equivalent gate length for the FET counterpart) is actually 30-40 nm, depending on the intrinsic-base doping concentration, because emitter-collector spacing includes the space-charge regions on each side of the intrinsic base.

Model calculations suggest the f_T and f_{max} of an SOI LBJT increases as W_B is reduced, with $f_T > 350$ GHz and $f_{max} > 1$ THz when W_B is scaled down towards 10 nm [2], [3]. By adopting a fin-structure, similar to FinFET for CMOS, model calculations suggest f_{max} could reach 1.4 THz [4].

At present, state-of-the art vertical SiGe HBT (IBM's 9HP) has peak f_{max} under 400 GHz [5]. To reach f_{max} of 1.5 THz, InP HEMT with a gate length of 25 nm is needed [6].

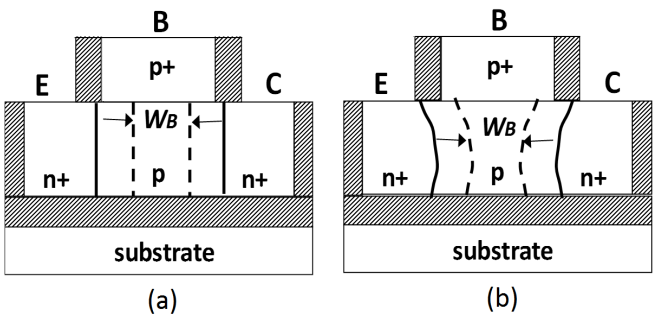

FIGURE 1. Schematic illustrating the structure of a symmetric NPN LBJT on SOI. The collector is as heavily-doped as the emitter. The quasineutral base width W_B is smaller than the physical E-C separation by the depletion layers on both emitter and collector sides. (a) Illustration of uniform base-width profile necessary for thin-base transistors. (b) Illustration of W_B profile using high-dose ion implantation for E/C formation.

Therefore, there should be strong motivation for developing SOI LBJT technology having W_B of about 10 nm, which is expected to be much more cost efficient than InP HEMT, for THz electronics applications.

To date, reported experimental studies of SOI LBJTs were all performed using high-dose ion implantation to form the E/C regions. They all follow a CMOS-like process to fabricate NPN only or to integrate NPN and PNP, using a CMOS mask set with minimum L_{DES} (emitter-collector separation at mask level) of 80 nm [7], [8]. While the results showed excellent device characteristics, such as high drive current and low E/C series resistance, they also revealed the need to use L_{DES} of smaller than 45 nm and to avoid high-dose I/I for E/C formation if the goal is to achieve controlled and reproducible W_B of about 10 nm. High-dose E/C implantation has large lateral implantation straggle and requires high-temperature (typically 1000° C or higher) post-implant anneal, resulting in large variation in W_B device-to-device and large non-uniformity of W_B within a device, as illustrated in Fig. 1.

In this paper, we demonstrate functional SOI NPN LBJTs using a novel low-temperature *in-situ*-doped lateral Si epitaxy to form the E/C regions, instead of high-dose ion implantation process. The process scheme for forming epitaxially grown E/C region is described. For the proof of concept purpose, the W_B for devices of this work are not aggressively scaled where the mask set, and hence the minimum L_{DES} dimension, were the same as in [7] and [8]. However, the process can be utilized to fabricate aggressively scaled base widths with proper lithography. Typical transistor characteristics are shown and discussed. Several process issues revealed from detailed electrical measurements of the affected devices are also discussed.

- **Substrates: 200mm SOI wafer**
- **intrinsic base ion-implant and STI/CMP process**
- **Permeable oxide, extrinsic base poly & hard mask deposition**
- **Base lithography, hard mask and poly-Si RIE**
- **Ultra-thin spacer formation and post etch clean**
- **Faceted sacrificial undoped Si epitaxy**
- **Base edge notch formation by epi RIE**
- ***In-situ* Phosphorus doped E/C epitaxy**
- **SiO_2 dep. & CMP to remove HM & planarize E/C**
- **E/C Activation and forming gas anneal**

FIGURE 2. Process flow to fabricate symmetric SOI lateral NPN bipolar transistors featuring a novel notch-assisted epitaxial E/C growth technique.

II. PROCESS FLOW AND EPITAXIAL-E/C PROCESS SCHEME

The device fabrication process flow is outlined in Fig. 2, and the epi-E/C formation scheme is schematically illustrated in Fig. 3. Starting substrates were 200 mm SOI wafers with a Si thickness of ∼55nm. Intrinsic base regions were formed by a multi-step ion implantation of BF_2 (at various target depth by adjusting implant dose and energy to achieve uniform profile), followed by a rapid-thermal anneal (RTA) process at 1000 °C for 5 sec for a target base doping density, $N_B \sim 2.4 \times 10^{18}cm^{-3}$. A standard shallow trench isolation (STI) and Chemical-Mechanical-Polishing (CMP) processes were used to isolate devices and form active areas. A poly-crystalline (poly-) Si layer of ∼100 nm was then deposited on a reaction-formed permeable oxide, followed by formation of zero level alignment marks and a CMP step to polish the poly-Si. Extrinsic base was formed by successive ion implantation of poly-Si using BF_2 through a thin low-temperature oxide mask and activated in an RTA furnace at 1000 °C for 5 sec. A tri-layer hard mask was then formed on top of poly-Si and the extrinsic base region was patterned using lithography and Reactive-Ion-Etch (RIE), and the etch was end-pointed on the permeable oxide. The process was then followed by a two-step wet clean process in diluted hydrofluoric acid and $NH_4OH:H_2O_2:H_2O$ solutions to clean the RIE damage/ residues, ultra-thin silicon nitride spacer deposition and spacer RIE. A highly uniform facetted undoped Si epitaxy process was developed with high selectivity to the spacer and base hard mask materials. The pre-epi wet clean chemistry and prebake epitaxy conditions (i.e., temperature and pressure) play a critical role in quality and selectivity of the epi. Moreover, facet formation was achieved by controlling HCl content during the growth process. A time-controlled Si etch in an RIE chamber was then developed to etch the sacrificial Si and expose the vertical base sidewalls. As can be seen in Fig. 3(d), a notch is formed at the E/C regions which allows the E/C junctions to be formed right at the exposed edges of the base region and potentially form a uniform base width. The E/C regions were then formed by selective epitaxial growth of *in-situ* phosphorus doped Si at a concentration of about $2 \times 10^{20}cm^{-3}$ at 725 °C. Wafers were then covered by a stack of highly conformal and relatively-high-temperature oxide (R-HTO), with relatively low deposition rate, and plasma-enhanced-chemical-vapor-deposition (PECVD) oxide, with very fast deposition rate. The oxide was then planarized by CMP. A second non-selective CMP was then utilized to remove the extrinsic base hard mask, epi nuclei (caused by low selectivity Si notch recess) and expose the B/E/C pads for direct electrical probing.

In this first experiment, no silicide was formed on the exposed extrinsic-base polysilicon or on the exposed E/C silicon extension regions. This helped us to practice various successive high-temperature anneals and electrical tests by direct probing on the highly doped base and E/C regions. All post process anneals were followed by a forming gas anneal at a temperature of 400 °C. In addition, all steps of the flow were monitored by Scanning Electron Microscopy (SEM) during the development. Fig. 4 shows sample top-down SEM images of an NPN LBJT, indicating well-formed faceted epi (used as RIE mask), notch with exposed vertical Si base surface for seeding epitaxial growth of E/C, and the well-formed epi-E/C with extension regions for electrical contact/probing. Transmission Electron Microscopy (TEM)

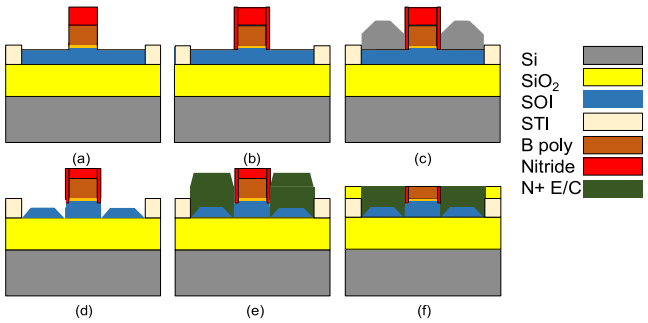

FIGURE 3. Schematic of the novel notch-assisted epitaxial emitter/collector growth method utilized to fabricate SOI lateral bipolar transistors after (a) HM and poly RIE, (b) spacer formation and clean, (c) sacrificial faceted E/C epitaxy, (d) notch formation by RIE, (e) *in-situ* phosphorus-doped E/C epitaxy and (f) oxide deposition and CMP. The notch is created using a two-step process (sacrificial faceted epi and RIE) to facilitate the symmetric E/C epitaxy.

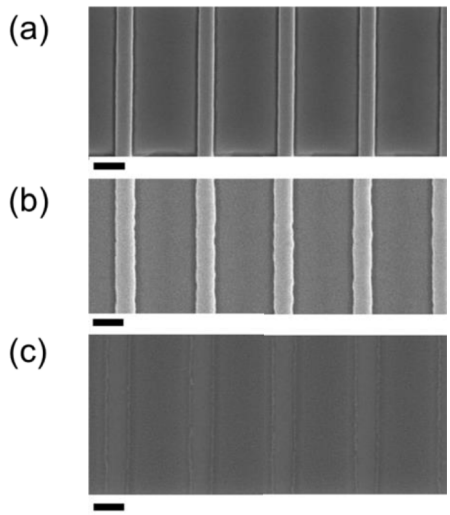

FIGURE 4. Top-down SEM images of the devices after (a) sacrificial faceted epi, (b) notch exposure by RIE and (c) E/C *in-situ* phosphorous doped epitaxy. Scale bars are 200nm.

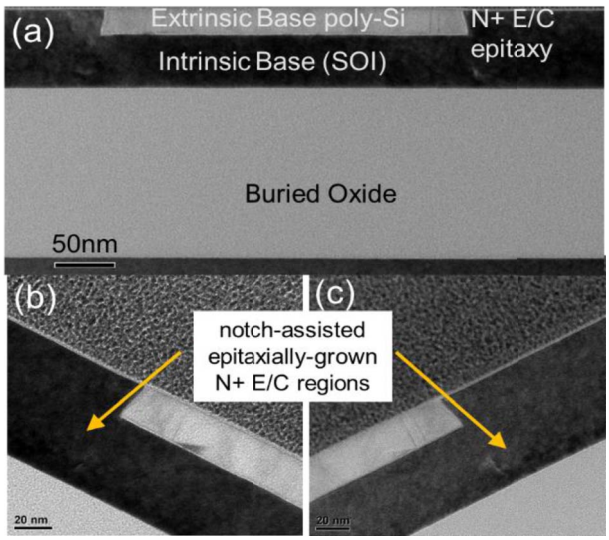

FIGURE 5. Cross-section TEM images of a lateral bipolar NPN after notch-filling *in-situ* phosphorus-doped E/C epitaxy and planarization steps. Higher magnification images near E/C regions are shown in (b) and (c). Epi has been uniformly grown and no void exists.

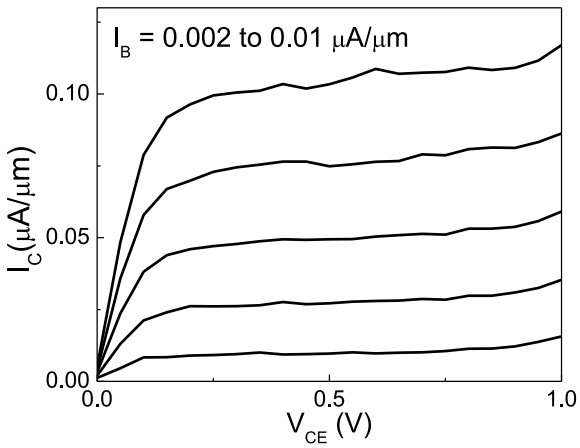

FIGURE 6. Output characteristics of a lateral SOI NPN BJT with epitaxial emitter/collector with $L_E = 0.12$um.

images in Fig. 5 show uniform, void free, and well-formed E/C epi layers.

III. MEASURED DEVICE CHARACTERISTICS

The fabricated transistors were measured as processed (post epi planarization, but before RTA) and after RTA at 850 °C for 20 sec. Fig. 6 shows the output characteristics of an NPN device after RTA, suggesting a well-behaved device. Fig. 7 compares the Gummel characteristics of an NPN device measured before and after RTA. Prior to RTA, the transistor did not function properly, showing exceedingly high base current, I_B, and low collector current, I_C, suggesting the E-B and C-B diodes were not yet activated properly. After RTA, the Gummel characteristics are as expected for a good quality transistor. The fact that it requires high-temperature RTA to form device-quality E-B and C-B diodes are consistent with reports on *in-situ*-doped polysilicon emitter process, which is used in all modern vertical BJT, including vertical SiGe HBT [9]. The data in Fig. 6 and Fig. 7 also suggest that the post-epi RTA at 850 °C for 20 sec appears adequate for epitaxial E/C activation.

In Fig. 7, the currents at large V_{BE} are limited by the high emitter and base series resistance (no silicide was formed). The base current at medium V_{BE} shows a pronounced 120-mV/decade component, suggesting the base current is dominated by recombination in E-B diode space-charge region, similar to the reported observation in devices with implanted E/C.

The total base current can be decomposed into a 60-mV/decade part, due to recombination of holes inside the n-type emitter region and/or recombination of electrons inside the p-type quasineutral base region, and a 120 mV/decade part due to recombination within the E-B diode space charge region. The 120-mV/decade component is

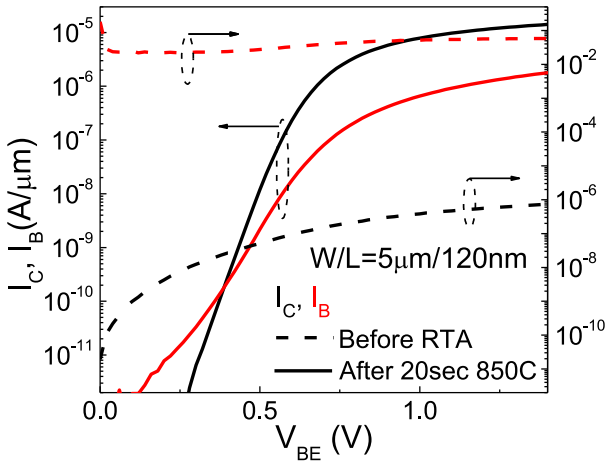

FIGURE 7. Gummel plots for an NPN LBJT before (dashed lines) and after (solid lines) RTA at 850°C for 20 sec.

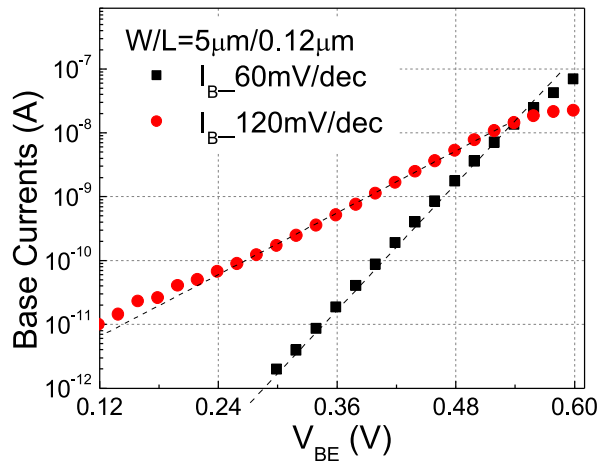

FIGURE 8. Base current components of the SOI LBJT device in Fig. 7.

expected to be reduced significantly after silicide formation step [10]. These base current components for the transistor in Fig. 7 are shown in Fig. 8. They appear noticeably larger than those reported for implanted-E/C devices [10]. A possible reason for this is discussed in the next section.

IV. PROCESS LEARNING FROM ELECTRICAL MEASUREMENTS

As this is the first attempt of a novel epi-E/C formation process for SOI LBJT, the experiment was designed to acquire fabrication process learning and develop process optimization. In this section, we discuss some process learning as revealed by the measured device currents.

A. BORON-DEFICIENT REGION IN EXTRINSIC BASE

In this first experiment, in the interest of process simplicity, high-dose boron implantation was used to dope the extrinsic-base polysilicon layer, with an intended final uniform doping concentration of 2×10^{20} cm^{-3}, the same as used previously in implanted-E/C experiments [7], [8]. There was no high-temperature anneal after boron implantation prior to epi-E/C

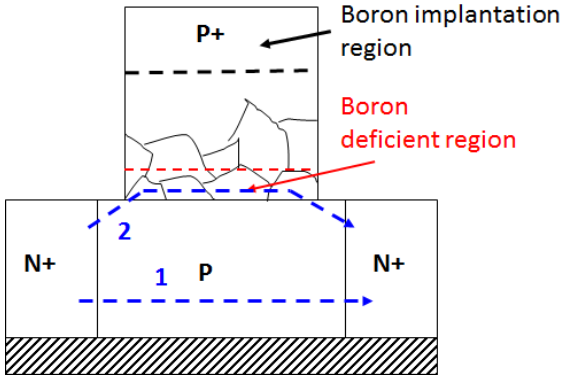

FIGURE 9. Schematic illustrating a boron-deficient region could form at the bottom of the extrinsic base polysilicon due to insufficient post-implant annealing, providing a parasitic path (path 2) for electron flow besides the normal path (path 1). (After [11]).

formation. That is, thermal diffusion of implanted boron in the extrinsic-base polysilicon layer was done at the same time when the epi-E/C regions were activated by RTA.

The transistor in Fig. 7 after RTA at 850°C for 20 sec shows well-behaved base and collector currents, but the currents are relatively higher than expected based on previous implanted-E/C devices [8]. The unexpectedly high collector and base currents are likely caused by the presence of a boron-deficient region in the extrinsic base adjacent to the intrinsic base, as explained below.

For the device in Fig. 7, the post-implantation RTA at 850°C for 20 sec was not adequate to diffuse the implanted boron uniformly throughout the extrinsic-base polysilicon layer. In previous experiments, it was observed that it may require an RTA of longer than 15s at 1000°C to consistently achieve uniform diffusion of the implanted boron throughout the extrinsic-base polysilicon layer [11]. The result is a boron-deficient region in the extrinsic base adjacent to the intrinsic base, as depicted schematically in Fig. 9. Electrically, this boron deficient region acts like a parasitic BJT having a very lightly doped base region (electron path 2), operating in parallel with the intended regular BJT (electron path 1). Since the collector current is inversely proportional to the base doping concentration, the lightly doped parasitic BJT, when present, greatly increases the measured collector current. The base current associated with the parasitic BJT is due to recombination of electrons (parasitic collector current) inside the p-type polysilicon base region [10]. That is, high collector current due to the presence of parasitic BJT is accompanied by high base current as well, as is the case in Fig. 7.

Additional evidence of the existence of a boron-deficient region in the extrinsic base adjacent to the intrinsic base can be found by examining the Gummel currents after the additional RTA cycle. In Fig. 10, the Gummel currents measured after the first 20 sec RTA at 850 °C and again after an additional 20 sec RTA at 850 °C are shown for two transistors. They clearly show that the currents are reduced by

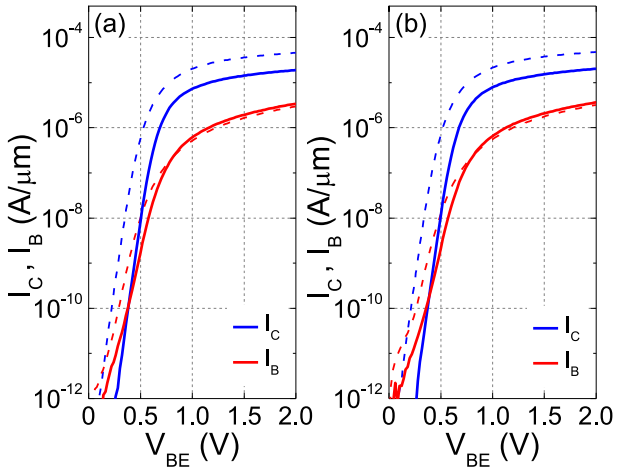

FIGURE 10. **Comparison of Gummel currents measured after the first RTA (dash lines) and again after an additional RTA (solid lines). The results for two sample transistors are shown: (a) W/L = 5μm/0.1μm (b) W/L = 5μm/0.12μm.**

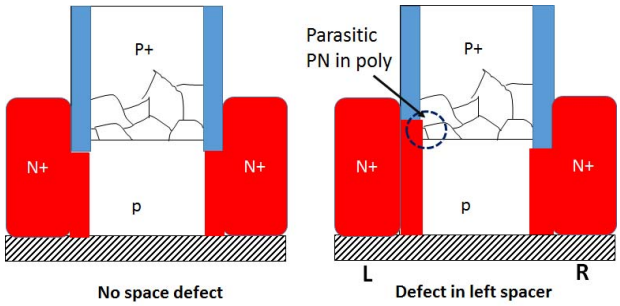

FIGURE 11. **Schematic showing the formation of a parasitic PN diode in the extrinsic-base polysilicon due to defect in the spacer, connected to the n+ region on the left (L). When the L PN diode is forward biased, the parasitic diode could inject electrons into the base and hence increase the collector current (electrons collected at the R n+ region) noticeably. When the L PN diode is reverse biased, the leakage current due to the parasitic diode adds to the leakage current measured at the L n+ region.**

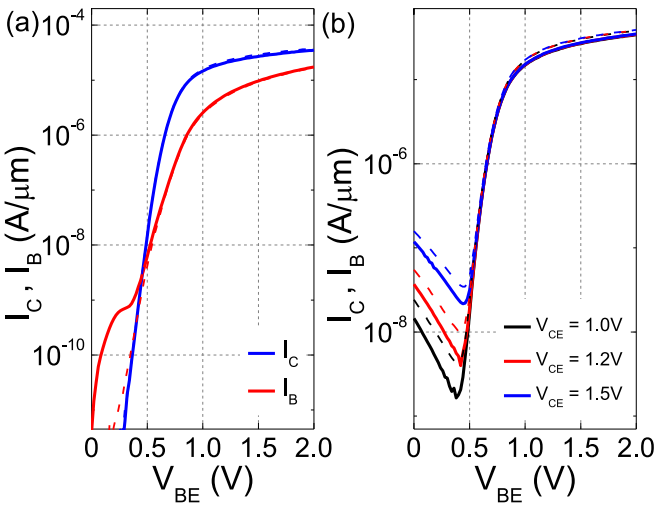

FIGURE 12. **Measured Gummel currents for one of the transistors that shows signs of parasitic diode on the emitter side, but not on the collector side. (a) Gummel currents measured at V_{BC} = 0 V in forward mode (solid lines, with emitter-base diode forward biased) and in reverse mode (dash lines, with collector-base diode forward biased). (b) Forward mode and reverse mode collector currents measured fixed V_{CE} = 1.0 V, 1.2 V, and 1.5 V.**

more than 10X from the first RTA to the second RTA. The data is consistent with the boron-deficient-region model, where the second RTA results in more uniform boron doping in the extrinsic-base polysilicon layer, significantly reducing or even almost eliminating the parasitic BJT.

The issue of boron-deficient-region can be avoided with post-implant high-temperature thermal diffusion prior to epi-E/C formation. A preferred approach is to use *in-situ*-doped polysilicon which is fairly uniformly-doped as deposited. In practice, *in-situ* boron-doped polysilicon has been used successfully as extrinsic base in the demonstration of SiGe-OI LBJT [12].

B. PROCESS RELATED E-B AND C-B DIODE DEFECTS

Epitaxially growing E/C regions should result in E-B and C-B diodes without defects associated with high-dose ion implantation. However, the E-B and C-Bs diode may still have defects caused by other process related issues. One process issue in our first experiment has to do with defects in the vertical spacers on the extrinsic-base polysilicon regions, as discussed below.

It is obvious from Fig. 3 that emitter-collector spacing includes the vertical spacers on both sides of the extrinsic-base polysilicon region. As a result, very thin (8nm as deposited and sub-3nm post process) spacers were used in our experiment. These thin spacers were subjected to extensive RIE prior to epi-E/C growth. A local defect in the final spacer, in the form of a pinhole or locally missing material, could lead to the formation of a parasitic PN diode, as illustrated in Fig. 11. This parasitic diode could lead to excess currents in the measured *I-V* characteristics, as exhibited in Fig. 12 by one of the transistors.

Figure 12(a) compares the Gummel currents measured at $V_{BC} = 0$ V in both the forward mode and reverse mode. For clarity, let us refer to Fig. 11 and designate the L-side n+ region to be the emitter and the R-side n+ region to be the collector. Accordingly, forward-mode operation means the L-side diode is forward biased, and reverse-mode operation means the R-side diode is forward biased. The forward-mode collector current shows a distinct hump at low currents. This additional hump feature in the current can be explained if we assume the presence of a parasitic PN diode on the emitter side or L-side, but not on the collector side or R-side, as illustrated in Fig. 11. In forward mode, this parasitic PN diode is turned on, injecting electrons into the base. As these parasitic electrons reach the R-side n+ region, they add to the measured collector current. In reverse mode, this parasitic PN diode has zero voltage across it (Gummel currents measured at $V_{BC} = 0$ V) and hence has no effect on the measured collector current.

Figure 12(b) compares the Gummel plots of the forward mode collector currents measured at three fixed V_{CE} values

and the Gummel plots of the reverse mode collector currents measured at the same fixed V_{CE}. For a given V_{CE}, the B-C diode is reverse biased when $V_{BE} < V_{CE}$. At $V_{BE} = 0$ V, the collector current is simply the leakage current of the B-C diode at a reverse bias of V_{CE}.

Let us focus just at the measured collector currents at $V_{BE} = 0$ V in Fig. 12 (b). The currents in forward mode are due to leakage currents from the R-side diode, while the currents in reverse mode are due to leakage currents from the L-side diode. It is clear that the L-side diode shows higher leakage than the R-side diode, consistent with the assumption of a parasitic PN diode on the L-side.

V. CONCLUSION

Symmetric lateral NPN bipolar junction transistors on SOI having *in-situ*-doped epitaxially grown emitter and collector have been successfully demonstrated, for the first time. A novel notch-assisted epitaxy scheme was developed using faceted silicon epitaxial layers as reactive-ion-etch mask to expose the vertical intrinsic-base epi-seeding surfaces. The process results in the epitaxial emitter and collector being automatically connected to extension regions for metal contact and/or for electrical probing. The results suggest a path to build low-cost CMOS-compatible SOI LBJT with quasineutral base widths of about 10 nm that can operate at THz frequency range.

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GHAVAM G. SHAHIDI, photograph and biography not available at the time of publication.