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High-Uniformity and High Drain Current Density Enhancement-Mode AlGaN/GaN Gates-Seperating Groove HFET

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ABSTRACT In this paper, we report on a novel E-mode AlGaN/GaN gates-seperating groove heterostructure field-effect transistor (GSG HFET). The current turn-on/off is controlled by changing gate voltage to regulate the horizontal energy band between the double gates. A threshold voltage of 0.23 V and a high drain current density of 851 mA/mm are obtained in GSG HFET. Compared with the proposed depletion-mode device, the maximum drain current of the GSG HFET deceases slightly (about 7%). It is noteworthy that the threshold voltage is less sensitive to the etching time. The devices show high-uniformity threshold voltage of 0.23 V within wide etching time range from 5 to 9 min.

INDEX TERMS E-mdoe, high current density, high-uniformity threshold voltage, GSG HFET.

I. INTRODUCTION

GAN based heterostructure field-effect transistors (HFETs) have received great attention in the energy-efficient power switching applications, due to the excellent characteristics of GaN over the conventional silicon [1], [2]. Normally-off GaN based HFETs are highly desirable in power switching applications for safety, power consumption and cost reasons [3]. In the last years, various techniques regulating vertical energy band have been developed to realize Enhancement-mode (E-mdoe) GaN based HFETs. The proposed approaches mainly include gate recess [4], [5], p-type gate injection [6], cascade structure [7], fluorine plasma treatment [8], [9], metal–2DEG Schottky tunnel junction [10], [11] and so on. The gate-recess technique has been widely studied and improved [12]. However, it still has the following problems: i) the drain saturation current (I_{dss}) and on resistance (R_{on}) always become worse due to the increase of channel resistance; ii) the uniformity of threshold voltage is poor, caused by the uncontrollable of the inductively-coupled-plasma (ICP) etch rate and the induced surface defects during the etching process [13]. Although the p-GaN solution seems to represent a promising technology for E-mode devices, the low value of I_{dss} is still a noteworthy issue.

In this paper, a novel E-mode AlGaN/GaN gates-seperating groove heterostructure field-effect transistor (GSG HFET) is proposed for the first time. This structure consists of double gates, while a barrier and low 2DEG density region at AlGaN/GaN heterojunction located between the gates is realized by ICP etching. The gate and drain voltages regulate the height and width of the barrier by adjusting the horizontal conduction energy band, which controls the current turn-on/off. A high current density is realized in the novel E-mode AlGaN/GaN HFET. Moreover, the value of V_{th} is less insensitive to the etching time, and high-uniformity threshold voltage is realized.

II. DEVICE FABRICATION

The used AlGaN/GaN heterostructure was grown by metal organic chemical vapor deposition (MOCVD) on a 4 inch SiC substrate. The heterostructure consists of a 2 nm GaN cap layer, a 18 nm $Al_{0.2}GaN$ barrier layer, a 1 nm AlN interlayer, and a 2 μm GaN buffer layer, as shown in

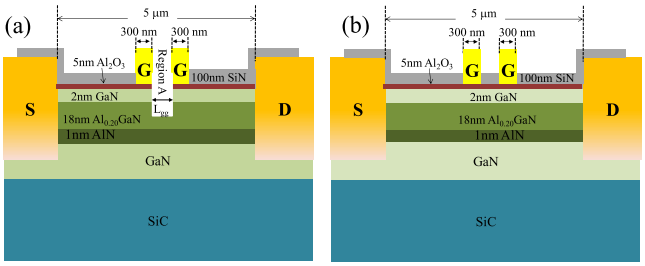

FIGURE 1. **Schematic cross section of (a) AlGaN/GaN GSG HFET and (b) D-mode AlGaN/GaN HFET.**

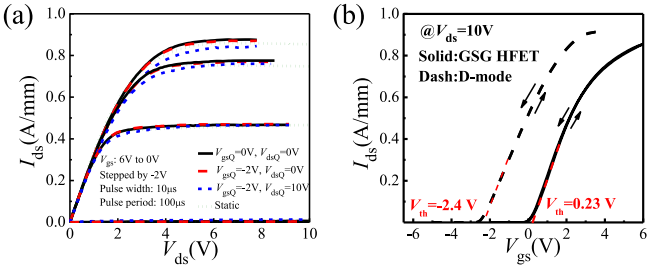

FIGURE 3. **(a) Static/pulsed output characteristics of GSG HFET, (b) double transfer characteristics of GSG HFET and D-mode AlGaN/GaN HFET.**

Fig. 1(a). A room-temperature electron mobility (μ) of around 2000 $cm^2/(V{\cdot}s)$ was achieved at a sheet concentration (n_s) of 0.9×10^{13} cm^{-2}. The device fabrication commenced with mesa isolation by Cl_2/BCl_3 plasma dry etching. The source/drain contacts with Ti/Al/Ni/Au (30/100/50/100 nm) were formed by electron-beam evaporation. An Ohmic resistance of 0.7 Ω·mm was obtained by a rapid thermal annealing at 860 °C in N_2 atmosphere. The distance between the source and drain Ohmic contacts was 5 μm. A 5 nm Al_2O_3 dielectric layer was deposited by atomic layer deposition (ALD) at 300 °C. Then post deposition annealing at 500 °C for 5 min under O_2 atmosphere was used to further improve the Al_2O_3 and Al_2O_3/GaN interface quality. Double Ni/Au (50/200 nm) gates with length/width of nominal 0.3/50 μm were located in the middle of the source-drain spacing and connected in one pad. The distance between the double gates (L_{gg}) was 80 nm, as shown in Fig. 2. A SiN passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The SiN located between the double gates was removed by reactive ion etching (RIE). The Al_2O_3 dielectric layer in region A between the double gates, as shown in Fig. 1(a), was removed by HF. Then the AlGaN barrier layer in region A was etched by ICP dry etching. To minimize the damage induced by ion bombardment, the RF bias and power were set very low to achieve an etch rate of ~1.5 nm/min. The RF generator power and ICP generator power were set to be 5 W and 180 W, respectively. Then the sample was annealed at 400 °C for 10 min under N_2 atmosphere. Besides, the D-mode AlGaN/GaN HFET without recess region was set as reference group, as shown in Fig. 1(b).

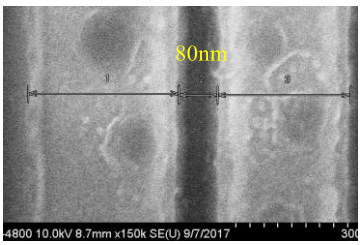

FIGURE 2. **Scanning Electron Microscope (SEM) cross-section image of the trench.**

III. RESULTS AND DISCUSSION

The measured static/pulsed output and double transfer characteristics of the fabricated GSG HFET with a 5-minutes etching time are shown in Fig. 3 (a) and (b), respectively. The device shows good pinch-off characteristics at zero gate bias. The gate lag can be negligible, and the total current collapse is about 5.6% from the pulsed measurements, as shown in Fig. 3(a). A value of V_{th} for GSG HFET is extracted to be 0.23 V. A high drain current density of 851 mA/mm @V_{gs} = 6 V is obtained. The double transfer characteristics of GSG HFET and D-mode device both exhibit almost no hysteresis, as shown in Fig. 3(b), indicating the good suppression of surface states. Moreover, compared to the D-mode device, the decrease of I_{dss} is just 7%.

Based on the commercial Sentaurus TCAD software, the two-dimensional simulations were performed to investigate the operating principle of GSG HFET. Following the work in [14], the surface donor traps with an energy level of 0.57 eV below the conduction band were taken. The dimension of the simulated device is same as the one in Fig. 1(a). Moreover, the I-V curves of the non-gate device with different etching time are shown in Fig. 4. The recess region here is defined as the whole area between source and drain. The drain current decreases sharply to 5.8×10^{-5} A/mm at 5-minutes etching time. Therefore, the low 2DEG density recess depth in the simulation is set from 8 nm.

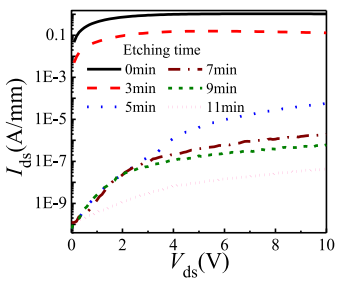

FIGURE 4. **I-V curves of the non-gate device with different etching time.**

In order to make the simulated data close to the measured data, the temperature-related model and source/drain parasitical resistances are added in the simulation. The simulated profile of lateral conduction band along channel is shown in Fig. 6(a). The barrier recess region is located from 2.3 to 2.38 μm. At zero gate bias, a barrier located in Region A is high enough to block the electron transition, realizing normally-off operation. With increasing the positive gate bias, the barrier height is pulled down. Besides, the block

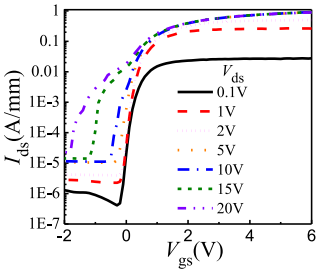

FIGURE 5. Subthreshold characteristics and DIBL effect of GSG HFET.

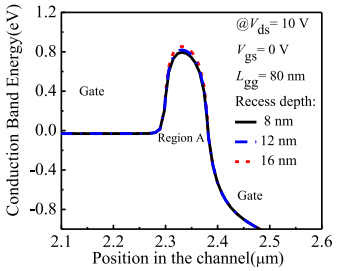

FIGURE 7. The simulated conduction band energy profiles along the channel under AlGaN/GaN heterojunction 1nm with different recess depth.

barrier becomes thinner and lower significantly with increasing drain voltage (from 0 V to 10 V as shown in Fig. 6(a)). Therefore, the drain induced barrier lower (DIBL) effect is remarkable, as shown in Fig. 5. The subthreshold slope (SS) is 125 mV/decade at V_{ds} = 1 V, while it increases to 214 and 401 mV/decade at V_{ds} = 10 and 20 V, respectively.

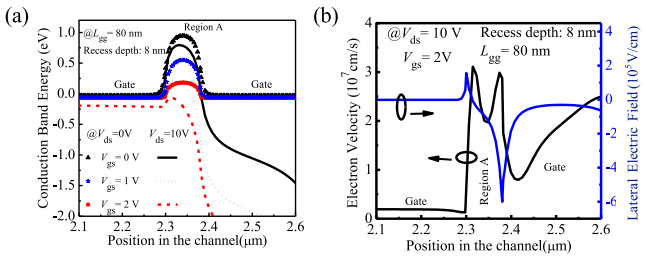

FIGURE 6. (a) Simulated lateral conduction band energy profiles along the channel under AlGaN/GaN heterojunction 1nm and (b) electron velocity and lateral electric field in Region A at V_{gs}=2V and V_{ds}=10V.

Compared to the conventional gate recess structure, the double gates enhance the regulation of the height and width in the block barrier at the same time. Moreover, the low-velocity electrons flowing from the source to the left of Region A will be sharply speeded up to through this region, as shown in Fig. 6(b). The left velocity peak in region A is caused by the abrupt 2DEG density, while the right electron velocity peak is caused by the high electric field [15], as shown in Fig. 6(b). As a result, the novel device can achieve high current after dry etching. It's also noteworthy that the block barrier height has little change with different recess depth from the simulated results, as shown in Fig. 7. This indicates that the threshold voltage is insensitive to the etching depth of AlGaN layer and will be constant in a wide range of dry etching time.

Transfer characteristics of GSG HFET with different etching time are shown in Fig. 8. The simulated data is for obtaining changing trends. As shown in Fig. 8 (a), the simulated results point out that I_{ds} (from 990 to 952 mA/mm), peak transconductance (from 193 to 178 mS/mm) and V_{th} (from 0.47 to 0.49 V) are insensitive to the recess depth, even in large range from 8 nm to 16 nm. The trend of experimental results agrees very well with the simulated data, as shown in Fig. 8 (b). The saturation drain current, transconductance and threshold voltage almost have no change as the

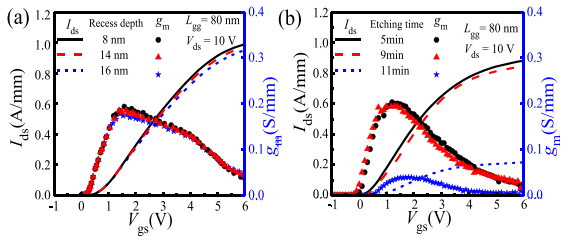

FIGURE 8. Transfer characteristics of GSG HFET with different etching time (a) simulated data, (b) measured data.

etching time increasing from 5 to 9 minutes. However, the drain current drops obviously with further increasing etching time to 11 minutes, as shown in Fig. 8 (b). This may be due to the barrier thickness fluctuation scattering [16], or surface defects scattering [17], or the damage of the channel, which are not given full consideration in the simulation.

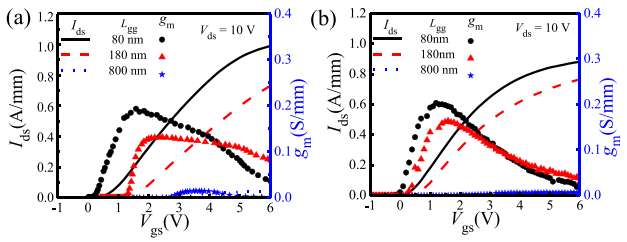

FIGURE 9. Transfer characteristics of GSG HFET with different L_{gg} (a) simulated data, (b) measured data.

Transfer characteristics of GSG HFET with different gate-to-gate distance (L_{gg}) are shown in Fig. 9. The trend of experimental data matches well with the simulated transfer characteristics of GSG HFET with different L_{gg}. With increasing the gate-to-gate distance, the threshold voltage rises obviously towards to positive direction, which can reach 3.1V at L_{gg} = 800 nm. However, the drain current density decreases significantly, caused by the decreasing electric filed and electron velocity in the region A. Further studies focused on material structure, gate length and insulation type are still needed to increase the threshold voltage while maintaining a high drain current.

IV. CONCLUSION

A novel E-mode AlGaN/GaN gates-seperating groove heterostructure field-effect transistor (GSG HFET) was fabricated. The block barrier located between the double gates was realized by ICP etching. Although the electrons density in the barrier region is low, the electron velocity in this region is high enough to keep a high drain current, which achieved 851 mA/mm. Meanwhile, the threshold voltage is less insensitive to the etching time, improving the threshold voltage consistency under uncontrollable etch rate. Due to the advantages of high current density and the high threshold voltage consistency, the novel structure may realize practical application in the foreseeable future.

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