

In-Ga-Zn-O Thin-Film Devices As Synapse Elements in a Neural Network

MUTSUMI KIMURA^{1,2} (Senior Member, IEEE), YUKI KOGA², HIROKI NAKANISHI², TOKIYOSHI MATSUDA² (Member, IEEE), TOMOYA KAMEDA¹, AND YASUHIKO NAKASHIMA¹ (Member, IEEE)

¹ Graduate School of Information Science, Nara Institute of Science and Technology, Ikoma 630-0192, Japan
² Department of Electronics and Informatics, Ryukoku University, Seta, Otsu 520-2194, Japan

CORRESPONDING AUTHOR: M. KIMURA (e-mail: mutsu@rins.ryukoku.ac.jp)

This work was supported in part by KAKENHI under Grant 16K06733, in part by the Yazaki Memorial Foundation for Science and Technology, in part by the Support Center for Advanced Telecommunications Technology Research, in part by the Research Grants in the Natural Sciences from the Mitsubishi Foundation, in part by the Collaborative Research with ROHM Semiconductor, in part by the Collaborative Research with KOA Corporation, and in part by the Laboratory for Materials and Structures in Tokyo Institute of Technology.

ABSTRACT We have succeeded in utilizing In-Ga-Zn-O (IGZO) thin-film devices as synapse elements in a neural network. The electrical conductance is regarded as the connection strength, and the continuous change by flowing electrical current is employed as the connection plasticity based on the modified Hebbian learning as a learning rule. We developed a cellular neural network using the IGZO thin-film devices and confirmed that the neural network can learn simple logic functions. These results suggest a possibility to realize 3-D layered structure for brain-type integrated systems.

INDEX TERMS In-Ga-Zn-O (IGZO), thin-film device, synapse element, neural network, conductance change, modified Hebbian learning.

I. INTRODUCTION

Artificial intelligences are thinking machines that mimic biological brains, and neural networks are promising as key technologies in future societies with many advantages, such as self-organization, self-teaching, parallel distributed computing, fault tolerance, etc [1]–[5]. These advantages are obtained by connecting a large number of neuron elements with a much larger number of synapse elements to imitate human brains, where more than 10^{11} neuron elements and 10^{15} synapse elements exist. However, because the conventional ones are complicated software executed on high-spec hardware, the machine size is very bulky and power consumption is unbelievably huge. Moreover, some of the aforementioned advantages, such as parallel distributed computing and fault tolerance, are not acquired, because they are executed on conventional Neumann-type computers, which sequentially handle processes and stop only if a physical device is broken. Furthermore, the computing architecture is not optimized for the artificial intelligence and therefore extra circuits occupy a large area and consume large power.

Therefore, some researchers are investigating neural networks built by real hardware instead of virtual software,

which can be compact, low power, and robust [6]–[12]. We named them “brain-type integrated system”, which can be integrated on everything in future life [13]–[19]. In order to realize such system, it is necessary to simplify the processing elements, such as neuron elements and synapse elements, and network architecture, because more elements can be integrated in a certain area of the network. Moreover, it is also necessary to produce three-dimensional structure and fabricate at low cost. We have already succeeded in simplifying the neuron elements.

Particularly in this study, we tried to simplify the synapse elements from the conventional ones [20] and utilize In-Ga-Zn-O (IGZO) thin-film devices as synapse elements in a neural network. IGZO thin-film transistors (TFTs) are promising for present and potential applications of flat-panel displays (FPDs) [21]–[25], and IGZO thin-film devices have been reported as synapse elements with a different architecture of a neural network such as spiking neuron without developing real system in a prior paper [26], [27]. On the other hand, we developed a cellular neural network using the IGZO thin-film devices and confirmed that the neural network can learn simple logic functions. In comparison with the late presentation from [28], particularly in this report, we

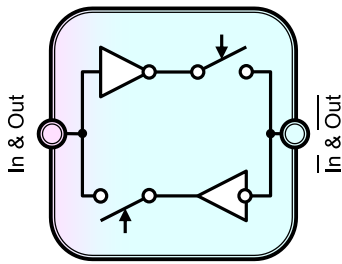


FIGURE 1. Neuron element.

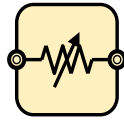


FIGURE 2. Synapse element.

confirmed that the neural network can learn multiple functions, which is very important because it indicates flexibility of the neural network. Because the IGZO thin-film devices can be fabricated at low temperature and low cost using simple methods, such as sputtering methods and printing methods [29], [30], once the practical working is confirmed, three-dimensional layered structure for brain-type integrated systems will be realized in the future.

II. SYSTEM ARCHITECTURE

The neuron element is shown in Fig. 1. It is simplified to a circuit where two inverters and two analog switches are circularly connected. It has the requisite minimum functions obtained by the deep consideration on the theoretical working of the neuron elements. The requisite functions are: (1) to generate and maintain a binary state called the fire and steady states and (2) to alternate the binary state according to the input signal. When the analog switches are on, the In & Out terminal is high voltage (H), whereas the $\overline{\text{In}}$ & $\overline{\text{Out}}$ terminal is low voltage (L), which corresponds to the fire state. Otherwise, the In & Out terminal is L, whereas the $\overline{\text{In}}$ & $\overline{\text{Out}}$ terminal is H, which corresponds to the steady state. Then the neuron circuit maintains these binary states. On the other hand, when the analog switches are off, the neuron circuit alternates the binary state according to the input signal from the In & Out and $\overline{\text{In}}$ & $\overline{\text{Out}}$ terminals [13]–[19].

The synapse element is shown in Fig. 2. It is simplified to a variable conductor. It also has the requisite minimum functions of the synapse elements. The requisite functions are: (1) to merge the state signals from multiple neuron elements and transfer the state signal to a neuron element to alternate the binary state following the majority rule and (2) to control the connection strength, namely, how the state signal is effectively transferred. It has been guaranteed that the continuous decrease of the electrical conductance by flowing electrical current can be employed as the connection plasticity based on the modified Hebbian learning as a learning rule [13]–[19].

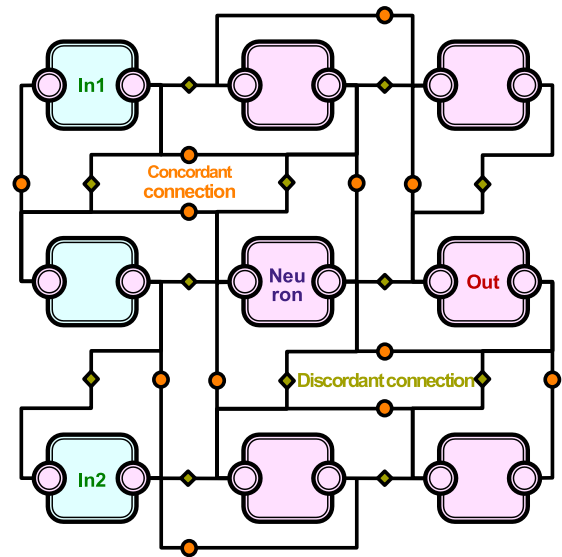


FIGURE 3. Neural network.

The neural network is shown in Fig. 3. It is a cellular neural network where each neuron element is connected to only the neighboring neurons, such as, the upper, lower, right, and left neuron elements. It is suitable for the integration of electron devices in the future, because there is no long connection. The synapse connections are classified to concordant connections and discordant connections by the connecting points. The concordant connections are indicated by orange circles, whereas the discordant connections are indicated by yellow lozenges, as shown in Fig. 3. Namely, the concordant connections connect two In & Out terminals or two $\overline{\text{In}}$ & $\overline{\text{Out}}$ terminals, whereas the discordant connections connect an In & Out terminal and an $\overline{\text{In}}$ & $\overline{\text{Out}}$ terminal. As a result, the concordant connections tend to make the binary states of the connected neurons the same, whereas the discordant connections tend to make the neuron states different.

Modified Hebbian learning is employed as a learning rule where the electrical conductance of the synapse element continuously decreases when the electric current flows [13]–[19]. It is also suitable for the integration of electron devices, because no additional circuits are needed for the learning. It should be noted that potentiation and depression functions are necessary for connection strength of synapse elements in the conventional theory of neural networks. On the contrary, the technical combination of the concordant and discordant connections play the same role of the potentiation and depression functions, even if the conductance decrease only occurs. Namely, the conductance decrease in the discordant connection has the same effect of the potentiation function in the concordant connection, as shown in Fig. 4. It should also be noted that no additional control is needed and only local phenomenon is used for the conductance decrease owing to the revised architecture of the neural network, which is similar to biological brains and

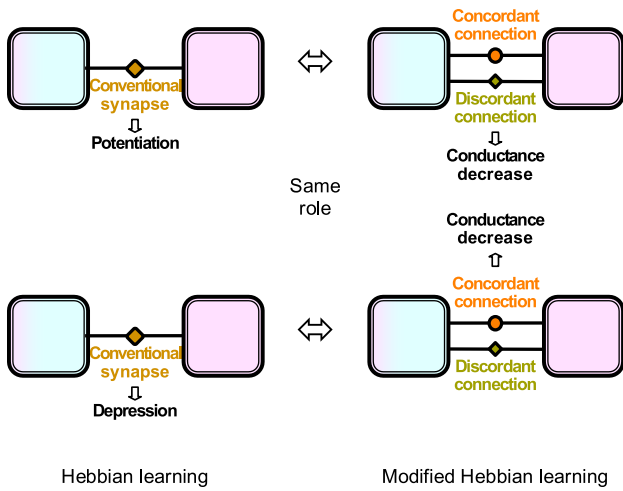


FIGURE 4. Modified Hebbian learning.

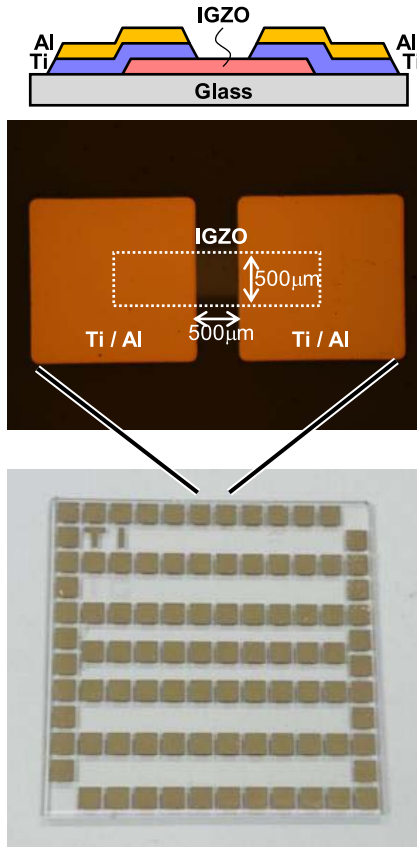


FIGURE 5. In-Ga-Zn-O thin-film device.

also suitable for the integration of electron devices because no additional circuits are needed.

III. IN-GA-ZN-O THIN-FILM DEVICE

IGZO thin-film devices are shown in Fig. 5. First, a quartz glass substrate was used. The thickness is 1 mm, and the size is 3 cm × 3 cm. Next, an IGZO thin film was deposited using radio-frequency (RF) magnetron sputtering.

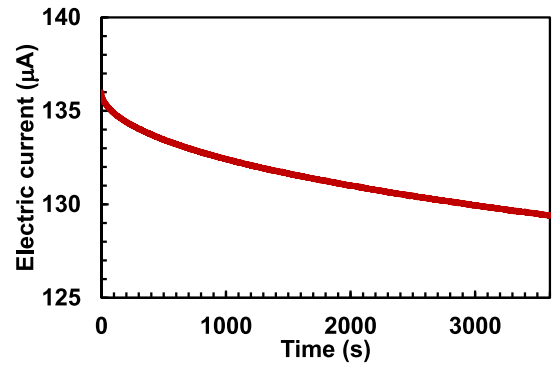


FIGURE 6. Electrical current through the In-Ga-Zn-O thin-film device.

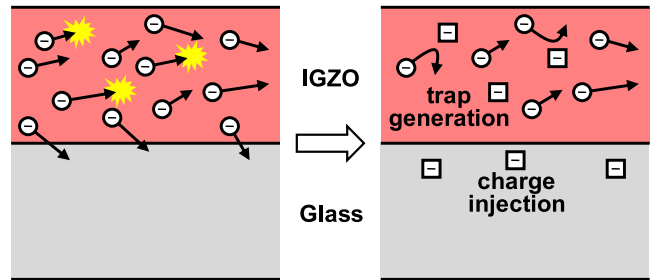


FIGURE 7. Mechanisms for the conductance decrease.

The sputtering target is an IGZO ceramic whose composition is In:Ga:Zn=1:1:1, and the sputtering gas is Ar. The IGZO thin film was patterned through a metal mask as shown by the dotted line in Fig. 5. The thickness of the IGZO thin film is 70nm. These fabrication conditions are the same as those for the thin-film transistors having the best performance. Finally, Ti and Au were sequentially deposited using vacuum evaporation. Ti and Au were also patterned through a metal mask as shown in Fig. 5. The thicknesses of Ti and Au are 50nm each. Ti is used to obtain ohmic contact to the IGZO thin film because it has a proper work function and improve adherence, and Au is used to avoid the surface oxidation and make probing easy. No additional annealing was executed.

The electrical current through the IGZO thin-film device is shown in Fig. 6. Here, we applied 3.3V between the two terminals of the Ti and Au and measured the electrical current through the IGZO thin-film device. It was found that the electrical conductance continuously decrease when the electric current flows. The conductance decrease is irreversible. The modified Hebbian learning can be employed using this phenomenon. As shown in Fig. 6, the conductance decrease is not so fast. However, because the operation of the neural network is based on the delicate balance of the majority rule, the slow change is sometimes convenient also to avoid the excess learning.

The mechanisms for the conductance decrease are shown in Fig. 7. It is supposed that this phenomenon is caused by either the generation of trap states in the IGZO thin film or injection of the electric charge into the interface between

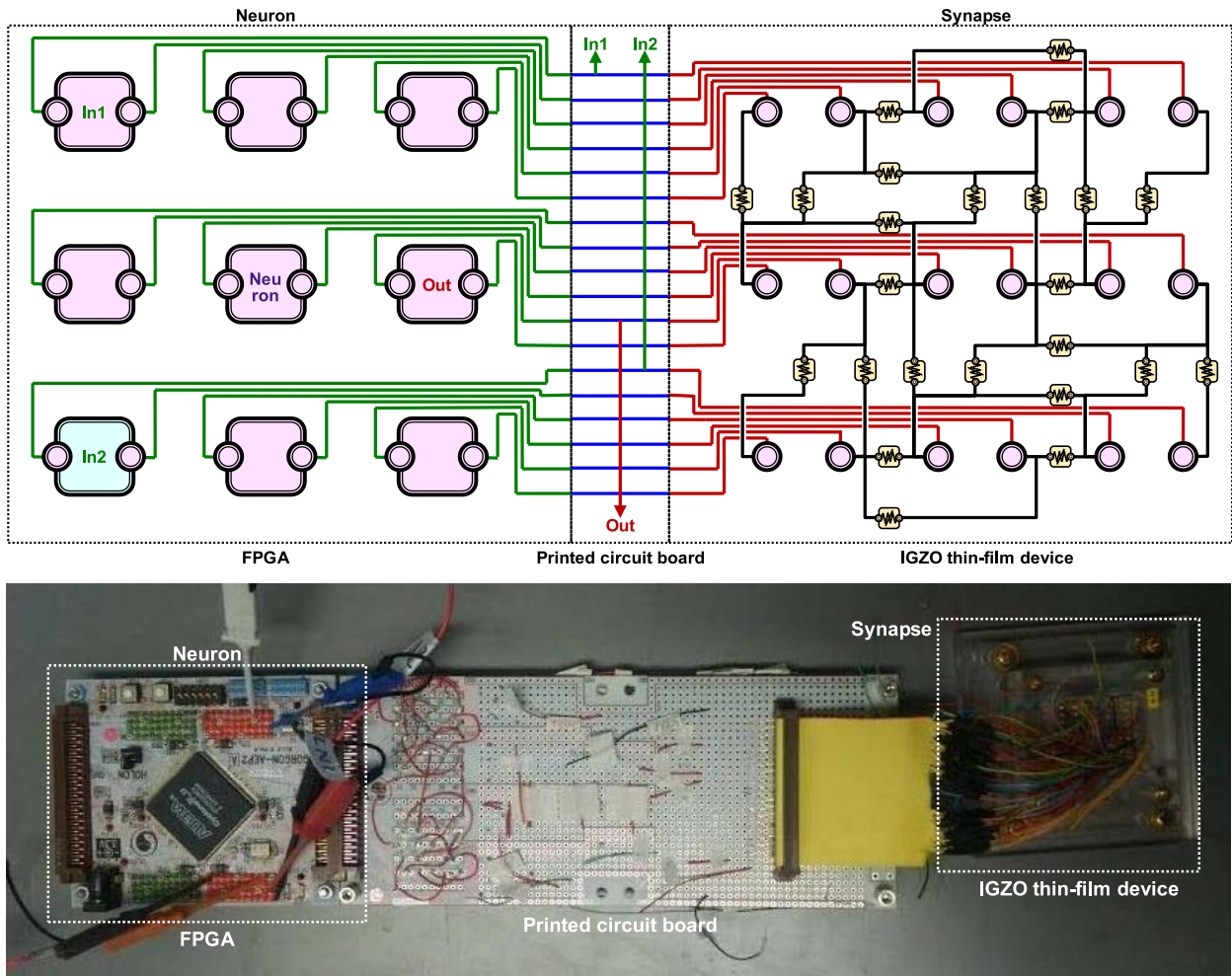


FIGURE 8. Experimental system for the logic learning.

the IGZO thin film and quartz glass substrate. In the case of the generation of trap states, first, free electrons are accelerated and collide to the IGZO crystal. Next, trap states are generated and capture free electrons. Finally, free electrons decrease because of the fixed charge in the trap states and are simultaneously scattered by them, which induces the conductance decrease. On the other hand, in the case of the injection of the electric charge, first, free electrons are again accelerated near the interface and are casually injected into the interface between the IGZO thin film and quartz glass substrate. Next, the free electrons are captured at the interface. Finally, free electrons decrease because of the fixed charge of the injected electrons, which also induces the conductance decrease.

The IGZO thin-film device is a kind of memristor, because the definition of the memristor is that the electric current changes by flowing electric charges. However, in comparison with the conventional memristors used as resistive memories [31], the IGZO thin-film device shows a continuous change of the electric conductance, which is preferable for our neural network. Moreover, it does not need high

temperature for fabrication process and can be potentially formed using printing methods. Furthermore, in comparison with the conventional floating-gate transistors [32], [33], the device structure is quite simple, which is convenient to realize a three-dimensional layered structure for brain-type integrated systems.

IV. LOGIC LEARNING

The experimental system for the logic learning is shown in Fig. 8. Here, a circuit diagram and actual photograph are shown. The neuron elements were formed in a field programmable gate array (FPGA). Here, we used Cyclone II FPGA supplied from Altera and designed it using hardware description language (HDL) [34]. The neuron elements can be easily formed because they are general digital circuits as shown in Fig. 1. Nine neuron elements are formed because we believe that this is the minimum number for the simple logic learning and it is also important to evaluate how small neural network can get the required functions. The synapse elements using the IGZO thin-film devices are properly connected through a printed circuit board. The round points in

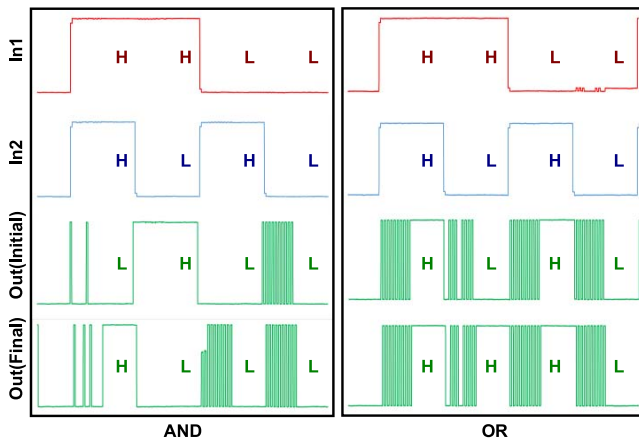


FIGURE 9. Experimental results of the logic learning.

the synapse substrate are just connecting terminals connected to In & Out terminals and \bar{In} & \bar{Out} terminals of the neuron elements. As a result, the exactly same neural network as that shown in Fig. 3 is reproduced in the experimental system. Here, we taught simple logic function, such as AND and OR. First, we assigned In1, In2, and Out as shown in Fig. 3. As a result, a neuron element exists between In1, In2, and Out each, which is a reason why nine is the minimum number of the neuron elements because all input and output signals can be affected by the neuron elements and synaptic connections. Next, we applied combinations of H (3.3V) and L (GND) to In1 and In2 and corresponding voltage to Out. As a result, the continuous change of the electric conductance occurs in each IGZO thin-film device. Finally, we applied the combinations of the voltages to only In1 and In2 and checked the voltage at Out.

The experimental results of the logic learning is shown in Fig. 9. Because the fine pulses are noises from the switching signals to the analog switches, ignore them. It was found that although Out is initially not correct before the learning, Out becomes finally correct after the learning for both AND and OR. A problem is that it takes as long as one hour for the learning. We expect that this problem can be solved by optimizing the electrical characteristic of the IGZO thin-film devices and speeding up the conductance decrease. In any case, we confirmed that the neural network can learn simple logic functions.

V. CONCLUSION

We have succeeded in utilizing IGZO thin-film devices as synapse elements in a neural network. The electrical conductance is regarded as the connection strength, and the continuous change by flowing electrical current is employed as the connection plasticity based on the modified Hebbian learning as a learning rule. We developed a cellular neural network using the IGZO thin-film devices and confirmed that the neural network can learn simple logic functions.

Although it currently takes long time for the learning, we expect that this problem can be solved by optimizing the electrical characteristic of the IGZO thin-film devices and speeding up the conductance decrease. As for the power consumption, although the current system is not satisfactory, it can be improved by decreasing the absolute value of the electric current through the IGZO thin-film devices by optimizing film quality and pattern dimension.

Although these results are fundamental, once the neural network can learn the simple functions, it can be expected that the neural network gets more complicated functions. If we scale up the neural network, we should integrate the neuron and synapse elements on an integrated chip, which does not seem difficult using current technologies. Therefore, we believe that the obtained results in this paper suggest a possibility to realize three-dimensional layered structure for brain-type integrated systems in the future.

REFERENCES

- [1] J. E. Dayhoff, *Neural Network Architectures: An Introduction*. New York, NY, USA: Van Nostrand Reinhold, 1990.
- [2] R. Hecht-Nielsen, *Neurocomputing*. Reading, MA, USA: Addison-Wesley, 1990.
- [3] S. Becker and G. E. Hinton, "Self-organizing neural network that discovers surfaces in random-dot stereograms," *Nature*, vol. 355, pp. 161–163, Jan. 1992.
- [4] J. V. Stone, N. M. Hunkin, and A. Hornby, "Neural-network models: Predicting spontaneous recovery of memory," *Nature*, vol. 414, pp. 167–168, Nov. 2001.
- [5] I. Goodfellow, Y. Bengio, and A. Courville, *Deep Learning*. Cambridge, MA, USA: MIT Press, 2016.
- [6] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA, USA: Addison-Wesley, 1989.
- [7] Y. Arima *et al.*, "A 336-neuron, 28 K-synapse, self-learning neural network chip with branch-neuron-unit architecture," *IEEE J. Solid-State Circuits*, vol. 26, no. 11, pp. 1637–1644, Nov. 1991.
- [8] M. Yasunaga *et al.*, "A self-learning digital neural network using wafer-scale LSI," *IEEE J. Solid-State Circuits*, vol. 28, no. 2, pp. 106–114, Feb. 1993.
- [9] T. Morie and Y. Amemiya, "An all-analog expandable neural network LSI with on-chip backpropagation learning," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1086–1093, Sep. 1994.
- [10] B. Widrow, W. H. Pierce, and J. B. Angell, "Birth, life, and death in microelectronic systems," *IRE Trans. Mil. Electron.*, vol. MIL-5, no. 3, pp. 191–201, Jul. 1961.
- [11] G. S. Snider, "Cortical computing with memristive nanodevices," *SciDAC Rev.*, vol. 10, pp. 58–65, 2008.
- [12] S. K. Essera *et al.*, "Convolutional networks for fast, energy-efficient neuromorphic computing," *Proc. Nat. Acad. Sci. USA*, vol. 113, no. 41, pp. 11441–11446, 2016.
- [13] T. Kasakawa *et al.*, "An artificial neural network at device level using simplified architecture and thin-film transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2744–2750, Oct. 2010.
- [14] M. Kimura, T. Miyatani, Y. Fujita, and T. Kasakawa, "Apoptotic self-organized electronic device using thin-film transistors for artificial neural networks with unsupervised learning functions," *Jpn. J. Appl. Phys.*, vol. 54, Feb. 2015, Art. no. 03CB02.
- [15] M. Kimura, Y. Fujita, T. Kasakawa, and T. Matsuda, "Novel architecture for cellular neural network suitable for high-density integration of electron devices—Learning of multiple logics," in *Proc. ICONIP*, 2015, pp. 12–20.
- [16] M. Kimura *et al.*, "Simplified architecture for cellular neural network suitable for high-density integration of electron devices," in *Proc. NOLTA*, Hong Kong, 2015, pp. 499–502.
- [17] M. Kimura *et al.*, "Simplification of processing elements in cellular neural networks—Working confirmation using circuit simulation," in *Proc. ICONIP*, Kyoto, Japan, 2016, pp. 309–317.

- [18] M. Kimura *et al.*, "Letter reproduction using a cellular neural network consisting of simplified neurons and synapses fabricated by thin-film transistors," in *Proc. NOLTA*, 2016, pp. 36–39.
- [19] M. Kimura *et al.*, "Cellular neural network formed by simplified processing elements composed of thin-film transistors," *Neurocomputing*, vol. 248, pp. 112–119, Jul. 2017.
- [20] M. Tanaka and T. Saito, *Neural Nets and Circuits*. Tokyo, Japan: Corona, 1994.
- [21] *IGZO Technology*. Accessed: Nov. 29, 2017. [Online]. Available: <http://www.sharp.co.jp/igzo/concept.html>
- [22] *LG OLED TV*. Accessed: Nov. 29, 2017. [Online]. Available: http://www.lg.com/jp/oled_tv/main.html
- [23] *TV VIERA*. Accessed: Nov. 29, 2017. [Online]. Available: <http://panasonic.jp/viera/products/ez1000.html>
- [24] M. Kimura and S. Imai, "Degradation evaluation of TFTs for application to AM-OLEDs," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 963–965, Sep. 2010.
- [25] H. Yamaguchi *et al.*, "11.7-inch flexible AMOLED display driven by a-IGZO TFTs on plastic substrate," in *Proc. Display Week*, 2012, pp. 1002–1005.
- [26] J. Zhou, N. Liu, L. Zhu, Y. Shi, and Q. Wan, "Energy-efficient artificial synapses based on flexible IGZO electric-double-layer transistors," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 198–200, Feb. 2015.
- [27] M. Dai *et al.*, "Realization of tunable artificial synapse and memory based on amorphous oxide semiconductor transistor," *Sci. Rep.*, vol. 7, Sep. 2017, Art. no. 10997.
- [28] Y. Koga, T. Matsuda, and M. Kimura, "Neural network using FPGA for neurons and IGZO thin films for synapses," in *Proc. AMFPD*, Kyoto, Japan, 2016, pp. 179–180.
- [29] K. Nomura *et al.*, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488–492, Nov. 2004.
- [30] J. F. Wager, "Transparent electronics," *Science*, vol. 23, no. 5623, pp. 1245–1246, 2003.
- [31] M. Prezioso *et al.*, "Training and operation of an integrated neuro-morphic network based on metal-oxide memristors," *Nature*, vol. 521, pp. 61–64, May 2015.
- [32] D. Kahng and S. M. Sze, "A floating gate and its application to memory devices," *Bell Syst. Tech. J.*, vol. 46, no. 6, pp. 1288–1295, Jul./Aug. 1967.
- [33] T. Hanyu, K. Teranihi, and M. Kameyama, "Multiple-valued floating-gate-MOS pass logic and its application to logic-in-memory VLSI," in *Proc. ISMVL*, Fukuoka, Japan, 1998, pp. 270–275.
- [34] *Cyclone II*. Accessed: Nov. 29, 2017. [Online]. Available: <https://www.altera.co.jp/products/fpga/cyclone-series/cyclone-ii/overview.html>



MUTSUMI KIMURA (M'10–SM'11) received the B.E. and M.E. degrees in physical engineering from Kyoto University in 1989 and 1991, respectively, and the Ph.D. degree in electrical and electronic engineering from the Tokyo University of Agriculture and Technology in 2001. He is currently pursuing the graduation degree with the Nara Institute of Science and Technology. He joined Matsushita Electric Industrial Company, Ltd., in 1991 and Seiko Epson Corporation in 1995. He is currently a Professor with Ryukoku University. His research interests are brain-type integrated systems, neural networks, and thin-film device applications.



YUKI KOGA received the B.E. and M.E. degrees in electronics and informatics from Ryukoku University in 2015 and 2017, respectively. His research interests were neural networks and thin-film device applications.



HIROKI NAKANISHI received the B.E. degree in electronics and informatics from Ryukoku University in 2016. His research interests were neural networks and thin-film device applications.



TOKIYOSHI MATSUDA received the B.S. degree in physics and the M.E. and Ph.D. degrees in earth and space science from Osaka University in 1997, 2000, and 2003, respectively. He joined the Kochi University of Technology in 2004 and Ryukoku University in 2011. He is currently a Guest Researcher with Ryukoku University. His research interests are oxide-semiconductor materials, thin-film process and devices, and characteristic evaluations.



TOMOYA KAMEDA received the B.S. degree in electrical and electronic systems engineering from the Osaka Institute of Technology in 2015 and the M.E. degree in information science from the Nara Institute of Science and Technology in 2017. His research interests were computing architecture, neural networks, and operation simulation.



YASUHIKO NAKASHIMA received the B.E., M.E., and Ph.D. degrees in information engineering from Kyoto University in 1986, 1988, and 1998, respectively. He joined Fujitsu Ltd., in 1988. He is currently a Professor with the Nara Institute of Science and Technology. His research interests are computing architecture, machine learning, and Internet of Things.