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Performance and Power Consumption Trade-Off in UTBB FDSOI Inverters Operated at NTV for IoT Applications

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ABSTRACT Power consumption and I_{on}/I_{off} ratio of an ultra-thin body and buried oxide fully depleted silicon on insulator CMOS inverter circuit has been calculated at near-threshold voltage operation from TCAD simulations. TCAD outputs (current, voltage, and capacitance) were used as parameters to solve the inverter circuit. Besides, a bias operation point (V_{OP}) has been proposed, which provides a good trade-off between the I_{on}/I_{off} ratio and the energy consumption. Variations of this operation point, due to the presence of interface traps, have been also analyzed.

INDEX TERMS Near-threshold voltage, power consumption, CMOS inverter, TCAD, IoT, UTBB FDSOI.

I. INTRODUCTION

The exponential increase of the number of transistors packed on chips and the stagnant of supply voltages (V_{DD}) is leading to a dramatic increase of the power density and energy consumption of the chips [1]. Moreover, Internet of Things (IoT) is changing the way of obtaining information from our environment (remote sensors) or even about ourselves ("wearables" or implantable devices). Devices used with this purpose have two common characteristics; they do not need to show a high performance but the energy consumption must be as low as possible. Therefore, the development of low-power technology is becoming one of the major design challenges [2].

In order to overcome this bottleneck, two solutions have been mainly reported in literature. On the one hand, ultra-thin body and buried oxide (BOX) fully depleted silicon on insulator (UTBB FD-SOI) technology could be a promising candidate to improve the power consumption, by adjusting the threshold voltage (V_{TH}) by applying body biasing voltage (V_{BB}) [3], [4]. On the other hand, devices operating in near-threshold voltage (NTV) improve the energy efficiency (10X or higher) at the cost of performance [5], [6]. Therefore, the study of energy consumption of logic gates composed by UTBB-FD-SOI devices, operating in NTV, could help to design a new generation of circuits [1].

Nevertheless, when circuits operate at NTV, not only their performance is reduced, but also their functional failures increase [7]. Variability sources such as random dopant fluctuation (RDF) or trapped charge in the gate or buried oxide can lead to functional failure or timing failure [7]. Therefore, an exhaustive study of energy consumption of circuits and the effects of such variability sources must be considered.

In this paper, the static and dynamic energy consumption of an inverter logic gate based on UTBB-FD-SOI devices operating in NTV are calculated from TCAD data. The TCAD tool used was ATLAS Silvaco [8]. Two structural parameters of the device, i.e., channel thickness (T_{SI}) and BOX thickness (T_{BOX}), and one operation parameter (V_{BB}), were considered to optimize the energy consumption of the inverter gate. These results could be assumed as a reference to be extended to more complex circuits. Finally, the impact of trapped charges in the gate oxide and BOX on energy consumption and operation frequency of the inverter gate was studied.

II. DEVICE SIMULATION

UTBB FD SOI 28 nm devices were considered to study the energy consumption in an inverter circuit from TCAD simulations using ATLAS Silvaco. The structure and doping data of devices were obtained from [3], [9], and [10] where different simulations and experimental results are presented

for UTBB FD SOI technology. Similar V_{BB} values to those reported in [9] and [11] were considered. Table 1 shows a summary of the dimensions and doping taken into account in this work for a n-type device. By assuming CMOS balanced circuits [4], [12], the p-type device was considered to have the same electric behavior (i.e., same currents and capacitances for the same applied voltages) than the n-type transistor and therefore it was not needed to be simulated in TCAD. Fig. 1 shows the 3D simulated structure, the net doping level in the channel and the metallization contacts for n-type device.

TABLE 1. Parameters considered in the simulations.

Parameter	Value
Oxide thickness (T_G)	1.5 nm (EOT)
Channel thickness (T_{SI})	(10 – 25) nm
Oxide thickness BOX (T_{BOX})	(10 – 25) nm
Substrate thickness (T_{SUB})	60 nm
Gate length (L_G)	28 nm
Substrate doping (S_{DOP})	10^{16} cm^{-3}
Channel doping (C_{DOP})	$3{\cdot}10^{18}$ cm^{-3}
Width (W)	100 nm
Back Biasing voltage ($\|V_{BB}\|$)	(0 – 4) V

For the simulations, a non-regular mesh was considered in the structure in order to have a resolution less than 1 nm under the gate in the Y-axis and $(1-2)$ nm in the X-axis and Z-axis. Thus, the electric potential can be accurately calculated, to study the impact of one trap on the device performance. Besides, a refined meshing in the channel was done proportional to the gradient of the doping profile.

Once the structure was defined, the models needed to simulate the device were chosen considering the next assumptions. The gate length is in the sub-100 nm regime and the FDSOI design is subjected to non-local effects such as velocity overshoot, diffusion associated with carrier temperature gradients and the dependence of impact ionization rates on carrier energy distributions [13], [14]. To this respect, the energy balance transport model, which adds the temperature as extra parameter in the transport of carriers, is used over the conventional drift-diffusion model, although the convergence and speed of simulation are slightly lower. Besides, in the ultra-thin channel, significance of quantum confinement of carrier becomes conspicuous, therefore the quantum effects must be taken into account. They are introduced using density gradient quantum correction [15]. Regarding the impact ionization, the Selberherr's model is assumed, because it includes temperature dependent parameters [16]. Finally, Fermi Dirac statistics and Shockley-Real-Hall (SRH) recombination are also considered in all simulations.

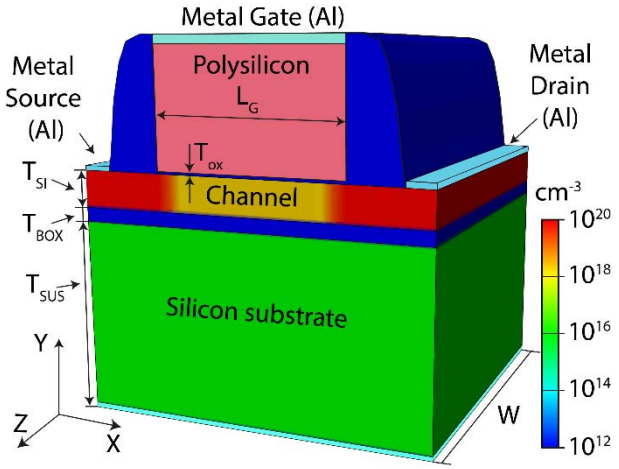

FIGURE 1. 3D TCAD structure of the simulated device showing the doping profile (not at scale).

Fig. 2a shows different I_DV_G curves for a nMOS device (T_{SI} =15 nm, T_{BOX} = 15 nm and V_{DS} = 0.1 V), for several V_{BB} from 0 to −4 V. Current values obtained are compatible with other works [17], [18], where devices of the same technology are studied. As it can be seen, when the $|V_{BB}|$ increases, I_DV_G curves show less current through the device modifying the V_{TH}.

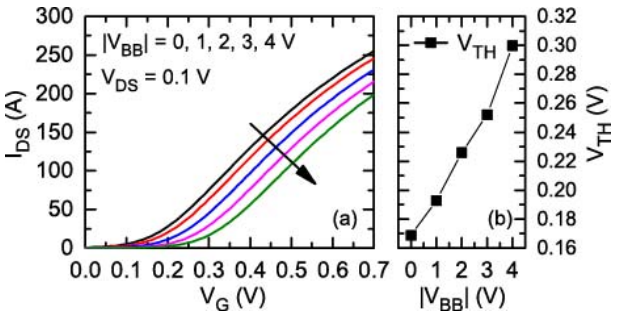

FIGURE 2. (a) I_DV_G curves simulated for several $|V_{BB}|$ for a nMOS device (T_{SI} = 15 nm, T_{BOX} = 15 nm and V_{DS} = 0.1 V). (b) The V_{TH} obtained from I_DV_G curves, as a function of $|V_{BB}|$.

Fig. 2b shows the V_{TH} variation as a function of V_{BB} where a linear relationship is found. Notice that the V_{TH} values range between 0.1 to 0.3 V, for the considered V_{BB}. The V_{TH} was calculated from I_DV_G curves applying the extrapolation in the linear region method [19]. Similar correlations of V_{BB} with V_{TH} were reported in [10].

III. SIMULATION RESULTS

To determine the energy consumption, two power dissipation mechanisms in an CMOS logic gate must be taken into account: the static power consumption (P_S), which is the result of the leakage current through the contacts of the devices in the circuit for the two logical states, and the dynamic power consumption (P_D), which is calculated by considering a capacitive load that is charged and discharged when the logic gate is switching. To evaluate this power

consumption, a circuit simulator such as SPICE can be used, considering a compact model to describe the electrical behavior of devices [11]. However, in this work, instead of a compact model, a TCAD simulator is used to evaluate the leakage currents at all contacts and the parasitic capacitances required to calculate the power consumption.

The key advantages of using TCAD simulation instead of compact models are that all device parameters can be changed easily, what allows parametric studies, and the parameters introduced in TCAD have a physical meaning. For instance, variability sources such as bias temperature instabilities (BTI) or random telegraph noise (RTN) can be introduced in the simulation, changing the physical parameters (trap parameters) which describe these phenomena [20]. As main drawback, the TCAD simulations consume more computational resources than compact models and therefore complex circuits cannot be easily simulated.

A. STATIC ENERGY CONSUMPTION

The static power consumption is a function of supply voltage (V_{DD}) and leakage current ($I_{leakage}$) flowing through the devices. In this work, the gate current and the drain–source current are considered as main contributions to the leakage current. Other leakage current contributions, such as bulk leakage current, are neglected, because the applied voltages are close to the threshold voltage. Actually, depending mainly on the gate oxide thickness and the applied voltages, the gate leakage current could be also neglected.

TABLE 2. nMOS voltages applied in TCAD simulations and corresponding voltages of the equivalent pMOS in an inverter.

Bias (V)	nMOS (on/off)	pMOS (on/off)
V_{gate_source}	V_{DD} / 0	V_{DD} / 0
V_{drain_source}	V_{OUT}	V_{DD} - V_{OUT}
V_{bulk_source}	-BB	-BB
V_{source}	0	0

Fig. 3a shows the $I_{leakage}$ simulated for the n-type device as a function of output voltage of the inverter (V_{OUT}), for different V_{DD}. These curves were estimated when the output of the logic gate was logic '0', i.e., the nMOS device was ON and pMOS OFF. Notice that pMOS device was considered electrically equivalent to the nMOS and therefore it was not simulated, saving computational time. The pMOS curves were derived from those of the nMOS, taking into account the voltages at device terminals when included in a CMOS inverter, which are shown in Table 2.

From the circuit analysis, (Fig 3.b) the crossing points of the curves in Fig 3.a represent the circuit solution where the $I_{leakage}$ flowing through both transistors is the same, for V_{OUT}. Note that in the case of evaluating the configuration of a logic "1", the voltages applied to devices would change, being nMOS in the OFF state and pMOS in the ON state.

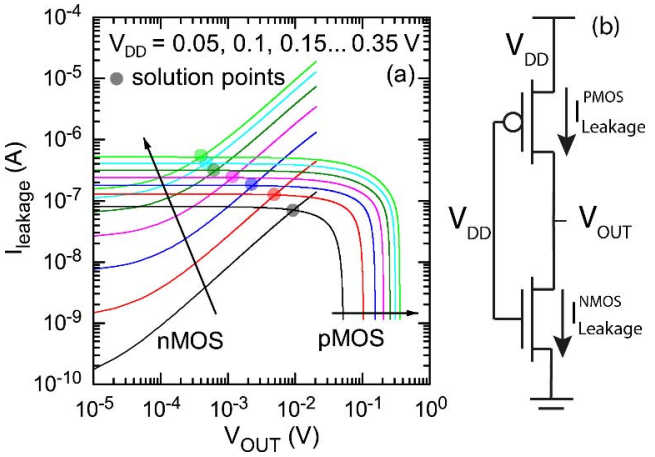

FIGURE 3. (a) $I_{leakage}$ as a function of V_{out} for different V_{DD} in an inverter logic gate. (b) Scheme of the inverter gate, highlighting $I_{leakage}$ for each transistor and V_{out}. The crossing points for the nMOS and pMOS curves represent the solution points of the circuit, where $I_{leakage}$ of both devices are equal.

The equation used to calculate the power consumption is;

$$P_s = I_{PMOS} \cdot (V_{dd} - V_{OUT}) + I_{NMOS} \cdot (V_{OUT} - 0) \quad (1)$$

where I_{PMOS} and I_{NMOS} are the currents flowing through the devices. To calculate the energy consumed per cycle, the power consumption is multiplied by the propagation delay (t_p) of one cycle, which can be calculated from the dynamic analysis in the next described section.

B. DYNAMIC ENERGY CONSUMPTION

CMOS dynamic power consumption is due to the current that flows when the inverter is switching from one logic state to the other. In order to estimate this energy consumption, the t_p is evaluated using a lumped load capacitance to ground (C_L). This load capacitance is the sum of all interconnect capacitances (including gate-drain capacitance (C_{GD}), drain-bulk capacitance (C_{DB}) and fan-out gates (C_G), (see Fig. 4a) connected to the output of the CMOS circuit [6]. Fig. 4b shows an example of gate parasitic capacitance as a function of gate voltage calculated by TCAD simulator. The other capacitances were also simulated and C_L calculated. The fan-out of the logic gate was considered equal to 1.

The equation that allows to calculate the dynamic energy consumption is;

$$E_d = C_L \cdot V_{DD}^2 \quad (2)$$

To evaluate the energy consumption, from eq. (1), the propagation delay, t_p is estimated by integrating the capacitor discharge/charge current. Equation (3) is a good approximation to calculate t_p from TCAD data [21];

$$t_p = 0.69 \cdot C_L \cdot \left(\frac{R_{eqn} + R_{eqp}}{2} \right) \quad (3)$$

where R_{eqn} and R_{eqp} are the equivalent resistance of nMOS and pMOS devices respectively. This propagation delay represents the minimum time needed to switch from one state

to the other. However in real circuits the logic gates are not switching as faster as possible, since their switching depends on the input signals. This is considered by adding an activity factor, whose value in this work is kept constant, to 0.001.

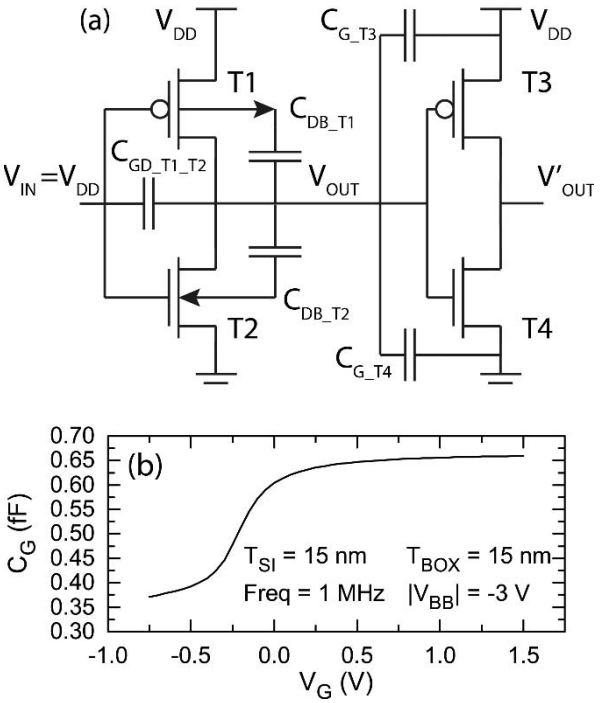

FIGURE 4. (a) Parasitic capacitances impact the transient behavior of the inverter, with fan-out equal to one. (b) An example of one gate parasitic capacitance.

Fig. 5 shows the total power consumption and maximum operating frequency (a) and the energy consumption per cycle (including the static and dynamic contributions) (b) as a function of V_{DD}. The considered parameters for those simulations were T_{SI} = 15 nm and T_{BOX} = 15 nm and the V_{BB} was equal to −3/3 V for n/p type. As it can be seen, when V_{DD} is scaled down (from 0.7 V to 0.4 V) the performance is reduced 1.7X, however, the energy consumption is improved 3.2X. This indicates that operating near the threshold voltage (see fig. 2b) reduces significantly the energy consumption [6]. Similar results have been obtained in circuits for other device technologies in [5] or for the same technology [11], [22] validating the methodology used in this work.

IV. PARAMETRIC STUDY

$|V_{BB}|$ and device structural parameters (such as T_{SI} and T_{BOX}) can impact the performance of UTBB FDSOI devices, and consequently, that of the inverter. Then, a detailed parametric study has been carried out, to evaluate the dependence of the energy consumption and I_{on}/I_{off} ratio of the inverter on those magnitudes.

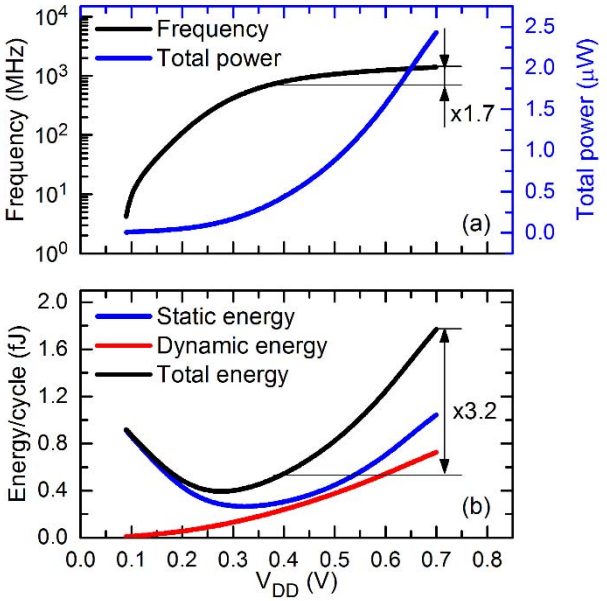

FIGURE 5. Simulated power, frequency and energy per cycle in a CMOS inverter implemented with UTBB FDSOI devices (T_{BOX} = 15 nm, T_{SI} = 15 nm) and the $|V_{BB}|$ = 3 V.

A. DEVICE OPERATION STUDY (BB)

Firstly, the impact on the energy consumption and I_{on}/I_{off} ratio of the $|V_{BB}|$ applied to the devices in the inverter is analyzed. This current ratio is also included in the study, because in digital applications values around 1000 are required for this ratio (International Roadmap for Devices and Systems (IRDS 2016) [23]) in order to distinguish the logic states. The simulations were performed in 2D because device properties were assumed to be completely homogeneous in the Z-axis direction. This assumption reduces the computational time (minutes) compared to 3D simulations (hours).

Fig. 6a and 6b show the energy consumption and the I_{on}/I_{off} ratio as a function of V_{DD}, respectively, for different V_{BB} ranging (from 0 to −4/4 V in n/p type devices). Structure parameters are kept constant with values T_{SI} = 15 nm and T_{BOX} = 15 nm. As it can be observed, when the $|V_{BB}|$is increased (negative values in nMOS and positive values in pMOS) the performance and consumption of the circuit improves. In fact, when $|V_{BB}| = 0$, V_{DD} for minimum energy is less than zero. These results can be explained through TCAD simulations. Higher $|V_{BB}|$ prevents the creation of the inversion layer under the gate. Therefore, the carrier concentration decreases (not shown), what rises the V_{TH} of devices and consequently reduces the current. Regarding the increase of the I_{on}/I_{off} ratio with $|V_{BB}|$ rises, it can be explained because Ion is only slightly reduced but I_{off} is diminished 2 orders of magnitude approximately.

As it can be seen, the V_{DD} that minimizes the energy consumption (yellow points Fig. 6a) and maximize the I_{on}/I_{off} ratio (yellow points Fig. 6b) are not coincident. Therefore an operation point that correspond to the best trade-off between

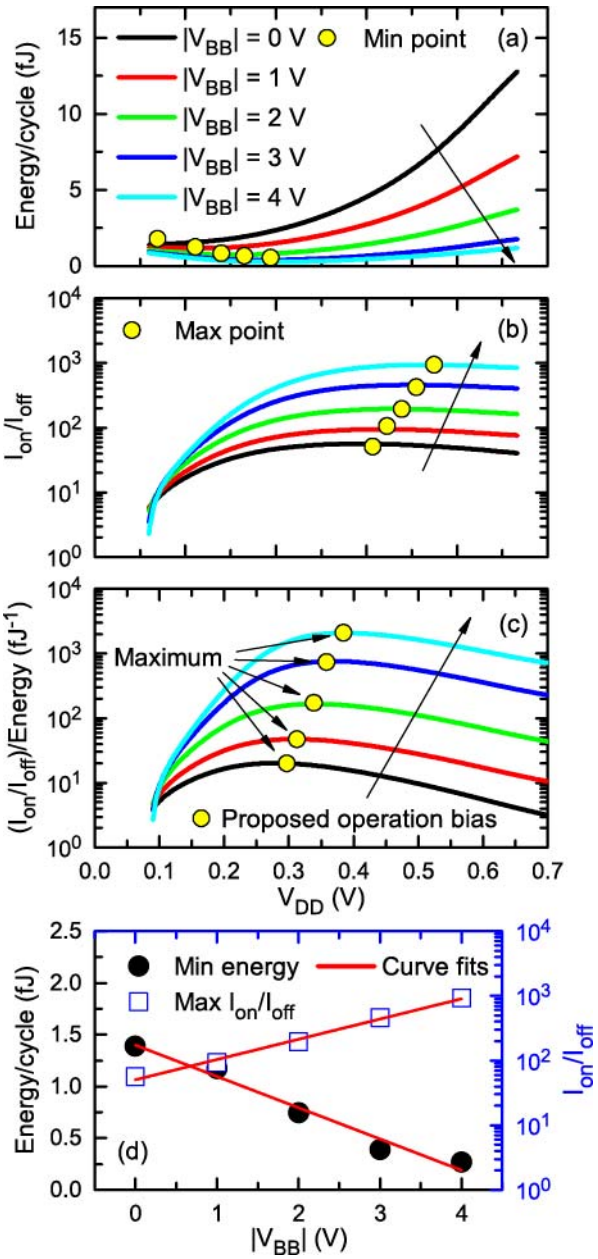

FIGURE 6. (a) Total energy consumption, (b) I_{on}/I_{off} ratio and (c) I_{on}/I_{off} and energy consumption ratio as a function of V_{DD}, for different $|V_{BB}|$ values. (d) Minimum energy consumption (black solid circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of $|V_{BB}|$. Red lines represent the data fitting. T_{SI} = 15 nm and T_{BOX} = 15 nm.

the two parameters has been proposed, as $\frac{I_{on}/I_{off}}{Energy\ consumption}$ which is shown in Fig. 6c. Note that this figure of merit has a maximum for a determined V_{DD} (yellow points Fig. 6c) whose value, V_{OP}, is proposed as an operation point of the inverter.

Fig. 6d shows the minimum energy consumption and the maximum I_{on}/I_{off}, as a function of $|V_{BB}|$. The studied devices show a linear dependence of the minimum energy consumption on $|V_{BB}|$. It is worth highlighting that this linear dependence is not accurate at the extreme values of $|V_{BB}|$ (0 and 4 V) indicating a possible saturation of the tendency. On the other hand, a logarithmic dependence is found for the maximum I_{on}/I_{off} as a function of $|V_{BB}|$. This kind of relationships could be useful in order to optimize the $|V_{BB}|$ voltage because they allow to predict the minimum $|V_{BB}|$ required to reach a target parameter.

B. DEVICE STRUCTURE STUDY (T_{BOX}, T_{SI})

A similar study to that shown in the previous section has been performed, but now, sweeping T_{BOX} between 10 and 25 nm, while the other parameters are kept constant T_{SI} = 15 nm and $|V_{BB}| = 3$ V. Minimum energy consumption and maximum I_{on}/I_{off} ratio as a function of T_{BOX} is represented in Fig. 7a. Moreover similar dependences of the minimum energy (linear) or maximum I_{on}/I_{off} (logarithmic) on T_{BOX} is observed as for the case of $|V_{BB}|$ Fig. 6d. The results indicate that a thinner BOX improves the electrical characteristics of the devices, reducing the energy consumption and rising the I_{on}/I_{off} ratio Fig. 7a. Fig. 7b represents the ratio I_{on}/I_{off} - energy as a function of V_{DD} showing that the V_{OP} increases when the T_{BOX} decreases, but it is still kept near to the threshold voltage. This dependence can be explained because smaller T_{BOX} leads to a higher influence on the carriers of the channel, increasing the device currents.

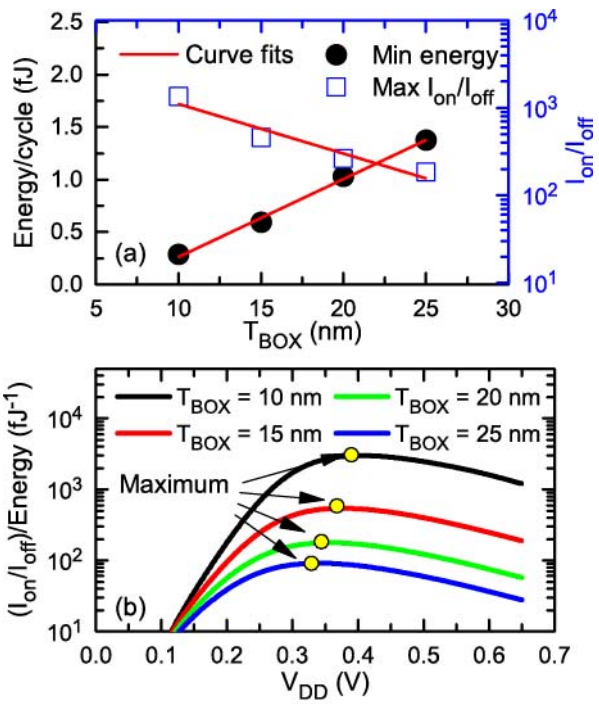

FIGURE 7. (a) I_{on}/I_{off} and energy consumption ratio as a function of V_{DD}, for different T_{BOX}. (b) Minimum energy consumption (black solid circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of T_{BOX} (b). Red lines represent the data fitting. T_{SI} =15 nm and |BB| = 3 V.

Finally, the impact of T_{SI} is analyzed in Fig. 8 (T_{BOX} =15 nm and |BB| = 3 V). Minimum energy consumption and maximum I_{on}/I_{off} ratio as a function of T_{SI} are

represented in Fig. 8a. When T_{SI} is diminished, the energy consumption and I_{on}/I_{off} improve significantly. This improvement in the energy consumption can be explained because the current flowing through the channel is smaller for thinner T_{SI}. On the other hand, the improvement of I_{on}/I_{off} ratio can be explained because the gate exerts more control over the channel. Besides, similar dependences are observed when T_{SI} is changed than when T_{BOX} is varied. Nevertheless, in our structure, in the case of energy consumption, a higher dependence on T_{BOX} than on T_{SI} is observed, whereas the opposite is observed for the case of the I_{on}/I_{off} ratio. These relations indicate that a trade-off between both device parameters could be considered in order to optimize circuits for a particular propose. Fig. 8b shows V_{OP} (yellow points) for the different values of T_{SI}, obtaining similar values than those when T_{BOX} is swept.

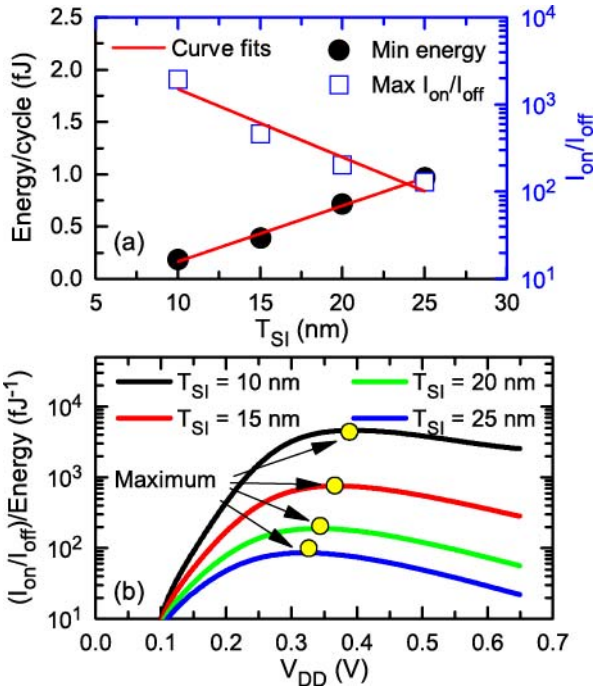

FIGURE 8. (a) I_{on}/I_{off} and energy consumption ratio as a function of V_{DD} for different T_{SI}. (b) Minimum energy consumption (black full circles) and maximum I_{on}/I_{off} ratio (blue empty squares) as a function of T_{SI}. Red lines represent the fitting performed. T_{BOX} = 15 nm and |BB|= 3 V.

In order to contextualize our results, the requirements for future technologies, the energy consumption per cycle and I_{on}/I_{off} ratios obtained for each V_{OP} estimated previously (see Fig. 6c, 7b and 8b) are compared to those given by [23]. To do this, in Fig. 9 the I_{on}/I_{off} ratio as a function of the energy consumption per cycle is represented. In solid black squares, the IRDS projected electrical specifications of logic core devices for each year are shown. The empty symbols represent our best result obtained for each of our studies ($|V_{BB}|$ = 4 V red circle, T_{BOX} = 10 nm green triangle and T_{SI} = 10 nm blue diamond), for the corresponding V_{OP}. Our results show lower energy consumption than projections beyond 2027 for all the studied cases, pointing out that UTBB-FD-SOI operating at NTV, with suitable $|V_{BB}|$, is an attractive candidate for low power applications. [3], [11]. However, the I_{on}/I_{off} ratio for $|V_{BB}|$ = 4 V and T_{BOX} = 10 nm are 46 % and 22% smaller than prediction respectively. Only when T_{SI} = 10 nm, the I_{on}/I_{off} ratio is comparable to the projections. This result indicates that T_{SI} parameter can play an important role to optimize this kind of devices.

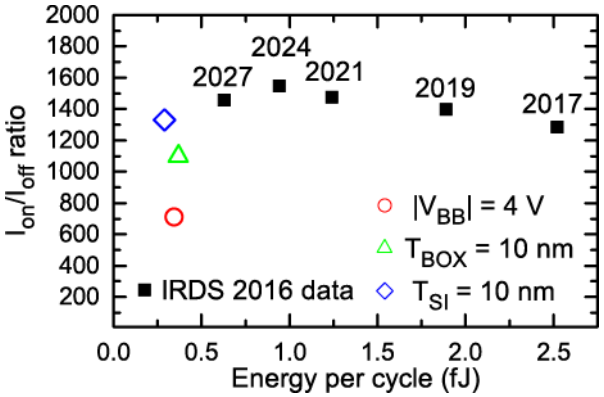

FIGURE 9. Comparison of energy consumption per cycle and I_{on}/I_{off} ratio of IRDS 2016 predictions from 2017 to 2027 (black solid squares) and our results (empty symbols).

C. IMPACT OF OXIDE TRAPPED CHARGE

Until now, simulated devices have not been considered to be affected by any variability source. In this section, the impact of interfacial traps charged with $1e^-$ on the frequency and energy consumption per cycle is analyzed. In particular, as a preliminary analysis, the study is focused on the comparison of these parameters in the pristine device to these devices where one trap is present in the gate oxide-channel (see Fig. 10a and 10b), in the BOX oxide-channel interface (see Fig. 10c and 10d) or both traps are simultaneously present. Since the presence of discrete charges in the devices breaks their homogeneity, the simulations were performed in 3D, with W = 100 nm. In the simulations T_{SI} = 15 nm, T_{BOX} = 15 nm and the $|V_{BB}|$ = 3 V were considered.

Fig. 10 shows the impact of one trap on the potential contour map in a n-type device, top (a) and sectional (b) view when it is introduced in the interface gate oxide–channel, and top (c) and sectional (d) view of the potential contour when the trap is located in the interface channel–BOX oxide. The bias applied to gate and drain contact was 0.35 V. As it can be observed, the trap modifies the device potential, hindering the carriers flow in the channel and consequently increasing the V_{TH} [20].

The change in the electrical behavior of devices because of the introduction of interfacial traps can provoke variations in the performance of logic gates. To show this point, frequency and energy consumption per cycle are analyzed, because large variations of these parameters in logic gates could be critical for design circuit [7].

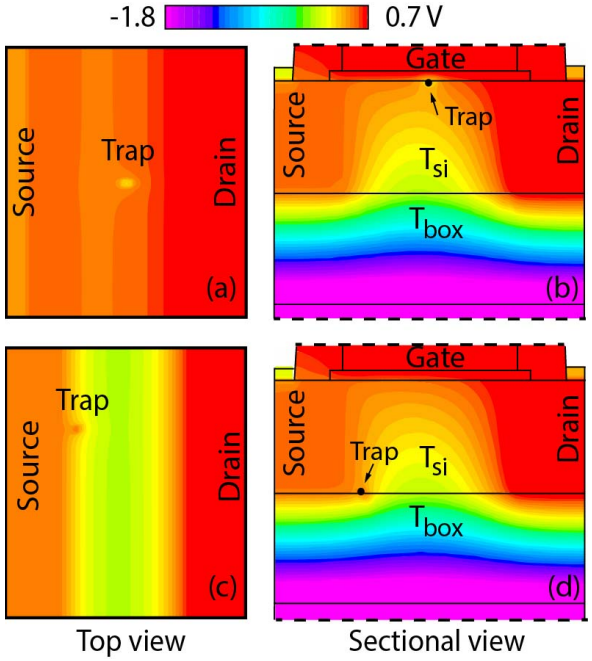

FIGURE 10. **(a, c) Potential maps of top and (b, d) sectional view of the device ($T_{SI} = T_{BOX} = 15$ nm and Vbulk = -3 V) when the trap is at the gate oxide (a,b) and at the BOX (c, d) interface. Gate and drain contacts are biased $V_{GS} = V_{DS} = 0.35$ V.**

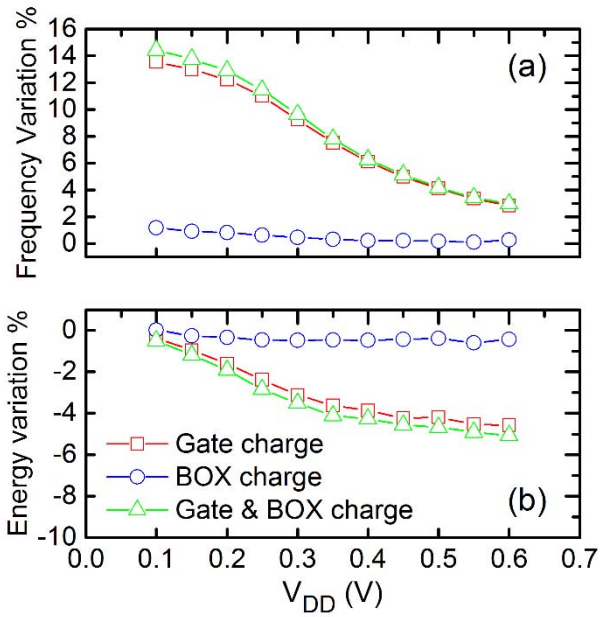

FIGURE 11. **(a) Frequency and (b) energy consumption shift when traps are present at gate (red squares), BOX (blue circles) and both simultaneously (green triangles) as a function of power supply (V_{DD}).**

Fig. 11a shows the frequency variation when charges are present compared to pristine devices. The impact of trap location was studied simulating three different scenarios; trap located at gate (G) interface, BOX interface (B) or both simultaneously (G & B). As it can be seen, traps located at the gate (red) have more impact than traps located at the BOX (blue) interface. Besides, the impact of both traps (simultaneously in the device) almost correspond to the sum of each trap separately, pointing out that the simulated traps, in our case, are independent. Also, the frequency variation depends on V_{DD}, being higher than 10% when V_{DD} is smaller than 0.30 V.

Fig. 11b shows the variation of energy consumption per cycle. Note that the variations are negative indicating that introducing traps in the device improves slightly the power consumption, around 4%. The cause of this improvement could be attributed to the reduction of leakage currents through the channel.

V. CONCLUSION

New strategies must be developed in order to reduce the power consumption of devices used in IoT. In this paper, UTBB-FD-SOI devices, which have been demonstrated to be good candidates for low power applications, have been considered operated at NTV for digital applications. The electrical characteristics of the devices have been simulated using Silvaco TCAD tool. The TCAD results were used to calculate the energy consumption and operation frequency of an inverter logic gate. The dependence of these parameters on two structural properties of devices (T_{BOX} and T_{SI}) and operation conditions (V_{BB}) has been studied. Our results indicate that higher |BB| and thinner T_{SI} and T_{BOX} improve significantly the energy consumption and I_{on}/I_{off} ratio of the logic gate. However, their impacts are different, and therefore an optimization criterion, which will depend on the application, must be considered. Besides, an operation point (V_{OP}) has been selected which could be useful on digital applications because it provides a good trade-off between the I_{on}/I_{off} ratio and the energy consumption. These results were compared to IRDS projections pointing out FD-SOI devices with thin T_{SI} and T_{BOX} operating at NTV as a promising technology in low power applications. Finally, the impact of interfacial traps on the frequency and energy consumption of the logic gate was studied obtaining variations in the frequency larger than 10%. Therefore, the variability related to the presence of charges in the gate and BOX oxide interfaces can be critical for the performance of circuits based on these devices operating in NTV.

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