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Improvement of Charge Injection by Using Separated SiN as Charge Trapping Layer in MONOS Charge Trap Flash Memory

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ABSTRACT The charge trapping characteristics in the metal-oxide-nitride-oxide-silicon memory with separated trapping layer were investigated. Charge injection was enhanced for the reduction of effective oxide thickness of the gate dielectric. High program/erase speed as well as large shift of the threshold voltage were obtained. Charges injection was improved according to the constant current stress measurement. The application of separated charge trapping layer can considerably improve the performance of charge trapping memory.

INDEX TERMS Hafnium oxide, charge trapping memory, NAND flash memory.

I. INTRODUCTION

The market growth of mobile applications such as smart phones and tablet computers has fueled the explosive demand of NAND Flash memories having high density [1]. Charge trapping flash (CTF) memory devices attract much attention due to their advantages such as of low program/erase (P/E) voltage, high scalability, and excellent endurance [2]. Nowadays, high-*k* materials were introduced as gated dielectric layer (tunneling layer and blocking layer) for the high performances achievement in CTF memory [3]. Meanwhile, metal was usually used as electrode companied with this high *k* gate dielectric. This metal-oxide-nitride-oxide-silicon (MONOS) structure was reported with good performance [4]. Among the high-*k* materials, HfO_2 is a desirable dielectric material due to its compatibility with the Si-based industry process [5], [6]. Nevertheless, the advantage of the high-*k* based gated dielectric was not sufficiently used for the NVM applications. For example, in high-*k* based MONOS structures, the charge trapping layer was inserted in the gate dielectrics, which makes it difficult to reduce the effective oxide thickness (EOT) of the gate dielectric for obtaining a high gate-to-channel coupling. This is harmful for fast program/erase characteristics because the charge trapping layer of SiN is in low-*k* state which degrade the function of high-*k* dielectric.

In this work, the SiN charge trapping layer that is separated from gate dielectric were fabricated for CTF memory applications. Its electrical characteristics are compared with those of a control device, i.e., a conventional MONOS device with intact charge trapping layer. The reduced EOT in proposed structure increases the electrical field across the tunneling oxide which effectively improves charge injection, resulting in the improved program/erase characteristics with high speed.

II. EXPERIMENT

The stack of the proposed and control MONOS structures were shown in Fig. 1(a) and (b), respectively. Same transistor size was adopted for the conventional and control devices, including same thickness of charge trapping layer. A standard RCA cleaning was applied on n-type Si (100) substrates ($1cm^2$) and the native dioxide on the Si surface was removed by diluted HF solution. Then, a 3 nm-thick tunneling oxide of HfO_2 was fabricated with atomic layer deposition (ALD) with $Hf[N(CH_3)C_2H_5]_4$ (TEMAH) and O_3 as precursors at 250 °C. Then a 5nm charge trapping layer was deposited on the HfO_2 surface using CVD method followed by pattern, electron beam photolithography (EBL) and ICP etching process. The pattern area was rectangular array for the purpose of totally separating the SiN layer (the length is $3\mu m$ and the

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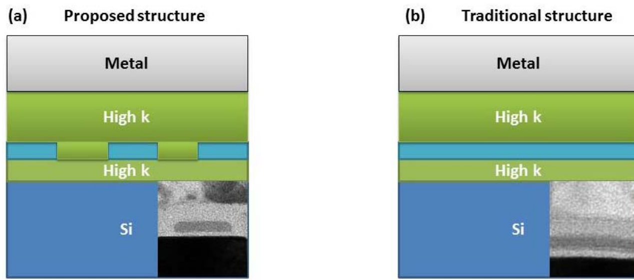

FIGURE 1. Illustration of (a) the proposed MONOS stack and (b) the control MONOS structure. Inset shows the TEM image of the corresponding structures.

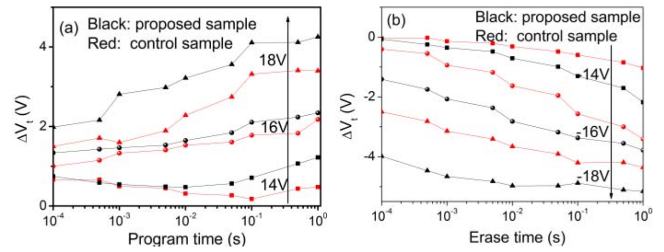

FIGURE 3. (a) Program transient characteristics vs. time of the fabricated devices at various bias conditions. (b) Erase transient characteristics of the fabricated devices at various bias conditions.

width is 30nm). For comparison, an intact charge trapping nitride was also fabricated without pattering. Meanwhile, the 3-9nm charge trapping layers were also prepared for both proposed and control stacks. Then, a 10 nm-thick blocking HfO_2 layer was deposited. For both devices, 200nm thick Al metal was deposited as a gate electrode and source/drain (S/D). The Al metal gate electrode deposited by electron beam evaporator was patterned by photo lithography as a square shape of $300 \times 200\mu m^2$ size. All devices were treated by a 500 °C annealing for 30min in a vacuum after electrode deposition. Except for three-terminal transistor, the simple two-terminal MONOS stack capacitors were also prepared. The thickness and microstructure were analyzed by using transmission electron microscopy (TEM). A Keithley 2400 SourceMeter was used to measure the *I–V* characteristics. The high frequency (1 MHz) capacitance-voltage (*C-V*) measurement (sweep range of ±6 V) were carried out to evaluate the charge trap property at trap layer. The TEM images of stacked structures were shown in inset of Fig. 1. The charge trapping layers in both devices have the same thickness but the overall structures of the gate dielectric stacks notably differ.

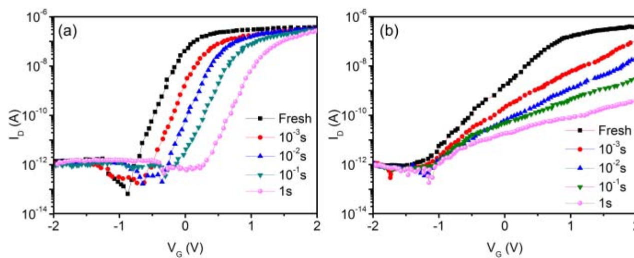

FIGURE 2. Transfer characteristics of (a) the control device and (b) the proposed device under 14V voltage with various programming time.

III. RESULTS AND DISCUSSION

In order to verify the performance of the charge trapping memory, the transfer characteristics were investigated after 14V programming voltage under different pulse time. Fig. 2(a) and (b) show the program characteristics of the control device and proposed devices, respectively. It was observed that the transfer curves of both devices shifted to the positive direction with the increasing of programming time. This confirms that the oxide-nitride-oxide (ONO) layers normally work. It was worth noting that the shift of the transfer characteristics in control device was parallel, whereas, the shift in proposed device was dispersive, which makes it have larger shift of the threshold voltage (V_t) at the same current (for example, 10^{-10}A). Actually, the proposed device can be equal to two parallel transistors: a transistor with an ONO layer and a sidewall transistor with only oxide layer. The V_t of the transistor is constant in programming process for the sidewall transistor, while the V_t of the transistor with an ONO layer is increasing due to the present of the charge trapping layer (SiN), which results in the non-parallel shift of the V_t. The degraded SS characteristic of the proposed device is a drawback. This degradation is caused by the structural difference compared with the control device. Since the charge injection could be greatly enhanced in proposed device, the proposed device leads to more charge accumulation (and fast injection) in separated SiN compared to that of control device at the same condition. The gate controllability to channel fitly though the separated SiN layer was actually degraded at this case. This was also confirmed by the TCAD stimulation below.

Meanwhile, Fig. 3(a) shows the program characteristics of the fabricated device at three voltage bias conditions, respectively. It was confirmed that the proposed device shows faster program speed than the control device with the same program voltage condition. As observed in the threshold voltage shifts (ΔV_t) according to the program voltages, all the program characteristics of the proposed device are better than those of the control device. Fig. 3(b) shows the erase characteristics of the fabricated devices. Similar to the trend observed in the program characteristics, the proposed device shows faster erase speed than the control device.

To verify the capability of charge storage, two-terminal capacitors based on our proposed MONOS structure were also investigated. Fig. 4 shows the flatband voltage shift (ΔV_{FB}) in both proposed and control capacitors as a function of the SiN thickness using *C-V* measurement. The ΔV_{FB} of both capacitors increase with the increasing of SiN thickness. However, the proposed capacitor shows a larger memory window than the control one at the same thickness. This result implies that more charges could be trapped in separated

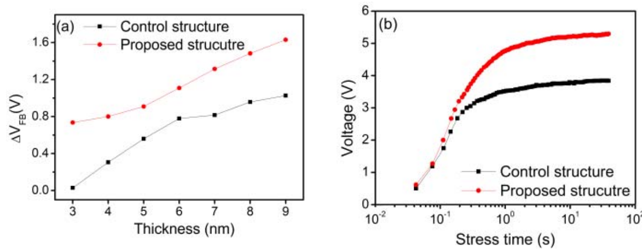

FIGURE 4. **(a) Dependence of flatband voltage shift (ΔV_{FB}) for both proposed and control MONOS capacitors on the thickness of charge trapping layers at high frequency of 1 MHz. (b) Charge trapping characteristics of both MONOS capacitors under constant current stress.**

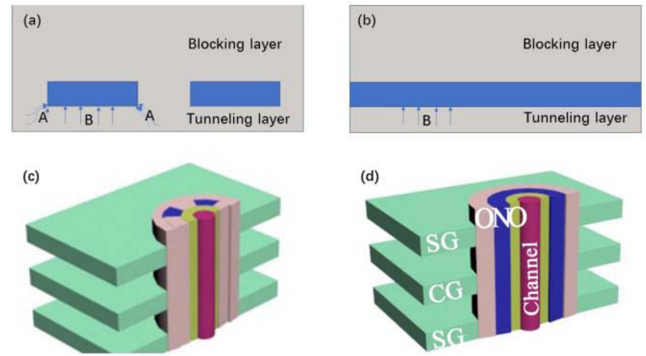

FIGURE 5. **Schematic illustration of the corner field and planer field for (a) the proposed MONOS planer structure and (b) the control MONSO structure. (c) The proposed and (d) control charge trapping layers (blue) in 3D-NAND string. Three cells are present: Center Gate (CG) and two Side Gates (SG).**

SiN layer even in same thickness. This should be ascribed to the reduction of the EOT in proposed structure, which further enhance the local electrical field on ONO stack layers. On the other hand, though the memory window of both capacitors in Fig. 4(a) continuously increases with the SiN thickness, different trends was present between the proposed and control capacitors at large thickness region (>6nm). That is, the ΔV_{FB} of control capacitor gradually became saturated with further increasing of the SiN thickness. This result is contrast with the robust increasing of ΔV_{FB} in proposed capacitors, which should be due to the enhancement of the local electrical field. Meanwhile, as shown in Fig. 4(a), even in ultrathin trap layer (less than 5nm), the memory window of separated capacitor is much higher than that of the intact SiN layer and show a similar value to 7nm-thick SiN trap layer in control structure.

We also evaluated the charge trap density of both SiN layers using the constant current stress measurement [7]. Fig. 4(b) shows charge trapping characteristics of both MONOS capacitors under constant current stress. The stress current is 10^{-8}A. The voltage drop at ONO stacked layer was measured as the gate voltage shift varied with increasing stress time. The shift in gate voltage is attributed to the charge trapping in SiN layer. It is confirmed that the proposed structure showed robust charge trap characteristic because the gate voltage shift was more significant compared with that of the control structure as shown in Fig. 4(b). Accordingly, we can conclude that the separated SiN layer has better charge trapping characteristics than intact SiN layer at the same thickness. This result is also well consistent with the results of Figs. 2 and 3, respectively.

It is concluded that the improved program/erase performance in the proposed device stems from the effective reduction of EOT. In proposed MONOS stacks, the EOT of the gate dielectric is actually decreased, thus the electrical field correspondingly increases. This enhancement of the electrical field boosts trapping/detrapping of the charges. On the other hand, the proposed structure not only strengthens the electrical filed across the gate dielectric with reduced EOT, but also physically put the SiN in an all-around surrounding state by high *k* dielectric. The distribution of the electrical filed is thus different with the control structure as shown in Fig. 5 (a) and (b). It is known that the electrical field near the corner region (denoted as region A) was much stronger than that in the plain bulk region (denoted as region B) for the control sample [8]. The proposed structure increases the contact area between charge trapping layer with the gate dielectric, which further increases the local corner electrical field. The energy band of the tunneling oxide could be steeper due to the enhancement of the field inside the tunneling oxide. This local enhancement of the field could improve the charge injection effectively. Meanwhile, due to the physically all-around surrounding of the high *k* dielectric to the separated layer, the charge retention was also acceptable. There was no degradation compared with the traditional intact SiN layer (data not shown). The proposed separated SiN layer could also be used in 3D NAND string, which is under investigation as shown in Fig. 5 (c) and (d). Improved gate-to-channel coupling could be expected due to the sufficient EOT reduction of high-*k* oxide dielectrics. Meanwhile, the separated charge trapping layer could reduce the probability of the noise ascribed to the interaction between the charge trapping layer with the surrounding layers.

Figure 6 (a) and (b) shows the retention characteristics of the proposed and control structures measured at room temperature. Average charge decay rates of the proposed and control structures were 133 mV/decade and 139 mV/decade in the programmed state and 163 mV/decade and 187 mV/decade in the erased state, respectively. The extrapolated data suggest that the memory window would still be as large as 1.25 V after 10 years in the proposed device. There was no degradation compared with the traditional control device with intact SiN layer. Moreover, due to the more efficient and sufficient charge injection, the initial and final widow in proposed sample is larger than that of the control one. The endurance characteristics of the two devices are shown in Fig. 6(c). Endurance degradation was not observed even after 10^5 *P/E* cycles, which indicates that the proposed device is good enough to be used for flash memories. The reliability proves the important advantage of the proposed structure: Improving the charge injection

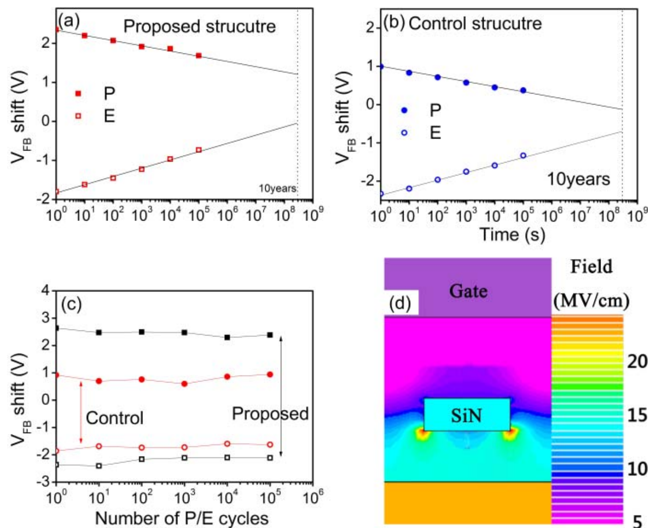

FIGURE 6. The retention characteristics of the proposed (a) and the control (b) structure. The endurance characteristics of both the devices (c). Cross-sectional E-field using 3-D TCAD simulation (d).

without sacrificing the preservation of charges. The conflict of the charge injection and the preservation is well known to be the main issue for the FG memory (including nanocrystal FG), as Dr. Jan De Blauwe has comprehensively reported before [9]. This is very interesting and practical considering the simplicity of our proposed separated structure, which is under further investigation.

The cross-sectional E-field for the proposed devices using simulation of TCAD is shown in Fig. 6(d). The improved efficiency of charge injection and fast program/erase characteristics of the proposed device were verified by simulation. The vertical E-field inside the tunneling oxide is strengthened in the proposed structure by the "corner" local region. The enhancement of the E-field could be caused by the combination of special local corner and the reduced EOT. At the same time, the robust field at local region is help to the hot electrons getting into SiN layer except for FN tunneling.

IV. CONCLUSION

In summary, the charge trapping characteristics of separated charge trapping layer were investigated. The proposed structure shows a larger memory window than the traditional memory at the same condition. The increased oxide coupling by the reduced EOT value strengthened the local electrical field inside the tunneling oxide to improve charge injection. The program/erase characteristics were enhanced with high speed and low operation voltage. These results would provide advantages in charge storage for next generation CTF memory.

REFERENCES

[1] C. H. Huang, W. C. Chang, J. S. Huang, S. M. Lin, and Y. L. Chueh, "Resistive switching of Sn-doped In_2O_3/HfO_2 core-shell nanowire: Geometry architecture engineering for nonvolatile memory," *Nanoscale*, vol. 9, no. 20, pp. 6920–6928, May 2017, doi: 10.1039/c6nr09564j.

[2] S. M. Amoroso *et al.*, "3D Monte Carlo simulation of the programming dynamics and their statistical variability in nanoscale charge-trap memories," in *Proc. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2010, pp. 22.6.1–22.6.4, doi: 10.1109/IEDM.2010.5703415.

[3] N. Ramaswamy *et al.*, "Multi-layer high-K tunnel barrier for a voltage scaled NAND-type flash cell," in *Proc. IEEE Workshop Microelectron. Electron Devices (WMED)*, Boise, ID, USA, Apr. 2009, pp. 1–3, doi: 10.1109/WMED.2009.4816146.

[4] Y. Q. Wang *et al.*, "Fast erasing and highly reliable MONOS type memory with HfO2 high-k trapping layer and Si3N4/SiO2 tunneling stack," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Apr. 2006, pp. 1–4, doi: 10.1109/IEDM.2006.346948.

[5] J. Ran, X. Erqing, and W. Zhenfang, "Interfacial chemical structure of HfO_2/Si film fabricated by sputtering," *Appl. Phys. Lett.*, vol. 89, no. 14, Oct. 2006, Art. no. 142907, doi: 10.1063/1.2358841.

[6] R. Jiang, X. Du, Z. Han, and W. Sun, "Investigation of chemical distribution in the oxide bulk layer in Ti/HfO_2/Pt memory devices using x-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 106, no. 17, Apr. 2015, Art. no. 173509, doi: 10.1063/1.4919567.

[7] H.-W. You and W.-J. Cho, "Charge trapping properties of the HfO_2 layer with various thicknesses for charge trap flash memory applications," *Appl. Phys. Lett.*, vol. 96, no. 9, p. 323, Mar. 2010, doi: 10.1063/1.3337103.

[8] J.-H. Ahn *et al.*, "A SONOS device with a separated charge trapping layer for improvement of charge injection," *AIP Adv.*, vol. 7, no. 3, Mar. 2017, Art. no. 035205, doi: 10.1063/1.4978322.

[9] J. D. Blauwe, "Nanocrystal nonvolatile memory devices," *IEEE Trans. Nanotechnol.*, vol. 99, no. 1, pp. 72–77, Mar. 2002, doi: 10.1109/TNANO.2002.1005428.

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