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Si₃N₄/Al₂O₃ Stack Layer Passivation for InAlAs/InGaAs InP-Based HEMTs With Good DC and RF Performances

**PENG DING, CHEN CHEN[✉], MUHAMMAD ASIF, XI WANG, JIEBIN NIU, FENG YANG,
WUCHANG DING, YONGBO SU, DAHAI WANG, AND ZHI JIN**

HF & HV Center, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

CORRESPONDING AUTHORS: C. CHEN and Z. JIN (e-mail: chenchen@ime.ac.cn; jinzhi@ime.ac.cn)

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ABSTRACT This paper introduces a novel surface passivation using Si₃N₄ (20-nm)/Al₂O₃ (15-nm) stack layers in InAlAs/InGaAs InP-based high-electron-mobility transistors (HEMTs). The new technology gives rise to good dc and RF performances in InP-based HEMTs. Notably different from the conventional Si₃N₄ approach, an ultrathin layer of Al₂O₃ (15-nm) grown by atomic layer deposition is incorporated in the surface passivation, which is the main feature of this technology. After passivation, the Si₃N₄/Al₂O₃-passivated HEMTs exhibit a superior dc performance demonstrating a high drain current up to 800 mA/mm, an increased peak transconductance of 1100 mS/mm at V_{GS} = -0.2 V and a slight threshold voltage shift of ΔV_{th} = +120 mV. In terms of their RF performance, a maximum oscillation frequency (*f*_{max}) up to 340 GHz has been obtained, showing an excellent quality of the surface passivation. A physical explanation is addressed over why the good dc and RF performances have been achieved.

INDEX TERMS InP-based high-electron-mobility transistors, Si₃N₄/Al₂O₃ stack layer passivation, DC characteristic, RF characteristic, small-signal modelling.

I. INTRODUCTION

Indium-phosphide-based high-electron-mobility transistors (InP-based HEMTs) with an extraordinary high-frequency [1] and a low-noise [2] performance are considered as the promising candidates to become the key components in Monolithic Millimeter-Wave Integrated Circuits [3], [4]. Surface passivation on gate recess region of the InP-based HEMTs is critically important to prevent the DC anomalous effects and achieve a long-term operational reliability.

Passivation issues in the InP-based HEMTs has been a long-term research topic in the community. Normally, a thick Si₃N₄ layer (~100nm) grown by Plasma Enhanced Chemical Vapor Deposition (PECVD) has been used to passivate the device [5], [6]. Whereas, the performance of InP-based HEMTs after passivation, e.g., the Maximum Oscillation Frequency (*f*_{max}) degrades due to the increment in parasitic capacitance [7]. Recently, an ultra-thin

Al₂O₃ layer deposited by atomic layer deposition (ALD) has been widely used in the III-V based HEMTs [8]–[10]. For instance, in [8], an Al₂O₃ thin layer deposited by CVD on GaN was reported as an effective surface passivation. The obtained results indicate that the present Al₂O₃ layer is promising for surface passivation and for the gate insulator in GaN-based electron devices. Seo and Kim [9], figured out that even though the effects of passivation are becoming more important in nanoscale HEMT devices, it is not clear which is the optimum passivation process. Full passivation of the gate structure is also needed for better reliability.

Up to now, there has been no report on the Si₃N₄/Al₂O₃ stack layer passivation in InAlAs/InGaAs InP-based HEMTs. And, their DC and RF performances of HEMTs are still waiting to be disclosed. In the case of the Al₂O₃/Si₃N₄ stack layer passivation, it has several advances against other approaches used. Compared with a single Si₃N₄ layer,

although there is an additional thin layer of Al_2O_3 , it was reported by [11] that it could eliminate the surface bombardment caused by ionized plasma during the PECVD processing, and was capable of the coverage to the complex gate structures with a superior thickness controllability. On the other hand, compared with a single Al_2O_3 layer, the incorporated Si_3N_4 thin layer could reduce the overall permittivity of the passivation layer. Because of this, an increase in the parasitic capacitance could be limited.

In this article, we present a novel passivation method using a set of stack layers including Si_3N_4 (group_1), $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ (group_2), Al_2O_3 (group_3), and $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ (group_4). Their effects on both DC and RF performances have been demonstrated. To evaluate the mechanism of RF performance, a small-signal model has been established, and the parasitic capacitance of C_{gs} and C_{gd} has been extracted and analyzed.

II. EXPERIMENT

Fig. 1(a) shows the InP-based HEMT structure we used in this work. The lattice matched InAlAs/InGaAs epitaxial layers are grown by MBE on a 3-inch semi-insulating InP substrate. These epilayers from bottom to top consist of 500 nm undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer, 15 nm undoped $\text{In}_{0.53}\text{Al}_{0.47}\text{As}$ channel layer, 3 nm undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ spacer layer, Si delta doping layer with $5 \times 10^{12} \text{ cm}^{-2}$ doping concentration, 8 nm undoped $\text{In}_{0.52}\text{AlAs}$ barrier layer, 4 nm InP etch-stop layer and 15 nm Si-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capping layer. Then, to form HEMT's structure, it has been carried out by mesa etching, source-and-drain ohmic contact formation, T-shaped gate recess via e-beam lithography. Ti(25nm)/Pt(25nm)/Au(300nm) is formed as a gate electrode via E-beam evaporation followed by gate recess lift-off defining the gate area of $2 \times (0.12 \times 50) \mu\text{m}^2$, as shown in Fig. 1(b). Detailed fabrication processing has also been mentioned in elsewhere [12].

For the surface passivation, in Fig. 1(a), InP-based HEMTs are then encapsulated with a set of Si_3N_4 and Al_2O_3 stack layers right after the gate-recess lift-off. A 15-nm Al_2O_3 layer is deposited by ALD (Beneq TFS200) at 220 °C, using trimethylaluminum (TMA) and H_2O precursors as Al and O sources. The growth rate is $\sim 1.05 \text{ \AA}/\text{cycle}$ with 500-ms of pulse and 5-sec of N_2 purge as a single growth cycle. And a 20-nm Si_3N_4 layer is formed by PECVD (Plasma-Therm 790+) at 294 °C, using precursors of He-diluted Silane (flow rate: 500 sccm) and ammonia gas (flow rate: 27 sccm) at 904 mTorr with RF power of 100 W. The surface passivation domain is defined via photolithography and a refined wet-etching process to selectively remove Al_2O_3 and Si_3N_4 layers. To minimize the processing variation from each group of samples, a commercial 7:1 BOE etchant has been used for all samples with the etching rate of 30 $\text{\AA}/\text{sec}$ for Al_2O_3 and 22 $\text{\AA}/\text{sec}$ for Si_3N_4 respectively, confirmed by Atomic Force Microscopy (not shown here).

To characterize the surface passivation effect, DC performance is carried out before and after passivation

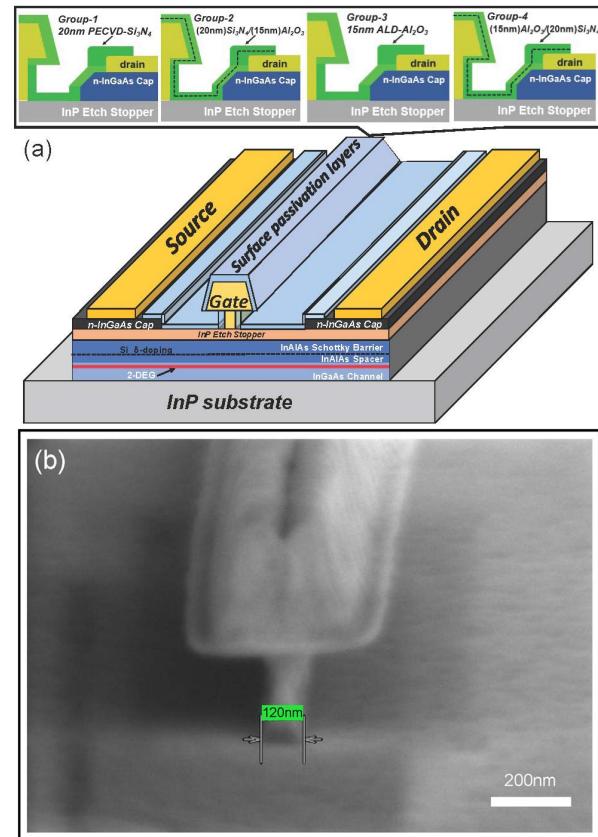


FIGURE 1. (a), A schematic view of Al_2O_3 and Si_3N_4 stack layer passivated InP-based HEMTs, and (b), FESEM image of the tilted T-shaped gate with gate footage of 120 nm.

through HP4142 semiconductor parameter analyzer at room temperature. RF Performance is characterized via an Agilent E8363B PNA vector network analyzer from 0.1 GHz to 40 GHz at room temperature. Their S-parameters are extracted and analyzed after measurement.

III. RESULTS AND DISCUSSION

A. DC CHARACTERISTICS

Fig. 2 and Fig. 3 show the DC characteristics of a $2 \times (0.12 \times 50) \mu\text{m}^2$ InP-based HEMT before and after different passivation including Si_3N_4 , $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$, Al_2O_3 and $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$. In Fig. 2(a), it plots the $I_{DS}-V_{DS}$ curves before and after $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation from group_2. In Fig. 2(b) and (c), it plots the $I_{DS}-V_{GS}$ curves and the transconductance (g_m) against V_{GS} curves from group_2 at $V_{DS} = 1.5 \text{ V}$ and $V_{DS} = 1.0 \text{ V}$, respectively. Before passivation, at $V_{DS} = 1.5 \text{ V}$, the drain current, I_{DS} , reaches 740 mA/mm at $V_{GS} = 0.08 \text{ V}$. After $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation, it has a dramatic increase up to 800 mA/mm at the same effective V_{GS} , considering the positive threshold voltage shift (ΔV_{th}) of +0.12 V after passivation. As shown in Fig. 2(b), the threshold voltage (V_{th}) is extracted to be -0.738 V before passivation and -0.618 V after passivation. A limited positive V_{th} shift +0.12 V is obtained after the $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$

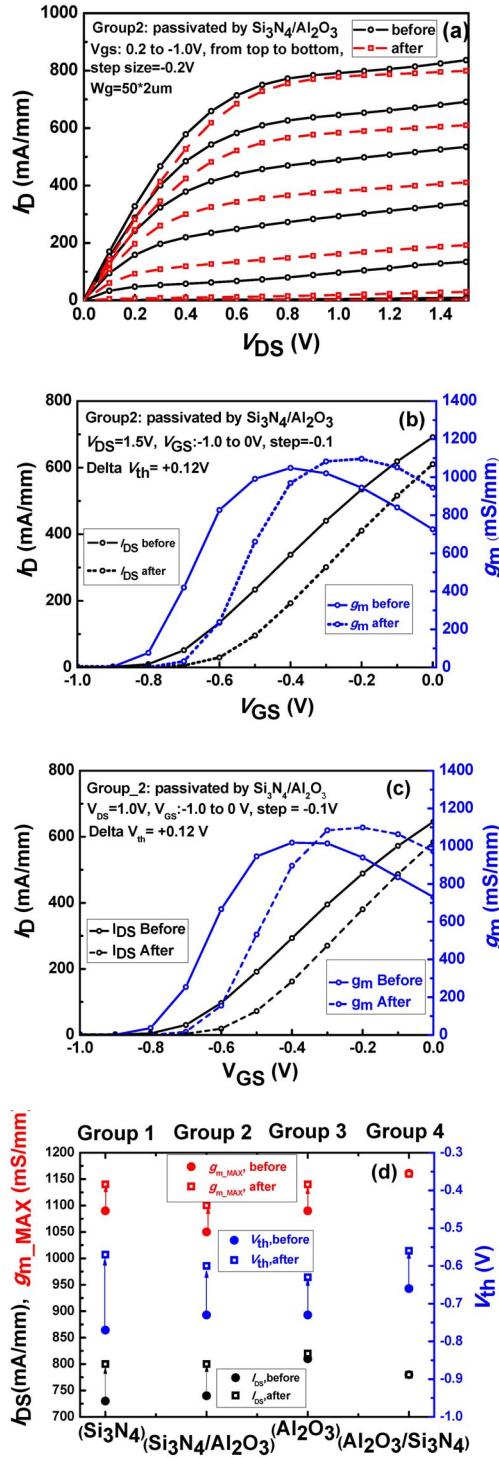


FIGURE 2. DC characteristics: (a) I_{DS} - V_{DS} curve of a $2 \times (0.12 \times 50) \mu\text{m}^2$ HEMT with $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation. (b) Transfer curves from Group_2($\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$) measured at $V_{DS}=1.5\text{V}$ before and after passivation. (c) Transfer curves from Group_2($\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$) measured at $V_{DS}=1.0\text{V}$ before and after passivation. (d) A summary of DC parameters, including I_{DS} , $g_{m,\text{MAX}}$, and V_{th} at $V_{DS}=1.5\text{V}$ before and after passivation.

passivation. In addition, at $V_{DS} = 1.5\text{V}$, the peak transconductance, $g_{m,\text{MAX}}$, shows an increase of 50 mS/mm from 1050 mS/mm at $V_{GS} = -0.4\text{V}$ (before) to 1100 mS/mm at

$V_{GS} = -0.2\text{V}$ (after). At $V_{DS} = 1.0\text{V}$, in Fig. 2(a), it also has an increase of +80 mS/mm in $g_{m,\text{MAX}}$.

In terms of V_{th} , it increases after passivation in all groups, in which the Si_3N_4 passivation exhibits the maximum increase of +0.2 V. While, other passivation schemes show a smaller positive shift of $\sim+0.1\text{V}$. Such a change of the positive shift of V_{th} was also reported by Vandersinissen *et al.* [7], with its $\Delta V_{th} \simeq +100\text{mV}$ after passivation using a much thicker Si_3N_4 layer of 200 nm. And, $\Delta V_{th} \simeq +120\text{mV}$ was also reported by Dammann *et al.* [13] corroborated by the decrease of gate-to-channel distance. This change can be explained by the in-diffusion of Pt into InAlAs shottkey layer which reduced the distance between the gate metal to the InGaAs channel, known as “gate sinking”. It was initially reported by Canali *et al.* [14] showing an increased ΔV_{th} due primarily to the interdiffusion of Au into the barrier layer in Auger composition in-depth profile [14], followed by the equation (1).

$$V_{th} = \phi_B + \frac{E_{F0}}{q} - \frac{q \cdot n_D \cdot d}{\epsilon} - \frac{\Delta E_C}{q} \quad (1)$$

where ϕ_B is the shottkey barrier potential; E_{F0} is the fermi-level at zero 2-DEG density; n_D is the ionized donor charge; d is the distance between gate metal to channel; ΔE_C is the conduction band discontinuity of heterojunction. In addition, it is more interesting to note that inserting an Al_2O_3 layer can make this change even smaller, as shown in Fig. 3(a) and (b). Also, if we consider an ultra-short nanodevice, as the critical dimension is geometrically scaled, the effect of semiconductor properties, e.g., doping, on threshold voltage of any conventional devices can be largely changed, as reported in [15]. And, there might seem to have multiple reasons on getting different V_{th} and ΔV_{th} for different structures.

For the peak transconductance, an increase of $g_{m,\text{MAX}}$ can be observed among all groups after passivation except in group_4($\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$). As shown in equation (2), the $g_{m,\text{MAX}}$ is synergistically affected by carrier density (n_s), carrier mobility, and parasitic resistance (R_S). The carrier mobility will be reduced as well as the emerging parasitic resistance caused by long-term high-stress-intensity ion bombardment during the Si_3N_4 film deposition process, resulting in a decrease in $g_{m,\text{MAX}}$. In our case, the side effect can be effectively circumvented by using a $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ stack layer passivation. So, an increment of $g_{m,\text{MAX}}$, is achieved.

$$g_m = \frac{\epsilon \cdot v_{sat} \cdot W}{d} \quad (2)$$

In Fig. 3, it shows the shifts in DC parameters at $V_{DS} = 1.5\text{V}$, and $V_{DS} = 1.0\text{V}$. As for the drain current, I_{DS} , it increases at the same effective gate bias after passivation using Si_3N_4 , $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ and Al_2O_3 at $V_{DS} = 1.0\text{V}$ with the increment of +40 mA/mm, +87 mA/mm and +38 mA/mm, respectively. At $V_{DS} = 1.0\text{V}$, the maximum increase of I_{DS} can be observed in group_2 using $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation. With respect to the peak of

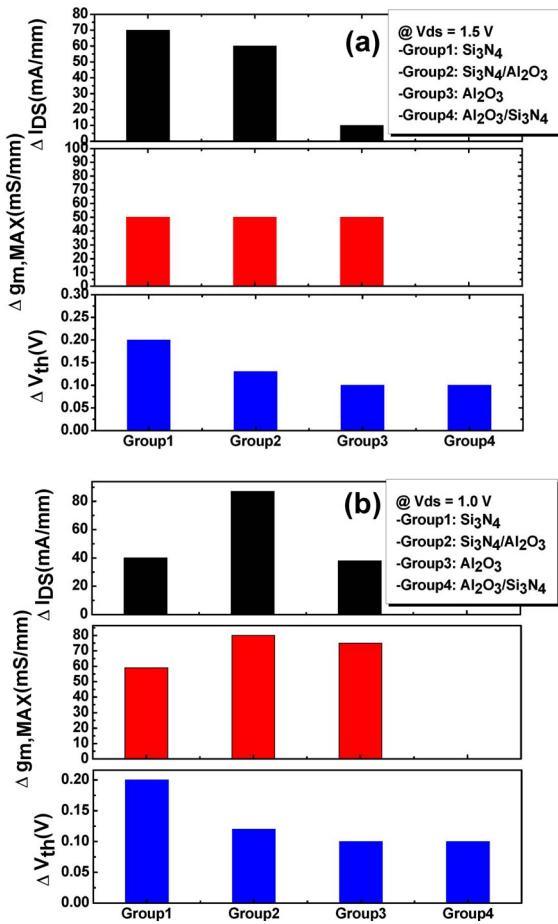


FIGURE 3. A summary of the shifts in DC parameters at (a) $V_{DS} = 1.5\text{V}$, and (b) $V_{DS} = 1.0\text{V}$.

transconductance ($g_{m,\text{MAX}}$), at $V_{DS} = 1.0\text{ V}$, it exhibits an increase of +80 mS/mm after passivated via $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$, which is the biggest increase of the $g_{m,\text{MAX}}$.

B. RF CHARACTERISTICS AND SMALL-SIGNAL MODELING

RF measurement has been carried out for all HEMTs before and after passivation. Their small-signal parameters have been extracted and plotted by modelling, as shown in Fig. 4. Before measurement, an Open-Short method is used to exclude the parasitic pad capacitances and inductances. Fig. 4(a) and (b) plot the current gains (H_{21}), Maximum Available Gain (MAG/MSG) and Mason's unilateral gain (U_g) against millimeter frequency at $V_{DS} = 1.4\text{ V}$ and $V_{GS} = -0.3\text{ V}$, where the maximum f_{max} is obtained for the $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivated HEMTs in group_2. The f_t and $f_{\text{max},\text{MAX}}$ are obtained by extrapolating the curve of H_{21} and U_g followed by a slope of -20 dB/dec, when stable factor k exceeds to 1 respectively. The measured and simulated curves are fitted well in Smith chart, showing a good extrapolation. Note that, before passivation, f_t and $f_{\text{max},\text{MAX}}$ are 179 GHz and 336 GHz. After passivation, f_t is decreased to 166 GHz, while $f_{\text{max},\text{MAX}}$ is increased to 340 GHz. In

Fig. 4(c), the variation of $f_{\text{max},\text{MAX}}$ and f_t before and after passivation is plotted for all groups. It is interesting to note that f_t shows a decrease after passivation regardless of the passivated layers used. However, in the case of $f_{\text{max},\text{MAX}}$, except for $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ passivation in group_4, it increases for the rest of groups after passivation with the maximum increase of 10 GHz for the Si_3N_4 passivation in group_1 and 4 GHz for the $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation in group_2.

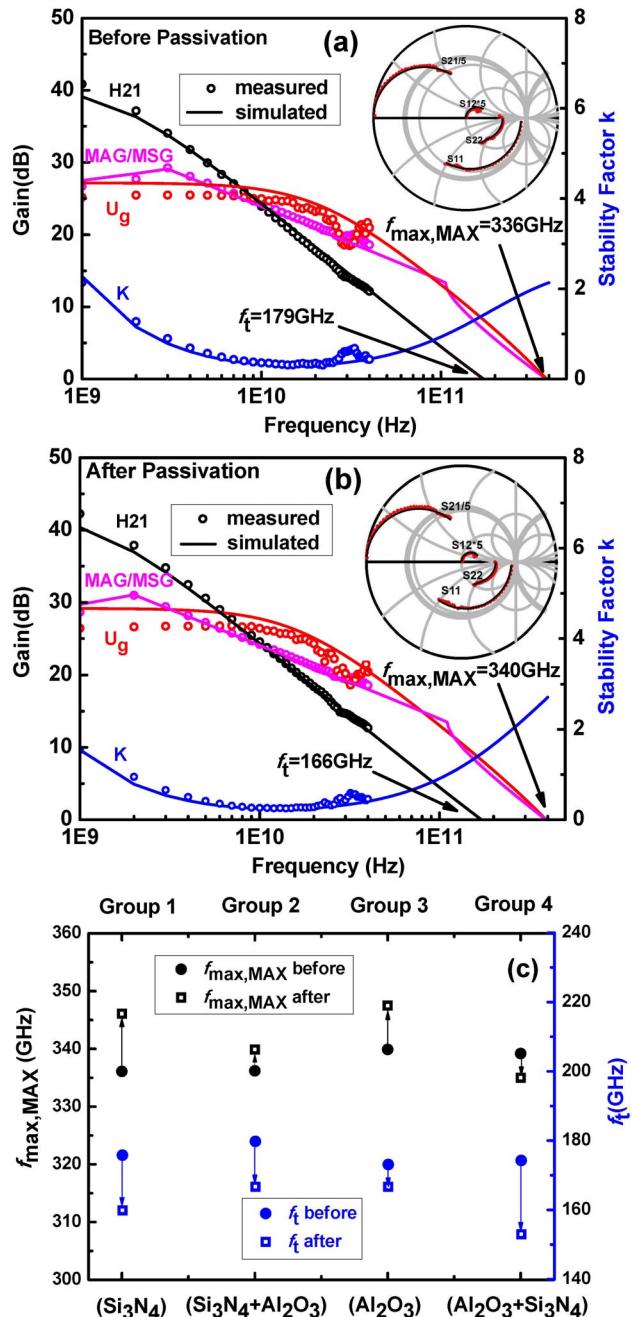


FIGURE 4. RF characteristics of the HEMTs at $V_{DS} = 1.4\text{ V}$ and $V_{GS} = -0.3\text{ V}$, (a) before $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation, and (b) after $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ passivation; (c) The dependence of the value of cutoff frequency, f_t , and the peak maximum oscillation frequency, $f_{\text{max},\text{MAX}}$, on different passivation.

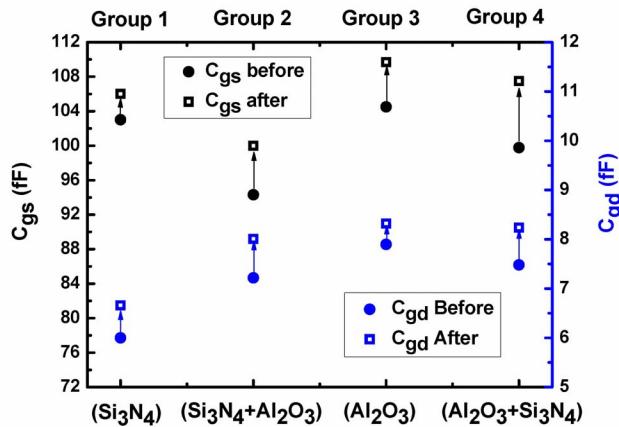


FIGURE 5. The extracted parameters of C_{gs} and C_{gd} based on the small-signal modeling at bias of the $f_{max,MAX}$.

To explain the variation of RF performance among different passivations, the parameters of C_{gs} and C_{gd} are extracted based on the small-signal modeling at a bias of the peak $f_{max,MAX}$, as shown in Fig. 5. It is found that after passivation both values show an increase in all four groups. And, in comparison of C_{gs} and C_{gd} before and after passivation, the minimum increase is obtained using a Si₃N₄ layer from 103 fF to 106 fF in C_{gs} and from 6.00 fF to 6.66 fF in C_{gd} at $f_{max,MAX}$ bias. In Si₃N₄/Al₂O₃ passivation, they are also increased simultaneously from 94.3 fF to 99.9 fF in C_{gs} and from 7.22 fF to 8.01 fF in C_{gd} . As reported by Vandersinissen *et al.*, the RF performance, however, suffers from the increased parasitic capacitances, such as C_{gs} and C_{gd} . In this work, it can be noted that after passivation in all cases of using the Si₃N₄ and Al₂O₃, the value of C_{gs} and C_{gd} increases due to the high dielectric constant of Si₃N₄ ($\epsilon_{Si_3N_4} = 7$) and Al₂O₃ ($\epsilon_{Al_2O_3} = 8.2$). This is consistent with what was reported in [7]. Plus, as shown in Fig. 5, the experimental results show higher capacitance for Si₃N₄/Al₂O₃ as opposed to Si₃N₄ because the net capacitance per unit area for the first case is given as:

$$C_{Si_3N_4/Al_2O_3} = \frac{\epsilon_{Si_3N_4}}{T_{Si_3N_4} + T_{Al_2O_3} \frac{\epsilon_{Si_3N_4}}{\epsilon_{Al_2O_3}}}$$

which is greater than the capacitance per unit area for Si₃N₄ passivation of the same thickness, as shown here:

$$C_{Si_3N_4} = \frac{\epsilon_{Si_3N_4}}{T_{Si_3N_4} + T_{Al_2O_3}}$$

because of the relative magnitudes of the permittivity. In addition, the profile of electrical field presented in the channel may also be varied in the stacked passivation. As reported in [16], the negative charges in the passivation layer could readily modulate the electric field distribution in the channel, introducing little parasitic capacitance. With respect to the stacked Si₃N₄/Al₂O₃ passivation, there exists a number of positive bulk fixed charges and negative interfacial fixed charges in ALD-deposited Al₂O₃ [17] which will remodulate the profile of the electric field induced by Si₃N₄,

resulting in a variation of parasitic capacitance in InP-based HEMTs.

IV. CONCLUSION

In this work, a novel surface passivation scheme utilizing Si₃N₄/Al₂O₃ stack layers for InAlAs/InGaAs InP-based HEMTs is reported. The Si₃N₄/Al₂O₃ passivated HEMTs exhibit a good DC and RF performances with a high drain current (I_{DS}), an increase in extrinsic transconductance (g_m) and a small positive threshold voltage shift (ΔV_{th}). For RF performance, after passivation the peak Maximum Oscillation Frequency ($f_{max,MAX}$) of HEMTs passivated by Si₃N₄/Al₂O₃ shows an increase up to 340 GHz. The RF performance is analyzed by a small signal modeling based on measured S-parameters. And, a physical explanation is addressed over why the good DC and RF performances have been achieved.

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