Received 3 July 2017; revised 27 August 2017, September 29 2017, and 28 October 2017; accepted 29 October 2017. Date of publication 3 November 2017; date of current version 26 April 2018. The review of this paper was arranged by Editor H. Wakabayashi.

Digital Object Identifier 10.1109/JEDS.2017.2769682

Punch-Through Stop Doping Profile Control via Interstitial Trapping by Oxygen-Insertion Silicon Channel

HIDEKI TAKEUCHI[1] (Member, IEEE), ROBERT J. MEARS[1] (Member, IEEE), ROBERT J. STEPHENSON[1] (Senior Member, IEEE), MAREK HYTHA[1] (Senior Member, IEEE), DANIEL CONNELLY[1] (Member, IEEE), PAVEL FASTENKO[2] (Member, IEEE), RICHARD BURTON[1] (Member, IEEE), NYLES W. CODY[1] (Member, IEEE), DORAN WEEKS[1] (Member, IEEE), DMITRI CHOUTOV[1] (Member, IEEE), NIDHI AGRAWAL[3] (Member, IEEE), AND SUMAN DATTA[4] (Fellow, IEEE)

1 Atomera Inc., Los Gatos, CA 95032, USA
2 Synopsys Inc., Mountain View, CA 94043, USA
3 Micron Technology Inc., Boise, ID 83716, USA
4 University of Notre Dame, Notre Dame, IN 46556, USA

CORRESPONDING AUTHOR: H. TAKEUCHI (e-mail: htakeuchi@atomera.com)

ABSTRACT Interstitial trapping by oxygen-inserted silicon channel results in blocking of boron and phosphorus transient enhanced diffusion as well as retention of channel boron profiles during the gate oxidation process. The enhanced doping profile control capability is applicable to punch-through stop of advanced CMOS devices and its benefits to 28 nm planar CMOS and 20 nm bulk FinFET devices projected by TCAD are discussed.

INDEX TERMS Oxygen-inserted silicon, transient-enhanced diffusion, CMOS, FinFET.

I. INTRODUCTION

OI (oxygen-inserted) silicon technology, in which partial monolayers of oxygen atoms are incorporated during silicon epitaxy [1], [2], has been shown to achieve unique characteristics such as simultaneous e^- and h^+ mobility improvement, gate leakage reduction, GOI improvements and SSR (super-steep retrograde) channel formation leading to Vt variability reduction [1]–[6]. The OI silicon film is epitaxially grown in a low-temperature epi process (≤800°C). Improved Ieff-Ioff characteristics in a 65nm technology [4] have been experimentally verified, indicating that the quality of the OI silicon is comparable to that of silicon material being used in an advanced manufacturing environment.

We reported an important additional doping profile control capability. It is experimentally demonstrated that trapping of silicon interstitials by the OI layer leads to suppression of interstitial-mediated diffusion of boron and phosphorus [7]. A new process TCAD model was developed to describe the experimental dopant diffusion behavior by taking into account trapping of interstitials by the OI layer.

The observed doping profile control feature is applicable to enhanced control of punch-through stop layer for planar and bulk FinFET CMOS devices. Device performance benefits projected by TCAD simulations are presented.

II. EXPERIMENTAL AND RESULTS

A. BLOCKING TED (TRANSIENT-ENHANCED DIFFUSION)

Boron and phosphorus are well known to form interstitial pairs to exhibit transient enhanced diffusion (TED) [8]. To investigate the interactions between interstitials and the OI layer, a high-energy implantation (B11 120keV with 1.4E14/cm2 at 7° tilt for boron; P31 220keV with 8.3E14/cm2 at 7° tilt for phosphorus) was performed through the OI layer, followed by a 1-hr anneal at 750°C to induce TED. Figs. 1 and 2 show boron and phosphorus SIMS profiles of the OI silicon and the control, respectively. It can be clearly seen that the 750°C anneal led to the upward

2168-6734 © 2017 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

diffusion of boron and phosphorus and that the diffusion is blocked by the OI layer thereby retaining low surface concentration whereas dopants diffuse to the top surface for the control.

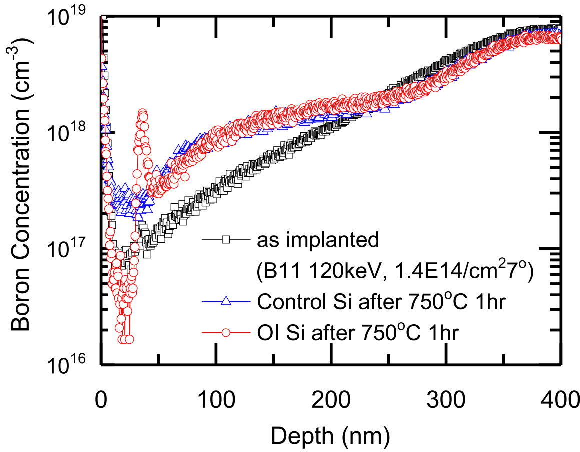


FIGURE 1. Boron depth profiles after implantation and after 750C 1 hr anneal for the control and OI Si.

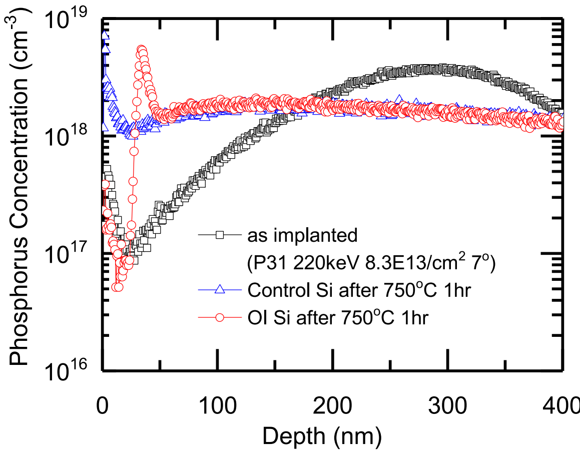


FIGURE 2. Phosphorus depth profiles after implantation and after 750C 1 hr anneal for the control and OI Si.

B. CHANNEL DOPING PROFILE CHANGE BY GATE OXIDATION AND SUBSEQUENT ANNEALS

TED is triggered by interstitial injection during thermal oxidation processes as well. Diffusion behavior of boron underneath the OI layer during oxidation process was studied.

For sample preparation, after growth of screen oxide (80A), B11+ was implanted at 25 keV with 2E13 at/cm^2, followed by well RTA at 1050°C for 5seconds. After oxide removal, OI layer followed by 20nm undoped silicon layer was epitaxially grown. For control, the OI layer was replaced with undoped Si with the same thickness. Then, samples received 125A oxidation at 800°C for 60min. followed by 850°C 30min post-oxidation anneal. After RTA at 1000°C for 2minutes, boron profiles were measured by SIMS.

Figs. 3 and 4 show boron profiles of undoped epi silicon with and without the OI layer. Whereas the non-OI epi film resulted in a reduction of boron peak concentration and deeper tail profiles after thermal processing, almost no profile change near the peak and the tail region was observed for the OI epi film. Also, whereas the non-OI epi film resulted in mid-E17 cm^{-3} surface boron concentration after gate oxidation and subsequent RTA, the OI epi film retained low surface boron concentration of 1 to 2E16cm^{-3} from the peak of 9E17cm^{-3} located at 16nm depth with steepness of 8nm/dec. after the same thermal processing. The observed differences are attributed to suppression of TED via trapping of interstitials by the OI layer.

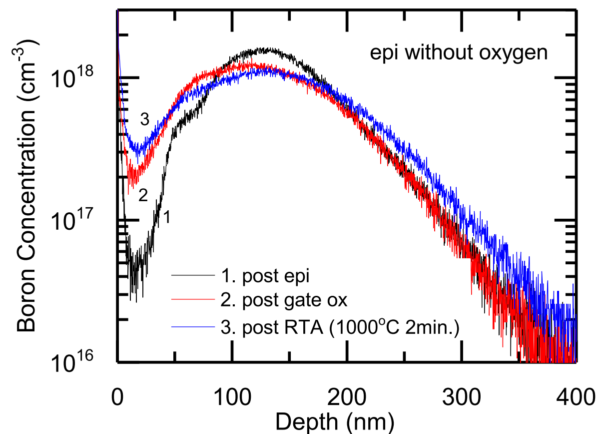


FIGURE 3. Boron depth profiles: 1. after implantation (B11 25keV, 2E13/cm^2, 0°) and undoped epi Si growth(20nm); 2. after 800C 60min and 850C 30min. gate oxidations; 3. 1000°C 2min anneal.

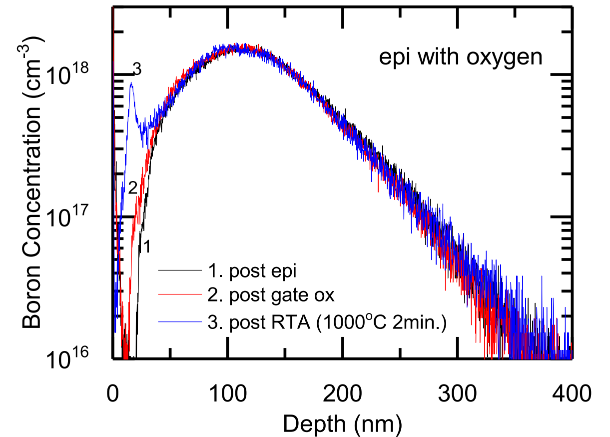


FIGURE 4. Boron depth profiles: 1. after implantation (B11 25keV, 2E13/cm^2, 0°) and undoped epi Si growth with the OI layer (20nm); 2. after 800C 60min and 850C 30min. gate oxidations; 3. 1000°C 2min anneal.

III. MODELING DOPANT DIFFUSION BEHAVIOR WITH INTERSTITIAL BLOCKING

We have implemented a Process TCAD model to help model and explain the creation of the punch-through stop layer. The

model uses Sentaurus Process Alagator API [9] to describe the interaction of the OI layer with implanted Boron and Phosphorus dopants under 750°C TED anneal as described in Section II-A. The TED broadened profile below the OI layer was found to be well-modelled by TCAD Sentaurus Advanced Calibration parameters with minimal parameter fitting. In order to capture the observed Boron profile adjacent to and above the OI layer an interface-based model with an interstitial blocking (annihilation) coefficient of 75% was developed. The modeled and experimental Boron and Phosphorus profiles are shown in Figs. 5 and 6 respectively. There is good agreement between experiment and simulation for the relatively simple interstitial blocking model. We believe that the model can be extended to simulate a wide range of engineered doping profiles using the OI technology.

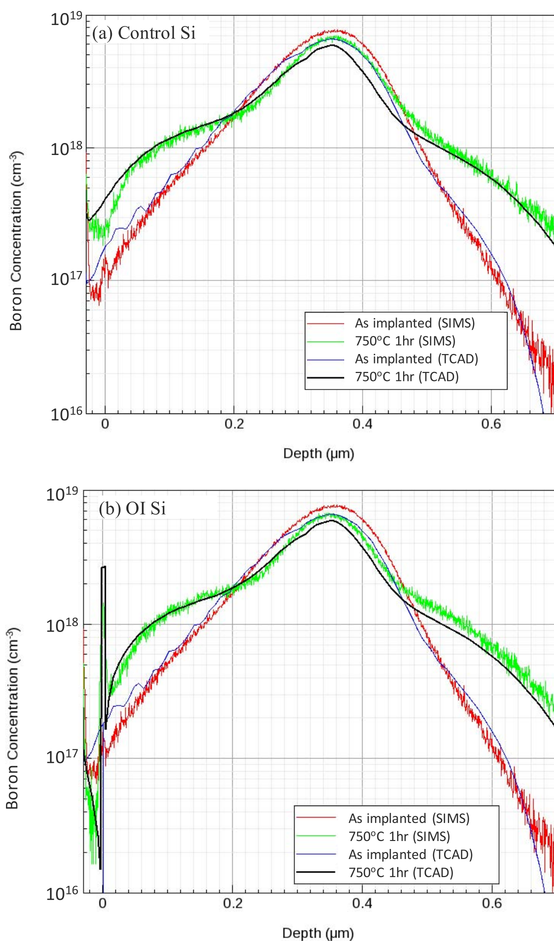


FIGURE 5. **Comparison between experimental Boron depth profile in Fig. 1 and TCAD model: (a) control Si; (b) OI Si.**

IV. APPLICATION TO PUNCH-THROUGH STOP LAYER

A. 28nm PLANAR CMOS

Interstitial trapping by the OI layer enables the precise control of a PTS (punch-through stop) layer. A halo-free SSR channel for sub-65nm CMOS devices, advantageous for variability reduction and thus for low-voltage operation [10], can be realized. To project its benefits, TCAD simulation was performed for Lg = 28nm NMOS using process conditions described in Fig. 7. Since Process TCAD model described in Section III has not been fully calibrated over a wide temperature range for different dopant species for full device fabrication process at this point, to simulate the interstitial trapping effect of the OI epi film, gate oxidation steps were replaced with deposited oxide while applying the same thermal budgets with controls since no change in the peak or tail profiles was observed as discussed in Section II-B. Undoped Si epi layer thickness was set at 10nm. Vt implant dose was adjusted for all splits to achieve the same Ioff = 100pA/um. Fig. 8 compares (a) boron profiles at the channel center (b) transfer characteristics of Lg = 28nm NMOS with and without TED by TCAD simulations. The PTS layer defined by interstitial trapping is projected to improve Ion by 13% compared to regular Si epi with TED.

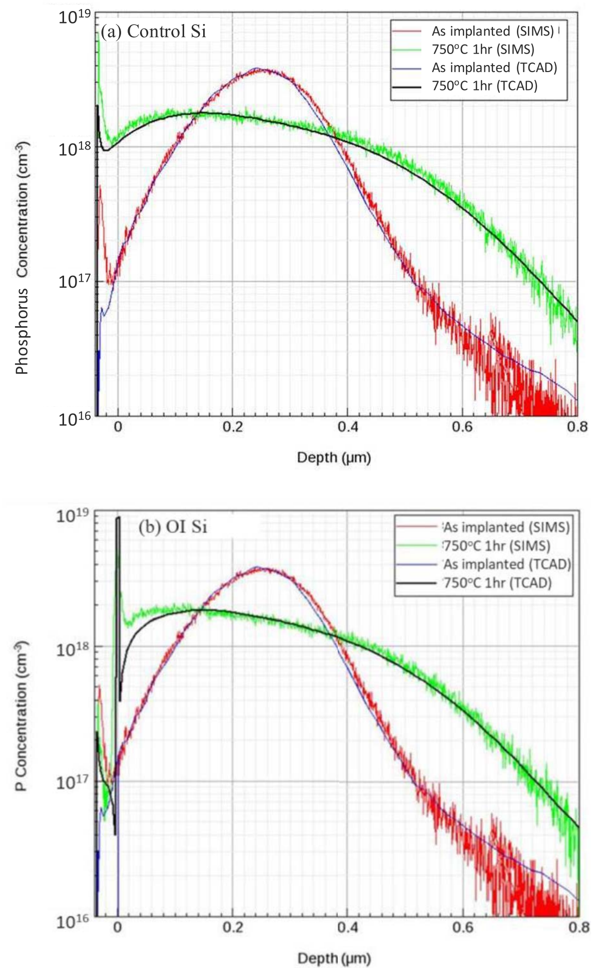


FIGURE 6. **Comparison between experimental Phosphorus depth profile in Fig. 2 and TCAD model: (a) control Si; (b) OI Si.**

B. 20nm BULK FINFET

It has been reported that undoped fin is advantageous over doped fin for FinFET performance [11]. For bulk FinFET

- Screen Oxide (8nm)
- Well implantation: B 40keV 2.5E13 +BF2 6keV dose adjusted to meet Ioff=100pA/um
- Selective Si epi (10nm)
- Gate Oxidation (splits)
  - Control: Oxide removal → 800C 30min (6nm) → oxide removal→ 1000C 30s (1.4nm)
  - No TED split: Oxide removal → Si removal (2 nm) → Oxide deposition (1.4nm)
- Gate poly Si CVD and patterning
- Poly reox (850C 1min): skip for no TED split
- Offset spacer (13nm)
- Extension implant (As 2keV 1E15) and LSA (1050C 10ms)
- Sidewall spacer
- Deep SD implant (P 3keV 3E15) and RTA(1050C 0.1s)

FIGURE 7. TCAD simulation flow of halo-free 28nm NMOS to assess impact of TED induced by oxidation processes.

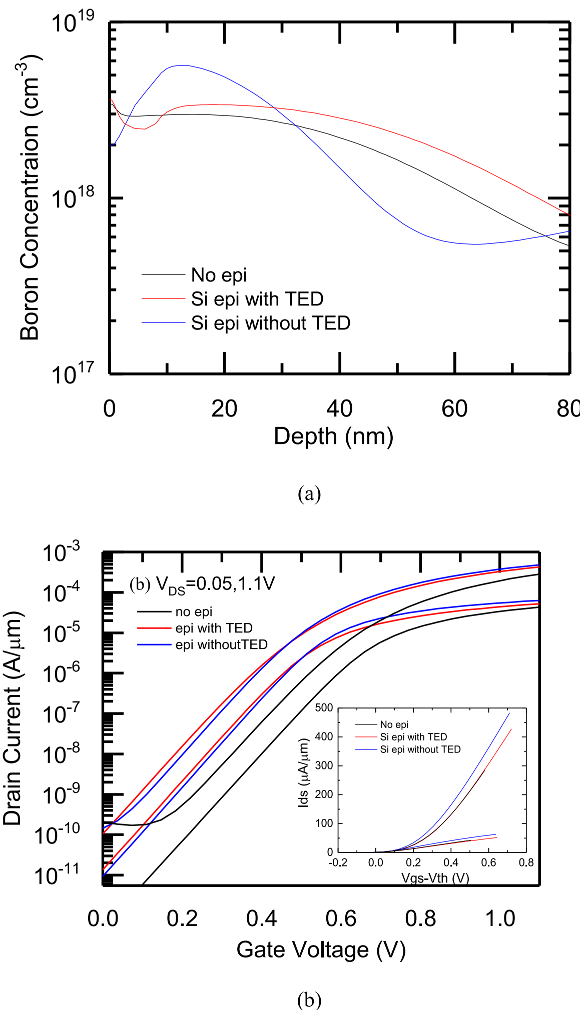


FIGURE 8. Simulated (a) channel boron profiles at the channel center and (b) transfer characteristics of Lg = 28nm NMOS for epi with and without TED during oxidation and processes and the Si control.

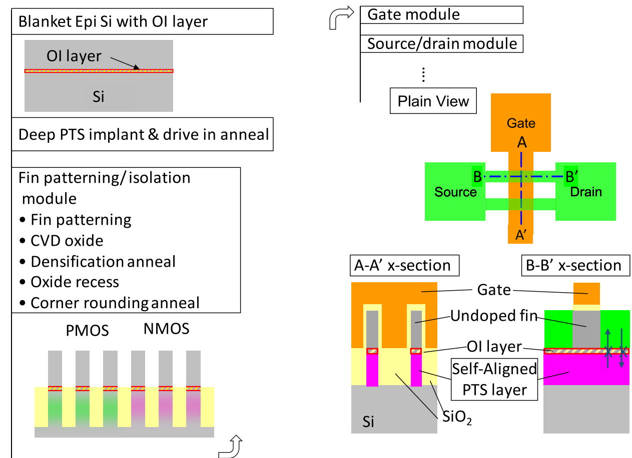


FIGURE 9. Bulk FinFET process outline using the OI layer on starting substrate.

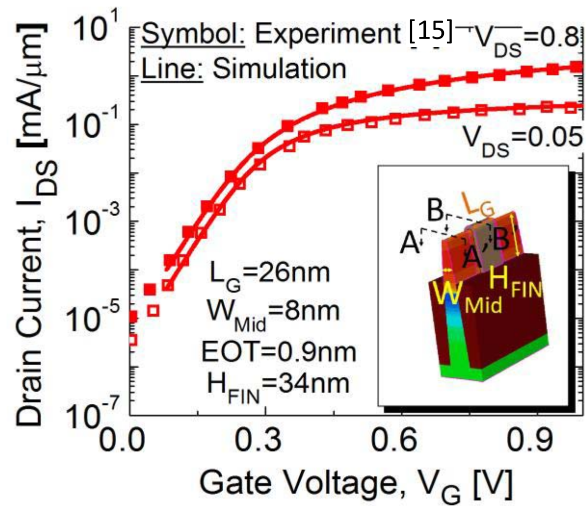
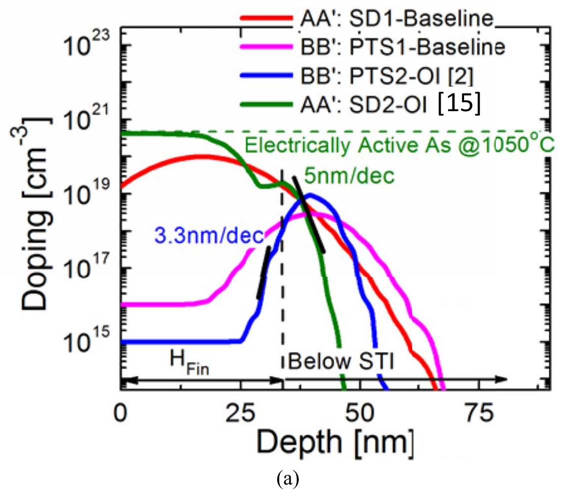


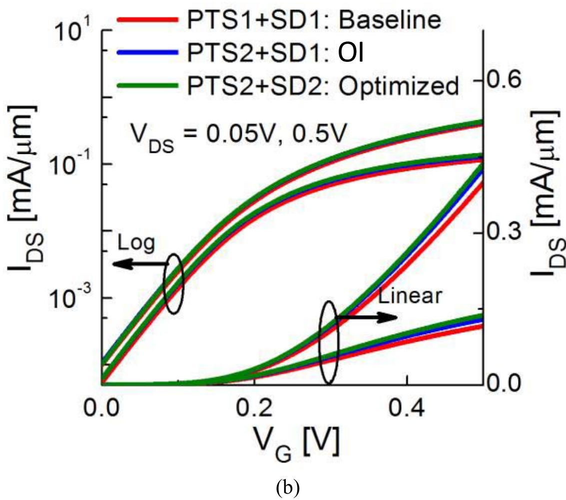
FIGURE 10. 3D numerical simulations of 22nm FinFET in excellent agreement with experimental data [15].

devices, the key challenge is the doping process of PTS layer to suppress sub fin leakage while retaining the undoped fin channel. Solid-phase diffusion after fin patterning [12], [13] and epitaxial growth of channel material after forming PTS layer [14] have been developed for this purpose. By taking advantage of the TED blocking effect, the OI silicon provides a unique process integration scheme for punch-through stop control of bulk FinFET devices by implementing the OI epi film to starting silicon substrates. The OI silicon layer blocks diffusion not only of the PTS layer but also SD (source/drain) dopants so that SD and PTS can be vertically self-aligned (Fig. 9). This allows aggressive diffusion anneals of SD dopants for series resistance reduction.

To quantify the effects of reduced fin doping and aggressive SD doping, 3D device simulation calibrated to the 22nm node n-channel FinFET [15] was performed. The nominal fin width in the middle of the fin, W_{MID}, is 8nm and the fin height, H_{FIN}, is 23nm. The physical gate length of the FinFET, L_G, is 26nm. A modified drift-diffusion model that includes non-equilibrium transport models such as field and dopant dependent mobility and velocity overshoot as well as



(a)



(b)

Electrical Parameter	(i) PTS1+SD1	(ii) PTS2+SD1 [(ii)/(i)]	(iii) PTS2+SD2 [(iii)/(i)]
Idsat (uA/um)	400	426 [1.07]	435 [1.10]
Idlin (uA/um)	115	130 [1.13]	137 [1.21]
Vtlin (mV)	169	167 [0.99]	168 [1.06]
SSlin (mV/dec)	74	71 [0.99]	74 [0.99]
SSsat (mV/dec)	79	76 [0.99]	79 [0.99]
DIBL (mV/V)	55	51 [0.99]	47 [0.85]
σVt-RDF (mV)	19.98	15.24 [0.76]	14.22 [0.71]
σVt-Total (mV)	31.6	26.8 [0.85]	26.3 [0.83]

(c)

FIGURE 11. (a) Source-drain doping profile optimization in 22nm FinFET using OI layers. (b) Transfer characteristics of PTS2 + SD2 : OI FinFET benchmarked against the 22nm baseline FinFET and the PTS2 + SD1 : OI FinFET. OI. (c) summary of TCAD simulation results.

the density gradient approximation that captures the effect of geometry induced quantization are utilized to accurately reproduce the transfer characteristics of the FinFET. The fin and the source-drain doping profile are adjusted to ensure the accurate capture of the sub-threshold, near threshold, and above threshold current vs voltage characteristics of the experimental device for both low and high drain biases. Figure 10 shows excellent match between the calibrated 3D numerical modeling results with the experimental results [15].

Figure 11 (a) B-B' lines show fin doping profiles used for the simulations. For the OI FinFET, fin doping profile (PTS1-OI) was assumed to decay from the peak of the PTS layer at 3.3nm/dec, based on experimental SIMS data obtained after gate oxidation and 1010°C 10s RTA [2]. For SD doping profile optimization, novel fin doping of Arsenic (As) using self-regulatory plasma doping (SRPD) process followed by a spike anneal at 1050°C for activation of the dopants has been characterized in detail [16]. To assess impact of SD doping profile (SD2-OI), Arsenic profiles, active dopant concentration, and their abruptness in this simulation were set to the experimental data reported in reference [16]. Figure 11 (b) and (c) compare the performance benefits of 22nm bulk FinFET projected by TCAD simulations calibrated to experimental data [15] (Fig. 10). Results of PTS2+SD1 represent performance benefits by undoped fin channel, whereas PTS2+SD2 represents additional benefits gained by SD profile optimization. OI layer (denoted by dashed vertical line) allows higher SD doping concentration (green solid line) over the baseline SD doping (red solid line) while reducing the junction depth in the sub-fin region below the STI at the same time (Fig. 11 (a)). Drain current is improved by mobility improvement by retaining undoped fin channel as well as by series resistance reduction. Reduced RDF leads to variability reduction as well. FinFET with re-optimized source-drain doping profile and punch-through implant profile provides a combined performance boost of 21% Idlin and 10% Idsat improvement at V_{DD} = 0.5V, due to reduction in external resistance and improvement in electron mobility from reduced impurity scattering. Considering RDF fluctuation as well as geometric fluctuation, OI FinFETs show 17% improvement in $\sigma V_{Th\text{-}Total}$ over baseline 22nm FinFET [15].

V. CONCLUSION

The OI silicon channel traps interstitials and thus suppresses boron and phosphorus TED. The observed interstitial trapping behavior can be modeled by advanced process TCAD. This feature is beneficial for controlling punch-through in planar and bulk-FinFET CMOS devices.

In addition to the punch-through stop doping profile control reported in this manuscript, the OI silicon has benefits of simultaneous e^- and h^+ mobility improvement, gate leakage reduction, GOI improvements and SSR channel formation. A single epi film brings multiple benefits simultaneously for NMOS and PMOS. Doping process adjustment from baseline process optimized for regular silicon, which does not trap interstitials, is the major challenge for process integration of the OI silicon.

REFERENCES

[1] R. J. Mears *et al.*, “Silicon superlattice on SOI for high mobility and reduced leakage,” in *IEEE Int. SOI Conf. Tech. Dig.*, Indian Wells, CA, USA, 2007, pp. 23–24.

[2] R. J. Mears *et al.*, "Simultaneous carrier transport enhancement and variability reduction in Si MOSFETs by insertion of partial monolayers of oxygen," in *Proc. IEEE Silicon Nanoelectron. Workshop*, Honolulu, HI, USA, 2012, pp. 33–34.
[3] N. Xu *et al.*, "MOSFET performance and scalability enhancement by insertion of oxygen layers," in *Proc. IEEE Int. Elect. Device Meeting*, San Francisco, CA, USA, 2012, pp. 127–130.
[4] N. Xu *et al.*, "Extension of planar bulk n-channel MOSFET scaling with oxygen insertion technology," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3345–3349, Sep. 2014.
[5] N. Xu *et al.*, "Electron mobility enhancement in (100) oxygen-inserted silicon channel," *Appl. Phys. Lett.*, vol. 107, Sep. 2015, Art. no. 123502.
[6] A. Marshall *et al.*, "The impact of oxygen insertion technology on SRAM yield performance," in *Proc. IEEE Elect. Devices Technol. Manuf. Conf.*, Toyama, Japan, 2017, pp. 191–192.
[7] R. J. Mears *et al.*, "Punch-through stop doping profile control via interstitial trapping by oxygen-insertion silicon channel," in *Proc. IEEE Elect. Devices Technol. Manuf. Conf.*, Toyama, Japan, 2017, pp. 65–66.
[8] P. A. Stolk *et al.*, "Physical mechanisms of transient enhanced dopant diffusion in ion-implanted silicon," *J. Appl. Phys.*, vol. 81, no. 9, pp. 6031–6050, 1997.
[9] *Sentaurus™ Process User Guide*, Synopsys Inc., Mountain View, CA, USA, 2016.
[10] K. Fujita *et al.*, "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications," in *Proc. IEEE Int. Elect. Devices Meeting*, Washington, DC, USA, 2011, pp. 32.3.1–32.3.4.
[11] K.-I. Seo *et al.*, "A 10nm platform technology for low power and high performance application featuring FINFET devices with multi workfunction gate stack on bulk and SOI," in *Symp. VLSI Tech. Dig.*, Honolulu, HI, USA, 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894342.
[12] S. Natarajan *et al.*, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," in *IEEE Int. Elect. Device Meeting Tech. Dig.*, San Francisco, CA, USA, 2014, pp. 3.7.1–3.7.3.
[13] Y. Kikuchi *et al.*, "Electrical characteristics of p-type bulk Si fin field-effect transistor using solid-source doping with 1-nm phosphosilicate glass," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1084–1087, Sep. 2016.
[14] R. Xie *et al.*, "A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels," in *IEEE Int. Elect. Devices Meeting Tech. Dig.*, San Francisco, CA, USA, 2016, pp. 47–50.
[15] C. Auth *et al.*, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. Symp. VLSI Technol.*, Honolulu, HI, USA, 2012, pp. 131–132.
[16] A. K. Kambham, A. Kumar, A. Florakis, and W. Vandervorst, "Three-dimensional doping and diffusion in nano scaled devices as studied by atom probe tomography," *Nanotechnology*, vol. 4, no. 7, 2013, Art. no. 275705.

HIDEKI TAKEUCHI, photograph and biography not available at the time of publication.

ROBERT J. MEARS, photograph and biography not available at the time of publication.

ROBERT J. STEPHENSON, photograph and biography not available at the time of publication.

MAREK HYTHA, photograph and biography not available at the time of publication.

DANIEL CONNELLY, photograph and biography not available at the time of publication.

PAVEL FASTENKO, photograph and biography not available at the time of publication.

RICHARD BURTON, photograph and biography not available at the time of publication.

NYLES W. CODY, photograph and biography not available at the time of publication.

DORAN WEEKS, photograph and biography not available at the time of publication.

DMITRI CHOUTOV, photograph and biography not available at the time of publication.

NIDHI AGRAWAL, photograph and biography not available at the time of publication.

SUMAN DATTA, photograph and biography not available at the time of publication.