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Quadruple Gate-Embedded T Structured GaN-Based Metal–Oxide–Semiconductor High-Electron Mobility Transistors

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ABSTRACT In this paper, high performance quadruple gate-embedded T structured GaN-based metal–oxide–semiconductor high-electron mobility transistors (MOSHEMTs) were fabricated using laser interference photolithography method and photoelectrochemical oxidation method, in which polymethylmethacrylate was used as sacrificial layer. The associated drain-source saturation current was improved to 175 mA/mm and the gate leakage current at the gate-source voltage of −80 V was improved to 0.81 μA compared with the 125 mA/mm and 7.6 μA of the conventional single gate GaN-based MOSHEMTs, respectively. Moreover, the associated maximum extrinsic transconductance of the quadruple gate-embedded T structured GaN-based MOSHEMTs was enhanced from 97.3 mS/mm to 118.4 mS/mm. Besides, the associated unit gain cutoff frequency and the associated maximum oscillation frequency were improved from 7.6 GHz to 10.8 GHz and from 11.4 GHz to 27.4 GHz, respectively. The improved performances of the quadruple gate-embedded T structure GaN-based MOSHEMTs were attributed to the function of the gate length reduction and the gate resistance decrease.

INDEX TERMS GaN-based metal-oxide-semiconductor high-electron mobility transistors, laser interference photolithography method, photoelectrochemical oxidation method, polymethylmethacrylate sacrificial layer, quadruple gate-embedded T structure.

I. INTRODUCTION

Recently, in view of the progress of epitaxial growth and fabrication techniques, gallium nitride (GaN)-based materials have been widely utilized in various electronic devices, optoelectronic devices and sensors [1]–[3]. Among the GaN-based electronic devices, the high-electron mobility transistors (HEMTs) were intensively developed for applying in high-power systems and high-frequency systems owing to the high electron mobility of the two-dimensional electron gas (2-DEG) induced in the interface between the AlGaN layer and the GaN layer [4], [5]. In order to improve the performances of the GaN-based HEMTs, the scaled down gate length, the reduced distance between the gate and the channel, and the minimized parasitic resistance and parasitic capacitance were widely utilized [6], [7]. It is well understood that the unit gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) of the field-effect transistors (FETs) can be improved by reducing the gate resistance, the gate-drain capacitance, and the gate length. However, the gate resistance increased with a reduction of the gate length [8]. To reduce the gate resistance, the T-gate structured and the mushroom-gate structured metal-oxide-semiconductor high-electron mobility transistors (MOSHEMTs) were proposed, previously [9], [10]. However, the unit gain cutoff frequency would be decreased by an increase of the parasitic capacitance of the top gate metal in the T-gate structure [11]. To reduce the parasitic capacitance, the low-k support layer of the T-gate structure was reported, previously [12]. Instead of the conventional single-gate structure, the double-gate structure and the triple-gate structure were reported, previously [13], [14]. In this work, quadruple

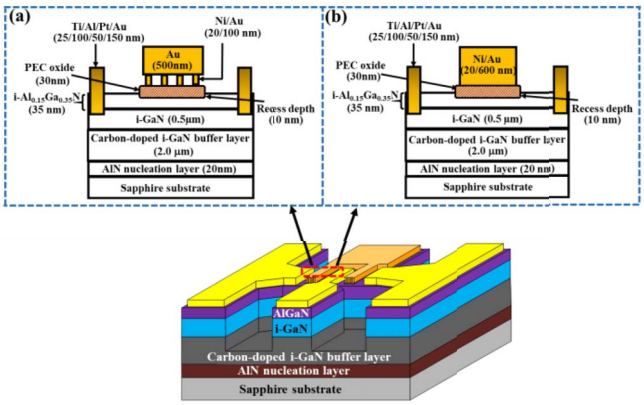

FIGURE 1. Schematic configuration of (a) quadruple gate-embedded T structured GaN-based MOSHEMTs and (b) conventional single gate GaN-based MOSHEMTs.

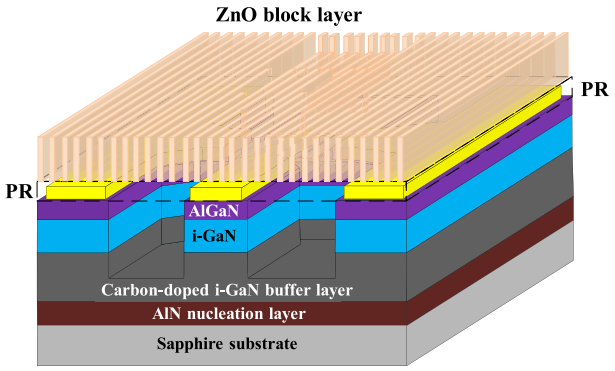

FIGURE 2. Schematic configuration of the stripped ZnO block layer on the devices.

gate-embedded T structured GaN-based MOSHEMTs were fabricated using laser interference photolithography method, photoelectrochemical (PEC) oxidation method, and polymethylmethacrylate (PMMA) sacrificial layer. In view of high volatility of the PMMA at a high temperature, the PMMA was used as sacrificial layer. When the PMMA sacrificial layer was removed, the gate parasitic capacitance could be reduced by the low k of air formed in the quadruple gate-embedded T structured GaN-based MOSHEMTs. In this work, the direct current (DC) and the high frequency performances of the quadruple gate-embedded T structured GaN-based MOSHEMTs were measured and analyzed.

II. EXPERIMENTAL PROCEDURE

Figure 1 (a) and (b) shows the schematic diagram of the quadruple gate-embedded T structured GaN-based MOSHEMTs and the conventional single gate GaN-based MOSHEMTs. In this work, an ammonia molecular beam epitaxial system was used to sequentially grow a 20-nm-thick AlN nucleation layer, a 2.0-μm-thick carbon-doped i-GaN buffer layer, a 0.5-μm-thick undoped i-GaN layer, and a 35-nm-thick undoped $Al_{0.15}Ga_{0.85}N$ layer on c-plane sapphire substrates. Using a Hall measurement system at room temperature, the sheet electron density and the electron mobility of the 2-DEG were $1.12\times10^{13}cm^{-2}$ and 1700 cm^2/Vs, respectively. To fabricate mesa regions of the conventional single gate GaN-based MOSHEMTs and the quadruple gate-embedded T structured GaN-based MOSHEMTs, the BCl_3 etchant in a reactive ion etching system was utilized to etch and make mesa regions, in which the mesa isolation area was 310 μm × 310 μm. Furthermore, to completely remove the undesired native oxide resided on the surface of the undoped AlGaN layer, the samples were then dipped into an $(NH_4)_2S_x$(S=6%) solution at 60 °C for 30 minutes [15], [16]. After the surface treatment process, a standard photolithography method was used to pattern the source regions and the drain regions of the GaN-based MOSHEMTs. Multilayer metals of Ti/Al/Pt/Au (25/100/50/150 nm) were deposited as the source electrode and the drain electrode using an electron-beam evaporator. Moreover, to form ohmic contact, the samples were then thermally annealed in a N_2 ambient rapid thermal anneal system at 850 °C for 3 minutes. To minimize the interface states, the PEC oxidation method was used to directly oxidize the gate region. During the PEC oxidation process, the light source of He-Cd laser (wavelength=325 nm and power density=10.0 mW/cm^2) illuminated on the sample which was dipped into the electrolytic solution of H_3PO_4 solution (pH=3.5). When the oxidized layer was thermally annealed in an O_2 ambient furnace at 700 °C for 2 hours, a 30-nm-thick high quality mixed β-Ga_2O_3 and α-Al_2O_3 gate insulator with ultralow interface state density was obtained [17]. After using a standard photolithography method to open the gate region, a 50-nm-thick ZnO block layer was deposited by a radio frequency (RF) magnetron sputter system. Using two intersected He–Cd laser beams in the laser interference photolithography system, an interference fringe pattern (strip width = 200 nm and strip spacing = 350 nm) was exposed and formed. After developing processes, a diluted H_3PO_4 solution (H_3PO_4:Deionized water = 1:200) was utilized to etch the ZnO block layer. The resulting configuration is shown in Fig. 2. A 20/100-nm-thick Ni/Au metals were deposited using an electron-beam evaporator system. The deposited Ni/Au metals would fill into the space among the ZnO strips. After using lift-off process of the ZnO film, a set of quadruple Ni/Au gate strip (strip width = 200 nm and strip spacing = 350 nm) was fabricated on the PEC oxidized gate insulator region. Moreover, to prevent the ungated regions covered by the consecutively spun PMMA sacrificial layer, an AZ6112 photoresist (PR) layer was first spread and then the window of the gate regions was opened using a self-aligned technique. When the PMMA sacrificial layer was spun, the spaces among the Ni/Au strips were filled by the PMMA as a support layer. After the PMMA sacrificial layer on the top area of the Ni/Au strips was removed using an oxygen plasma, a 500-nm-thick Au metal was deposited using the electron-beam evaporator system. After lift-off the

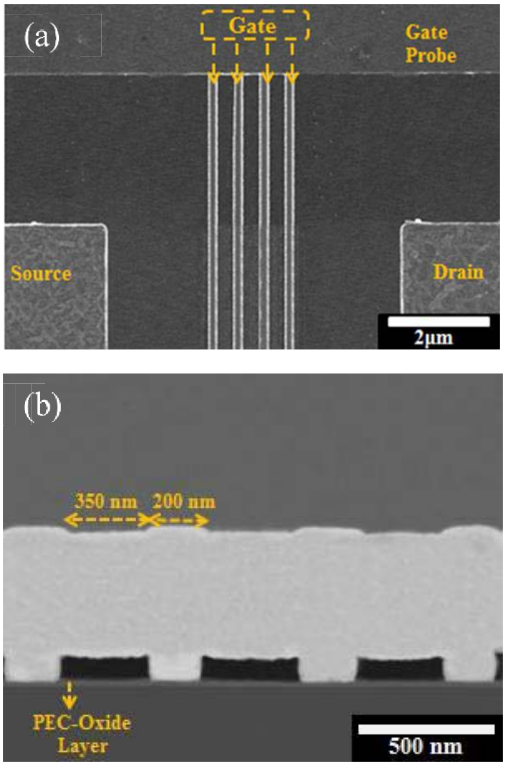

FIGURE 3. The SEM images of (a) top view and (b) cross section of quadruple gate-embedded T structured GaN-based MOSHEMTs.

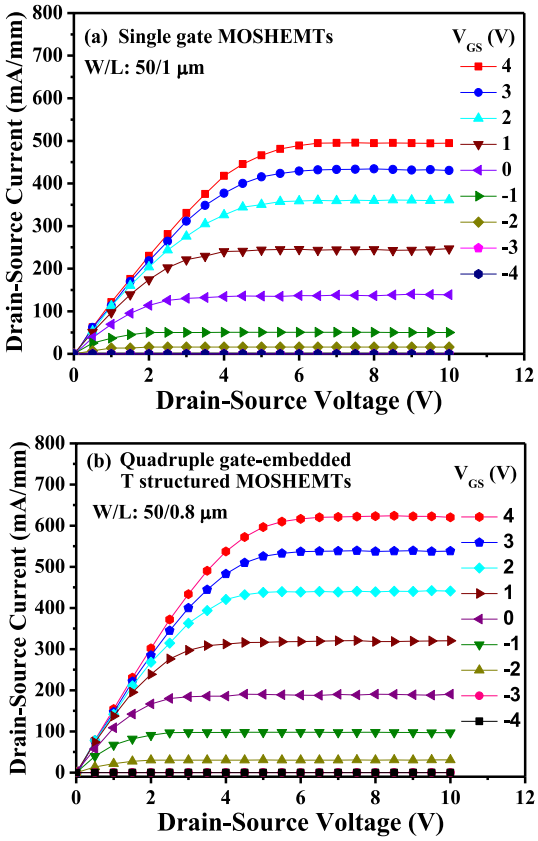

FIGURE 4. Drain-source current-drain-source voltage characteristics of (a) conventional single gate GaN-based MOSHEMTs and (b) quadruple gate-embedded T structured GaN-based MOSHEMTs.

PMMA sacrificial layer resided on the ungated region, the PMMA remained within among the Ni/Au metal strips was then completely removed in an air ambient furnace at 250°C for 1 hour. Finally, the GaN-based MOSHEMTs with two finger gates, in which each finger gate was constructed by the quadruple gate-embedded T structure, as shown in Fig. 1 (a) were fabricated. The scanning electron microscope (SEM) images of the top view and the cross section of the quadruple gate-embedded T structure are shown in Fig. 3 (a) and (b), respectively. For fabricating the conventional single gate GaN-based MOSHEMTs with two finger gates, in which each finger gate was constructed by one single gate, the gate metals of Ni/Au (20 nm/ 600 nm) were deposited and patterned using the standard fabrication process, as shown in Fig. 1 (b). The gate length and the gate width of the single gate GaN-based MOSHEMTs were 1 μm and 50 μm, respectively.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 4 (a) and (b) shows the dependence of the drain-source current (I_{DS}) on the drain-source voltage (V_{DS}) of the conventional single gate GaN-based MOHEMTs and the quadruple gate-embedded T structured GaN-based MOSHEMTs operated at various gate-source voltages (V_{GS}), respectively. The drain-source saturation current (I_{DSS}) of the former one and the latter one operated at a V_{GS} of 0 V and a V_{DS} of 6 V was 125 mA/mm and 175 mA/mm, respectively. In general, the relationship of the drain-source current I_{DS} and the gate length L in the saturation region can be expressed as:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \quad (1)$$

where W is the gate width, C_{ox} is the capacitance per unit area of the gate oxide, V_t is the threshold voltage, and μ_n is the electron mobility. It would be deduced that the enhanced drain-source saturation current of the quadruple gate-embedded T structured GaN-based MOSHEMTs was attributed to the reduction of the gate length. Furthermore, the electrons propagated through the channel would be rapidly accelerated and the short-channel effect would be suppressed by the screening effect using the multiple gate structure [18], [19]. Consequently, the higher electron drift velocity and the screening effect could cause more enhancement of the drain-source saturation current in the quadruple gate-embedded T structured GaN-based MOSHEMTs. The dependence of the drain-source current and the extrinsic transconductance (g_m) on V_{GS} of the conventional single gate GaN-based MOSHEMTs and the quadruple gate-embedded T structured GaN-based MOSHEMTs operated at $V_{DS} = 6$ V is shown in Fig. 5 (a) and (b), respectively. The maximum transconductance g_m value of the former one and the latter one was 97.3 mS/mm and 118.4 mS/mm, respectively.

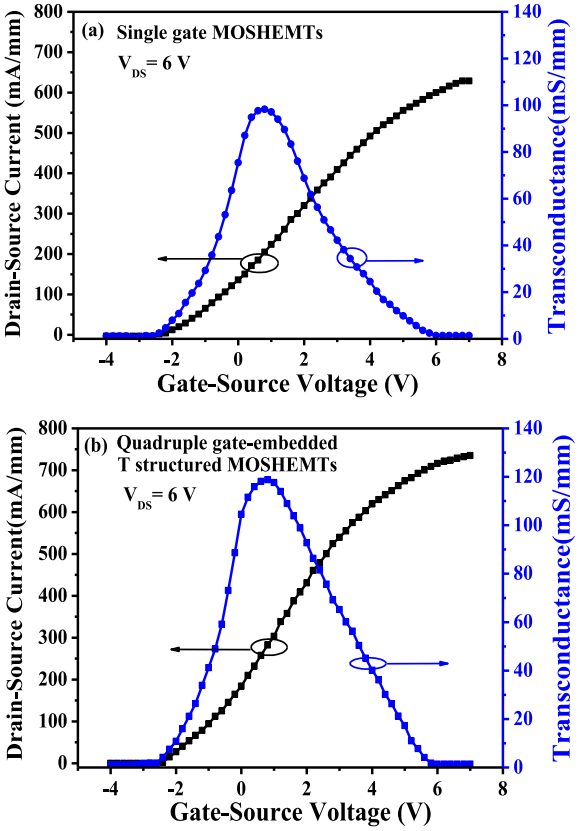

FIGURE 5. Drain-source current-gate-source voltage characteristics and extrinsic transconductance-gate-source voltage characteristics of (a) conventional single gate GaN-based MOSHEMTs and (b) quadruple gate-embedded T structured GaN-based MOSHEMTs.

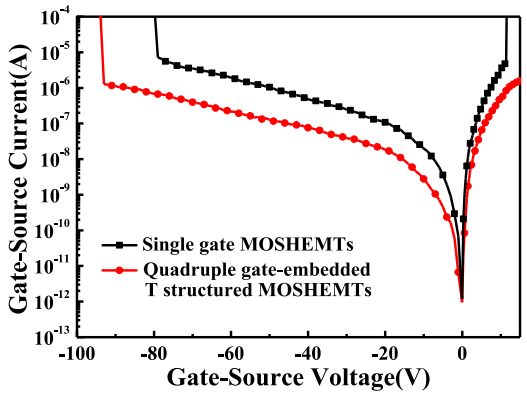

FIGURE 6. Gate–source leakage current-gate-source voltage characteristics of conventional single gate MOSHEMTs and quadruple gate-embedded T structured GaN-based MOSHEMTs.

It was worth noting that the g_m value of the quadruple gate-embedded T structured GaN-based MOSHEMTs increased due to the reduction of the gate length.

Figure 6 shows the gate-source leakage current as a function of the gate-source voltage. The gate-source leakage current of the conventional single gate GaN-based MOSHEMTs and the quadruple gate-embedded T structured GaN-based MOSHEMTs operated at a V_{GS} of −80 V was 7.6 μA and 0.81 μA, respectively. The breakdown voltage of the former one and the latter one was −81 V and −92 V, respectively. Comparing with the conventional single gate GaN-based MOSHEMTs, the leakage current of the quadruple gate-embedded T structured GaN-based MOSHEMTs was reduced about one order of magnitude due to the smaller contact area between the gate electrode and the gate oxidation layer. Compared with the conventional single gate GaN-based MOSHEMTs, the results revealed that the gate surface carrier density could be dispersed in the quadruple gate-embedded T structured GaN-based MOSHEMTs [20]. Therefore, the electron injection opportunity from the gate electrode to the channel could be effectively suppressed by the quadruple gate-embedded T structure.

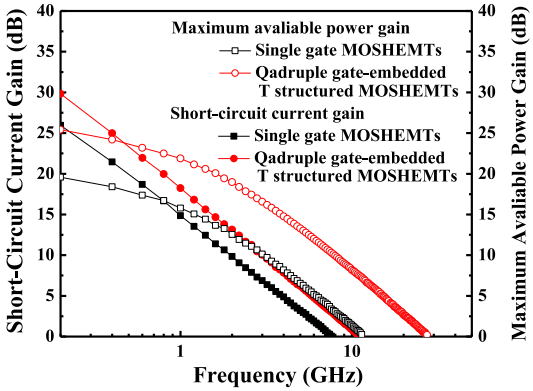

FIGURE 7. Short-circuit current gain-frequency characteristics and maximum available power gain-frequency characteristics of conventional single gate MOSHEMTs and quadruple gate-embedded T structured GaN-based MOSHEMTs.

Figure 7 shows the short-circuit current gain and the maximum available power gain as a function of frequency of the GaN-based MOSHEMTs derived from the S-parameters measured at a V_{DS} of 6 V using an Agilent 8510C network analyzer. The unit gain cutoff frequency f_T and the maximum oscillation frequency f_{max} of the conventional single gate GaN-based MOSHEMTs were 7.6 GHz and 11.4 GHz, respectively. However, the unit gain cutoff frequency f_T and the maximum oscillation frequency f_{max} of the quadruple gate-embedded T structured GaN-based MOSHEMTs were improved to 10.8 GHz and 27.4 GHz, respectively. The enhanced f_T and f_{max} of the quadruple gate-embedded T structured GaN-based MOSHEMTs were attributed to the improved maximum transconductance g_m value, the reduced gate resistance and the reduced gate capacitance.

IV. CONCLUSION

In this study, the quadruple gate-embedded T structured GaN-based MOSHEMTs were fabricated using laser interference photolithography method, photoelectrochemical oxidation method, and PMMA sacrificial layer. The DC performances of the resulting devices were improved by the novel gate structure. Compared the quadruple gate-embedded T structured GaN-based MOSHEMTs with the conventional

single gate GaN-based MOSHEMTs, the drain-source saturation current was enhanced from 125 mA/mm to 175 mA/mm, the breakdown voltage was improved from −81 V to −92 V, the gate leakage current operated at a V_{GS} of −80 V was reduced from 7.6 μA to 0.81 μA, the maximum transconductance was enhanced from 97.3 mS/mm to 118.4 mS/mm, the unit gain cutoff frequency was enhanced from 7.6 GHz to 10.8 GHz, and the maximum oscillation frequency was enhanced from 11.4 GHz to 27.4 GHz. According to the experimental results, the novel quadruple gate-embedded T structure can be expected as the promising structure candidate in high performance semiconductor devices.

REFERENCES

[1] C.-T. Lee, C.-L. Yang, C.-Y. Tseng, J.-H. Chang, and R.-H. Horng, "GaN-based enhancement-mode metal–oxide–semiconductor high-electron mobility transistors using $LiNbO_3$ ferroelectric insulator on gate-recessed structure," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 2481–2487, Aug. 2015.

[2] C.-T. Lee *et al.*, "Color conversion of GaN-based micro light-emitting diodes using quantum dots," *IEEE Photon. Technol. Lett.*, vol. 27, no. 21, pp. 2296–2299, Nov. 2015.

[3] C.-T. Lee, Y.-S. Chiu, and X.-Q. Wang, "Performance enhancement mechanisms of passivated InN/GaN-heterostructured ion-selective field-effect-transistor pH sensors," *Sensors Actuator B Chem.*, vol. 181, pp. 810–815, May 2013.

[4] P. Javorka *et al.*, "AlGaN/GaN HEMTs on (111) silicon substrates," *IEEE Electron Device Lett.*, vol. 23, no. 1, pp. 4–6, Jan. 2002.

[5] J. Liu *et al.*, "DC and RF characteristics of AlGaN/GaN/InGaN/GaN double-heterojunction HEMTs," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 2–10, Jan. 2007.

[6] Y.-L. Chiou, L.-H. Huang, and C.-T. Lee,"Photoelectrochemical function in gate-recessed AlGaN/GaN metal–oxide–semiconductor high-electron-mobility transistors," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 183–185, Mar. 2010.

[7] E.-Y. Chang, C.-I. Kuo, H.-T. Hsu, C.-Y. Chiang, and Y. Miyamoto, "InAs thin-channel high-electron-mobility transistors with very high current-gain cutoff frequency for emerging submillimeter-wave applications," *Appl. Phys. Exp.*, vol. 6, no. 3, pp. 1–3, Feb. 2013.

[8] J. Mateos, T. González, D. Pardo, V. Hoel, and A. Cappy, "Effect of the T-gate on the performance of recessed HEMTs. A Monte Carlo analysis," *Semicond. Sci. Technol.*, vol. 14, no. 9, pp. 864–870, 1999.

[9] Y. Murase *et al.*, "T-shaped gate GaN HFETs on Si with improved breakdown voltage and f_{MAX}," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 524–526, May 2014.

[10] D. S. Lee *et al.*, "245-GHz InAlN/GaN HEMTs with oxygen plasma treatment," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 755–757, Jun. 2011.

[11] R. Thompson, T. Prunty, V. Kaper, and J. R. Shealy, "Performance of the AlGaN HEMT structure with a gate extension," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 292–295, Feb. 2004.

[12] X. Lu *et al.*, "Fabrication and characterization of gate-last self-aligned AlN/GaN MISHEMTs with in situ SiN_x gate dielectric," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1862–1868, Jun. 2015.

[13] G. Yu *et al.*, "Dynamic characterizations of AlGaN/GaN HEMTs with field plates using a double-gate structure," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 217–219, Feb. 2013.

[14] N. Fasarakis *et al.*, "Compact model of drain current in short-channel triple-gate finFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1891–1898, Jul. 2012.

[15] Y. L. Chiou, C. S. Lee, and C. T. Lee, "AlGaN/GaN metal-oxide-semiconductor high-electron mobility transistors with ZnO gate layer and $(NH_4)_2S_x$ surface treatment," *Appl. Phys. Lett.*, vol. 97, no. 3, pp. 1–3, Jul. 2010.

[16] C.-T. Lee *et al.*, "Performance improvement mechanisms of i-ZnO/$(NH_4)_2S_x$-treated AlGaN MOS diodes," *Appl. Surface Sci.*, vol. 258, no. 22, pp. 8590–8594, Sep. 2012.

[17] L.-H. Huang and C.-T. Lee, "Investigation and analysis of AlGaN MOS devices with an oxidized layer grown using the photoelectrochemical oxidation method," *J. Electrochem. Soc.*, vol. 154, no. 10, pp. H862–H866, Aug. 2007.

[18] S. Russo and A. Di Carlo, "Influence of the source–gate distance on the AlGaN/GaN HEMT performance," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 1071–1075, May 2007.

[19] W. Long, H. Ou, J.-M. Kuo, and K. K. Chin, "Dual-material gate (DMG) field effect transistor," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 865–870, May 1999.

[20] C.-T. Lee, H.-Y. Lee, H.-L. Huang, and C.-Y. Tseng, "High-performance depletion-mode multiple-strip ZnO-based fin field-effect transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 446–451, Jan. 2016.

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