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Hysteresis Reduction in Negative Capacitance Ge PFETs Enabled by Modulating Ferroelectric Properties in $HfZrO_x$

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ABSTRACT We experimentally demonstrate that hysteresis of negative capacitance (NC) Ge pFETs is reduced through modulating the ferroelectric properties in $HfZrO_x$ (HZO) by changing the post annealing temperature. As annealing temperature varies from 350 °C to 450 °C, HZO exhibits a significant increasing in the ratio of remnant polarization P_r to coercive field E_c, which results in the improvement of the magnitude of ferroelectric NC C_{FE}, therefore contributing to the reduction of hysteresis of the ferroelectric NC Ge transistors. It is also reported that the NC Ge transistor annealed at 450 °C has a small hysteresis of 0.10 V, and achieves the improved SS and I_{DS} compared to control device without HZO.

INDEX TERMS Negative capacitance, ferroelectrics, hysteresis, subthreshold swing, MOSFET.

I. INTRODUCTION

The ferroelectric negative capacitance (NC) field-effect transistor (FET) has been considered as a promising device candidate to overcome the fundamental limitation in subthreshold swing (SS) for the conventional metal-oxide semiconductor FET since it employs the NC action of a ferroelectric film inserted into gate stack [1]. Steep SS below 60 mV/decade has been demonstrated in a number of NC FETs integrated with various ferroelectrics, but the devices are still facing the challenge to achieve the hysteresis-free characteristics [2]–[5]. The theoretical study suggested that the hysteresis characteristics can be modulated by varying the ferroelectric material properties, including the thickness, remnant polarization P_r, and coercive field E_c of the ferroelectric film [6].

Recently, we reported the ferroelectric $HfZrO_x$ (HZO) NC Ge and GeSn pFETs, and the devices exhibited the sub-60 mV/decade SS and hysteresis in $I_{DS} - V_{GS}$ curves induced by the NC effect [7], [8]. It was found that the post annealing temperature had a great impact on the hysteresis performance in the NC FETs. Experiments revealed that, as ratio of P_r/E_c of HZO increased, the hysteresis could be suppressed. However, there is still a lack of the comprehensive study of the effects of variation of ferroelectric properties on the NC transistor performance.

In this paper, the electrical performance of NC Ge pFETs with the post annealing temperature ranging from 350 to 450 °C are characterized. Based on the statistical measurement of ferroelectric properties of HZO annealed at various temperatures, it is proved that hysteresis of NC transistors is significantly reduced with the increasing of the magnitude of ferroelectric negative capacitance C_{FE} realized by modulating the P_r and E_c properties of HZO. The impacts of posting annealing temperature on SS and gate capacitance C_G characteristics of the NC devices are also discussed.

II. FERROELECTRIC PROPERTIES OF HZO

To confirm the crystallization in the HZO film after the post annealing, X-ray diffraction (XRD) measurement was performed on the TaN/HZO/TaN samples. The thickness

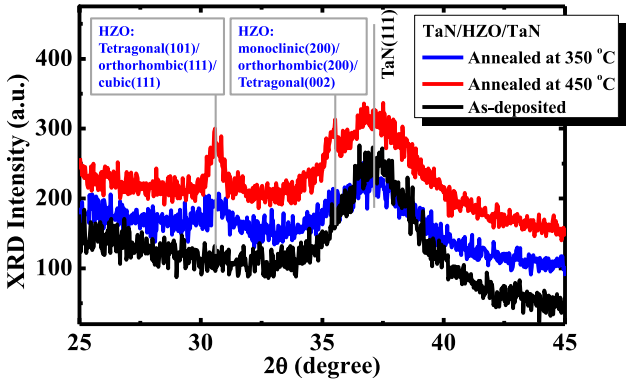

FIGURE 1. **Measured XRD curves of the TaN/HZO/TaN samples indicating the formation of the mixing of tetragonal, orthorhombic, and cubic phases after the post annealing at 350 and 450 °C.**

of HZO is about 6.6 nm. HZO with a Hf:Zr ratio of 0.5:0.5 was deposited by atomic layer deposition (ALD), and TaN was deposited by reactive sputtering. According to the reference patterns for HZO in [9] and [10], XRD curves in Fig. 1 demonstrate that the mixing of tetragonal, orthorhombic, and cubic phases was formed in HZO after the post annealing, which was similar to [9] and [11]. It was reported that the orthorhombic phase contributes to the ferroelectricity of the film [10], [12]–[14].

The ferroelectric characteristics of the HZO film are investigated by the polarization P versus electric field E hysteresis loops measurement. P-E loops were recorded on the pristine devices. Fig. 2(a) shows the curves of P as a function of E for the TaN/HZO/TaN samples with and without the post annealing. A linear polarization indicating the paraelectric dielectric film is observed for the as-deposited TaN/HZO/TaN. After the post annealing at 350, 400 and 450 °C, the ferroelectric phase transition is confirmed by the P-E hysteresis loops. The measured capacitance versus voltage curves of the TaN/HZO/TaN sample are illustrated in Fig. 2(b), demonstrating the ferroelectric properties of HZO [10], [15]. From the statistical plots of P_r and E_c for TaN/HZO/TaN samples in Fig. 2(c), it is clearly seen that the ratio of P_r to E_c of HZO can be effectively modulated by varying the post annealing temperature and the sweeping range of applied voltage. With the post annealing temperature increasing from 350 °C to 450 °C, the P_r of the devices is enhanced, which should be owing to the increasing of quantity of ferroelectric domains [11], [16]. It was also reported that this might be the typical transition from a sub-loop behavior to a well saturated ferroelectric hysteresis, [17]. The impact of the post annealing temperature on the E_c is much weaker compared to the P_r , which is consistent with the results in [18].

Based on the P_r and E_c values in Fig. 2(c), the magnitude of C_{FE} induced by HZO can be calculated by $C_{FE} = (2/3\sqrt{3}) \cdot (P_r/E_c \cdot t_{HZO})$ [6], where t_{HZO} is the thickness of HZO film. From Fig. 3, we can observe that $|C_{FE}|$ is obviously improved by increasing the post annealing temperature and the sweeping range of applied voltage.

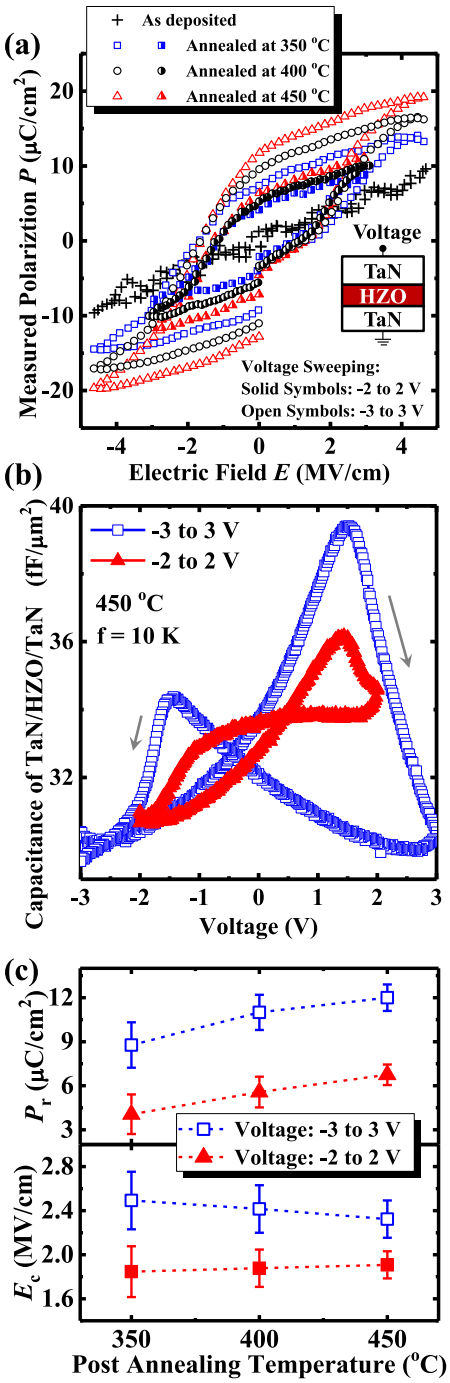

FIGURE 2. **(a) *P-E* hysteresis loops for TaN/HZO/TaN samples with and without the post annealing. The ferroelectric properties of the HZO are directly related to the sweeping range of applied voltage and the post annealing temperature. (b) Measured capacitance versus voltage curves for TaN/HZO/TaN sample annealed at 450 °C. (c) Statistical plots showing that the P_r and E_c can be effectively modulated by varying the post annealing temperature and the sweeping range of applied voltage.**

III. DEVICE FABRICATION

Fig. 4(a) shows the key process steps for the fabrication of NC Ge pFETs integrated with HZO film on n-Ge(001). After the wafer cleaning, Ge substrate was loaded into an ultrahigh

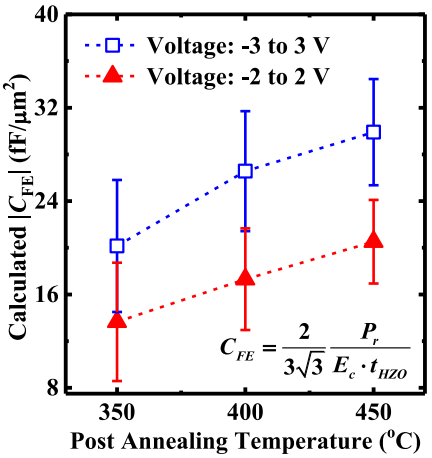

FIGURE 3. Calculated $|C_{FE}|$ of HZO indicating that $|C_{FE}|$ is improved by increasing the post annealing temperature and the sweeping range of applied voltage.

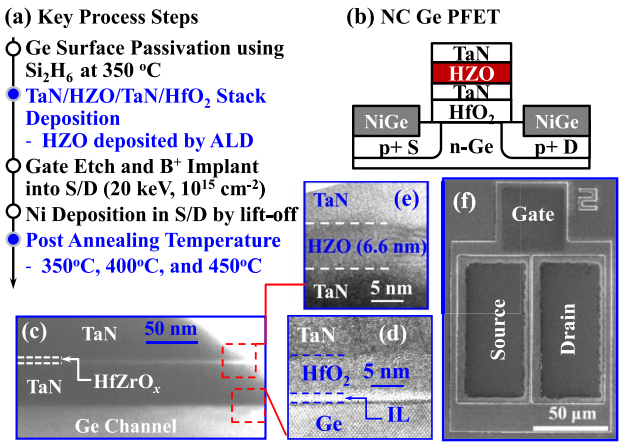

FIGURE 4. (a) Key process steps for the fabrication of ferroelectric NC Ge pFETs. Post annealing was carried out on the devices at different temperatures. (b) Schematic of the fabricated NC transistor. (c) TEM image showing the gate stack of NC device. High resolution TEM (d) featuring TaN/HfO_2 stack on Ge with SiO_2/Si IL, and (e) illustrating the 6.6 nm HZO layer. (f) Top view SEM image of the NC device.

vacuum chamber for annealing at 620 °C for 20 minutes to remove the native oxide. Si_2H_6 passivation at ~350 °C was then carried out to form a Si passivation layer. This was followed by the formation of TaN/HZO/TaN/HfO_2 stack. After gate etching, boron ions (B^+) were implanted into source/drain (S/D) at an energy of 20 keV and a dose of 1 $\times 10^{15}$ cm^{-2}. Non-self-aligned S/D metals were formed by lift off process. Finally, post annealing was carried out at various temperatures for dopant activation, S/D metallization, and crystallization of HZO film. Ge control pMOSFETs with the same TaN/HfO_2 stack but without HZO were also fabricated.

Fig. 4(b) shows the schematic of the fabricated ferroelectric NC Ge pFET. Transmission electron microscope (TEM) image in Fig. 4(c) depicts the TaN/HZO/TaN/HfO_2 stack on Ge channel. High resolution TEM (HRTEM) image in

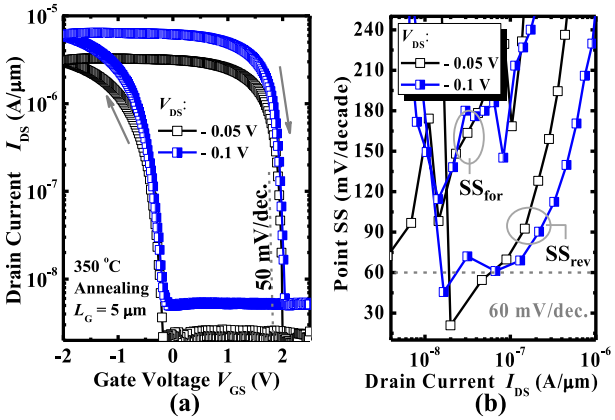

FIGURE 5. (a) Measured $I_{DS} - V_{GS}$ curves of a ferroelectric NC Ge pMOSFET with a post annealing at 350 °C. (b) Point SS versus I_{DS} for the device showing the sub-60 mV/decade steep point SS_{rev}.

Fig. 4(d) shows the uniform SiO_2/Si interfacial layer (IL) on Ge channel. HRTEM image in Fig. 4(e) indicates the poly crystallization of 6.6 nm HZO after the post annealing. Fig. 4(f) shows the top view scanning electron microscope image (SEM) of the NC device. It should be noted that the "wake up effect" of the HZO ferroelectric film will have the impact on the reliability and lifetime of the NC transistors [19]–[21], which needs to be investigated in the future work.

IV. RESULTS AND DISCUSSION

The electrical performance, including the source/drain current I_{DS}, gate leakage current I_G, and capacitance characteristics of NC Ge pFETs annealed at different temperatures were investigated. For all the measurements, the sweeping range of gate voltage V_{GS} was from 2.5 to −2.0 V, and the reverse sweeping was carried out after the forward one. It should be noted that the sweeping range of V_{GS} has influence on the hysteresis of the device, while its impact on SS of the device can be negligible. Fig. 5(a) shows the measured transfer characteristics of a ferroelectric NC Ge pFET underwent a post annealing at 350 °C at V_{DS} of −0.05 and −0.1 V. Gate length L_G of the device is 5 μm. As V_{GS} sweeps reversely, the steep average SS of 50 mV/decade is demonstrated in the NC transistor over two orders of magnitude (i.e., 20 nA/μm ~ 2 μA/μm) of I_{DS}, which is attributed to the NC effect induced by the HZO film. Fig. 5(b) illustrates the point SS versus I_{DS} characteristics of the NC device, demonstrating that sub-60 mV/decade forward and reverse SS, denoted by SS_{for} and SS_{rev}, respectively, are obtained. The device exhibits a larger hysteresis of 2.30 V, which is resulted from the characteristic feature of the ferroelectric control of the charge. In this work, hysteresis is defined as the difference between the V_{GS} at a I_{DS} of 10^{-7} A/μm for the forward and reverse V_{GS} sweeping. No degradation in SS or change in hysteresis is observed when double sweeping of $I_{DS} - V_{GS}$ loops at different V_{DS}. It should be noted that the charge trapping effect also leads to the hysteresis, but

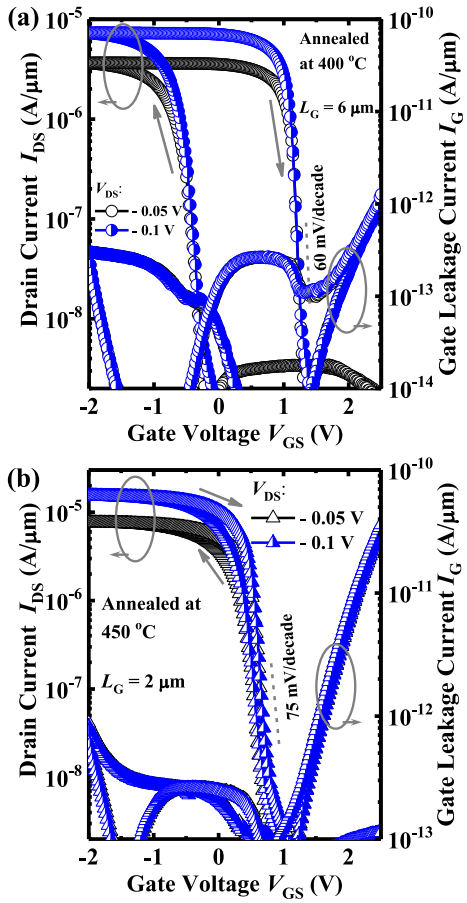

FIGURE 6. Measured $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of the typical ferroelectric NC Ge pFETs with the post annealing at (a) 400 °C and (b) 450 °C.

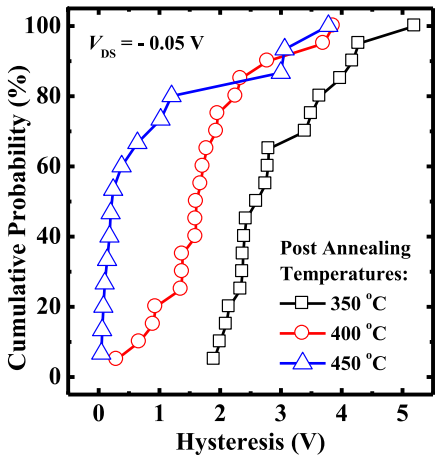

FIGURE 7. Cumulative distribution of hysteresis of the ferroelectric NC Ge pFETs with the post annealing at various temperatures. Some NC transistors annealed at 450 °C have the reduced hysteresis below 0.2 V.

that produces the counterclockwise $I_{DS} - V_{GS}$ loop, opposite to the results induced by ferroelectric switching [22].

The post annealing temperature has a great impact on the hysteresis of the ferroelectric NC Ge transistors. Fig. 6(a) presents the $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of a typical ferroelectric NC Ge pFET with the post annealing at 400 °C at V_{DS} of −0.05 and −0.1 V, and the device exhibits a hysteresis of 1.67 V. As the annealing temperature increases to 450 °C, the hysteresis of the ferroelectric NC transistor can be reduced to be about 0.1 V, as shown in Fig. 6(b). I_G of the NC devices is orders of magnitude lower than the I_{DS}. Comparing Fig. 5(a) and Fig. 6, it is seen that, although, the hysteresis of NC Ge pFETs can be reduced by increasing the annealing temperature, the SS of the devices is degraded. This is consistent with the theoretical study [6], [23]. Later, we will show that the NC transistor with reduced hysteresis still has the improved SS over the control device without HZO.

Fig. 7 illustrates the cumulative distributions of hysteresis of the ferroelectric NC Ge pFETs with the post annealing at different temperatures. The devices have the L_G ranging from 2 to 6 μm. The median values of hysteresis for the NC transistors annealed at 350, 400, and 450 °C are 2.60, 1.61, and 0.22 V, respectively. Some devices with the 450 °C post annealing achieve the hysteresis less than 0.2 V.

The mechanism underlying the effects of variation of the post annealing temperature on the hysteresis of ferroelectric NC Ge pFETs is discussed. It was theoretically predicted the elimination of hysteresis of NC FET could be expected, as $|C_{FE}|$ was larger than the MOSFET gate capacitance C_{MOS} [1], [6], [24]. C_{MOS} is about 20 fF/μm^2, which was extracted from the control device. As shown in Fig. 3, with the applied voltage ranging from - 2 to 2 V, $|C_{FE}|$ of HZO with the post annealing at 350 °C is 14 fF/μm^2. $|C_{FE}|$ of the sample is 21 fF/μm^2 at an annealing temperature of 450 °C, higher than the C_{MOS}, and magnitude of $|C_{FE}|$ is further improved with increasing the post annealing temperature or the sweeping range of applied voltage. In spite of this, the ferroelectric NC Ge pFETs exhibit obvious hysteresis, as top V_{GS} sweeps between 2.5 and -2 V for the I_{DS}-V_{GS} measurement. This is because that the voltage distribution between C_{FE} and C_{MOS} makes the voltage drop at HZO lower than the top V_{GS}, which might make the $|C_{FE}|$ smaller than C_{MOS}. So it is reasonable to observe the hysteresis for the NC Ge transistors. As the post annealing temperature increase from the 350 to 450 °C, the increasing of the ratio of P_rE_c leads to the increasing of $|C_{FE}|$, reducing the hysteresis of the NC devices, which is well consistent with the calculation results in [6].

Fig. 8 shows the measured C_G versus top V_G curves of the NC device annealed at different temperatures and control transistor without HZO. The hysteresis phenomenon is also observed in the C_G-V_G curves of the NC Ge pFETs with the post annealing at 350 °C and 400 °C, which is consistent with the I_{DS}-V_{GS} characteristics. Inset depicts the simple capacitance model of the NC transistor. The TaN/HfO$_2$ stack below HZO in NC transistors is the same as the gate stack of the control device. So C_{MOS} of NC devices can be obtained from the C_G-V_G curve of the control device. Here, the series combination of C_{OX} and C_S is referred to the C_{MOS}. It is

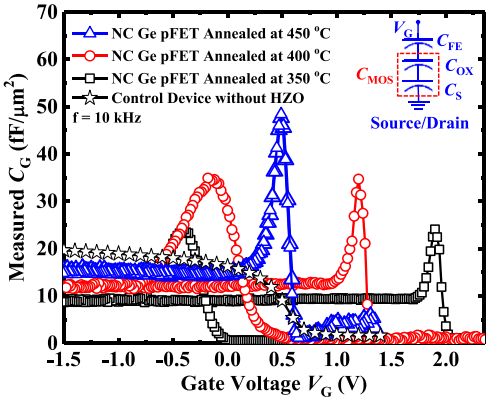

FIGURE 8. Measured C_G versus V_G curves of the NC Ge pFETs annealed at different temperatures and the control device. Inset shows the simple capacitance model of the NC device. The series combination of C_{OX} and C_S is referred to the C_{MOS}. A significantly improved C_G peak is obtained in the NC Ge pFETs compared to the capacitance of the control device, which is due to the NC effect induced by the HZO film.

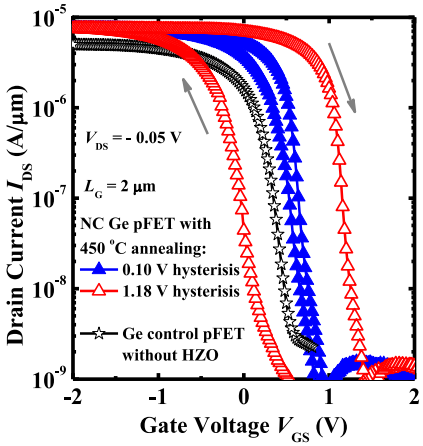

FIGURE 9. I_{DS}-V_{GS} curves of NC Ge pMOSFETs with different values of hysteresis and Ge control device.

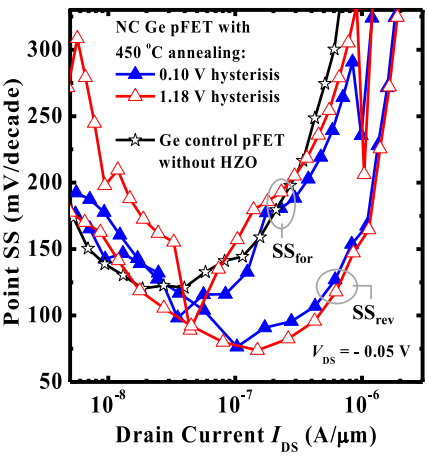

FIGURE 10. Comparison of point SS versus I_{DS} for the NC Ge pFETs and the control device. Both SS_{rev} and SS_{for} of the NC transistor with a hysteresis of 0.10 V are steeper than SS of control device.

noted that, C_G of the NC Ge pFET, which is equivalent to $(C_{FE}{}^{-1}+C_{MOS}{}^{-1})^{-1}$ [24], demonstrates the significantly improved peaks compared to the control device. This proves that the negative C_{FE} is achieved with the sweeping of V_G in the NC devices, in spite of the hysteresis. From the steep SS in I_{DS}-V_{GS} curves, it also can be known that NC effect is achieved in NC transistors annealed at 350 °C and 400 °C. C_{FE} should be close to CMOS for the highest peak of C_G. Nevertheless, if $|C_{FE}|$ reduces to across C_{MOS}, hysteresis will occur [25]. Compared to the 450 °C annealing, the 350 °C and 400 °C produce the smaller magnitude of negative C_{FE}, which lead to the increased hysteresis due to $|C_{FE}| < C_{MOS}$. It is observed that peaks of C_G of the NC transistors are reduced as the post annealing temperature gets decreased. Actually, under $|C_{FE}| < C_{MOS}$ condition, the negative C_G is unstable, and through the voltage allocation, $|C_{FE}|$ is still larger than C_{MOS} at V_{GS} of C_G peaks. Nevertheless, the smaller $|C_{FE}|$ reduces the voltage drop at C_{MOS} as well as the value of C_{MOS}, which results in the decreased C_G peak value. It is clarified that the transient feature of NC effect in devices needs to be characterized at a frequency up to GHz, which was not performed in this work.

Comparable study of SS, transconductance, and output characteristics of the ferroelectric NC Ge pFETs and the control device is carried out. Fig. 9 illustrates the transfer characteristics of a pair of ferroelectric NC Ge pFETs with different values of hysteresis and the control device without HZO. The devices with the L_G of 2 μm underwent the post annealing at 450 °C. The values of hysteresis of the NC transistors are 0.10 and 1.18 V. It can be observed that each NC transistor exhibits the significantly enhanced I_{DS} compared to the Ge control device, whether its hysteresis is larger or small. Point SS as a function of I_{DS} curves in Fig. 10 show that the point SS_{rev} of ferroelectric NC Ge pFETs is much superior to that of control device. It is also noted that the ferroelectric NC Ge pFET with 1.18 V hysteresis obtains a steeper SS_{rev} in comparison with the NC device with hysteresis of 0.10 V in the entire measuring range of I_{DS}. As the V_{GS} sweeps forwardly, the NC Ge transistors achieve the smaller values of minimum SS_{for} over the control device without HZO.

Fig. 11 depicts transconductance G_M of the transistors extracted from the curves in Fig. 9, showing that ferroelectric NC Ge pFETs have the improved G_M over the control device. Ferroelectric NC transistor with 0.10 V hysteresis obtains the 101% and 140% enhancement in the peak G_M in comparison with the control device, as V_{GS} sweeps forwardly and reversely, respectively, at a V_{DS} of −0.05V, which is indicative of the remarkably improved channel conductivity in NC transistor over the control device. Fig. 12 shows the statistical plot of the G_m peak of NC Ge pFETs and the control devices without HZO. All the transistors in this plot have the L_G of 2 μm. NC device have the obvious variation of the performance indicating the non-uniformity of the NC effect. NC devices exhibit 94% and 105% improvement in

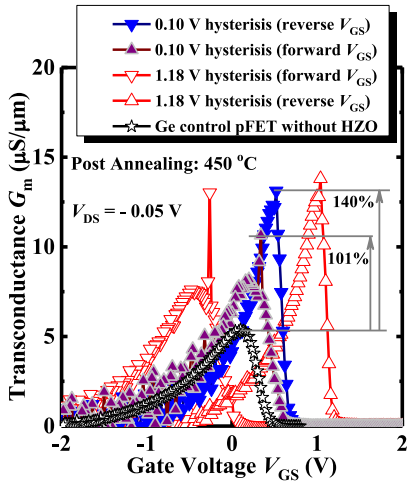

FIGURE 11. Ferroelectric NC Ge pFETs demonstrating the significant improvement in G_M with reverse and forward sweeping of V_{GS} in comparison with Ge control device.

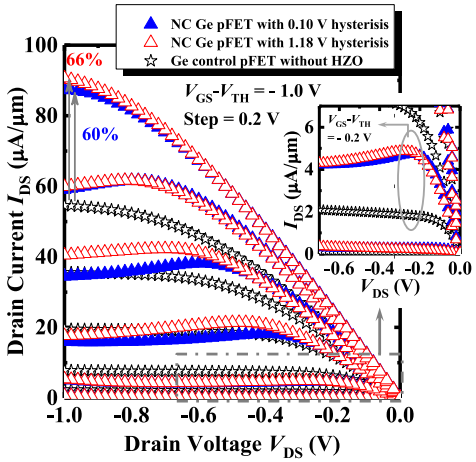

FIGURE 13. I_{DS}-V_{DS} curves of the NC Ge pFETs and the control device without HZO. 60% and 66% I_{DS} improvement are achieved in the NC transistors with 0.10 and 1.18 V hysteresis, respectively, compared to the control device at a supply voltage of −1.0 V. The NC devices exhibit the obvious NDR effect.

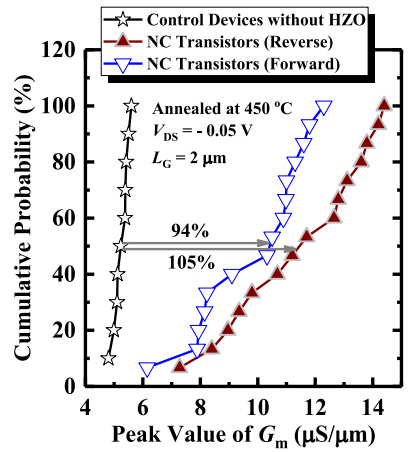

FIGURE 12. Statistical plot of G_m peak for NC Ge pFETs and control devices at V_{DS} of −0.05 V. Peak values of G_m in NC Ge transistors are significantly improved compared to the control devices without HZO.

median G_m peak with forward and reverse sweeping of V_{GS}, respectively, as compared to the control MOSFETs.

Output characteristics of the ferroelectric NC Ge pFETs and the control device in Fig. 13 show that 60% and 66% I_{DS} enhancement are achieved in the NC transistors with 0.10 and 1.18 V hysteresis, respectively, compared to the control device at a supply voltage of −1.0 V. Here, V_{TH} is defined as the V_{GS} at I_{DS} of 10^{-7} A/μm for the forward sweeping of V_{GS} in the I_{DS}-V_{GS} curves in Fig. 9. From Fig. 13 and the inset, it is observed that the negative differential resistance (NDR) is demonstrated in the I_{DS}-V_{DS} curves of the ferroelectric NC devices, which has been theoretically predicted in [26] and [27]. The NDR phenomenon is attributed to the fact that, although V_{GS} is held a constant, the effective voltage at the internal gate is affected by the V_{DS}. At a fixed V_{GS}, where the NC device operates in the NC region, with V_{DS} increasing from zero, the internal gate charge decreases due to drain-to-channel coupling, improving the voltage drop at HZO, which further reduces the internal gate voltage. This positive feedback leads to the suppression of inversion charge density in channel induced by V_{DS}. Initially, in the linear region with small V_{DS}, the increased horizontal electric field by V_{DS} dominates the I_{DS}. While, at a higher V_{DS}, the decreased inversion charge density with V_{DS} due to ferroelectric HZO starts to produce a reduced I_{DS}, causing the NDR effect [26]. Devices shown in Fig. 13 have the similar NDR, except for the curves at the $|V_{GS}\text{-}V_{TH}|$ of 0.6 V. At $V_{GS}\text{-}V_{TH} = -0.6$ V, NC Ge pFET with 1.18 V hysteresis has the reduced NDR phenomenon compared to the device with the hysteresis of 0.10 V, which might be due to the unstable NC effect.

V. CONCLUSION

The effects of variation in P_r and E_c of HZO on the hysteresis of ferroelectric NC Ge pFETs are experimentally studied. The hysteresis of NC transistors is effectively reduced by increasing the magnitude of C_{FE} by modulating P_r and E_c of HZO. It is also demonstrated that the ferroelectric NC Ge pFETs obtain the improved I_{DS} and SS over the control device without HZO. After the post annealing at 450 °C, the ferroelectric NC Ge transistor has a small hysteresis of 0.10 V and demonstrates a 60% I_{DS} enhancement compared to control device at a supply voltage of 1.0 V.

REFERENCES

[1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008.

[2] K.-S. Li *et al.*, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in *IEDM Tech. Dig.*, Washington, DC, USA, 2015, pp. 620–623.

[3] M. H. Lee *et al.*, "Prospects for ferroelectric $HfZrO_x$ FETs with experimentally CET=0.98nm, SS_{for}=42mV/dec, SS_{rev}=28mV/dec, switch-OFF <0.2V, and hysteresis-free strategies," in *IEDM Tech. Dig.*, Washington, DC, USA, 2015, pp. 616–619.
[4] A. I. Khan *et al.*, "Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 111–114, Jan. 2016.
[5] A. Rusu, G. A. Salvatore, D. Jiménez, and A. M. Ionescu, "Metal-ferroelectric-metal-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2010, pp. 395–398.
[6] C.-I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, "Effects of the variation of ferroelectric properties on negative capacitance FET characteristics," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2197–2199, May 2016.
[7] J. Zhou *et al.*, "Ferroelectric negative capacitance GeSn PFETs with Sub-20 mV/decade subthreshold swing," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1157–1160, Aug. 2017.
[8] J. Zhou *et al.*, "Ferroelectric $HfZrO_x$ Ge and GeSn pMOSFETs with sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved I_{DS}," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2016, pp. 310–313.
[9] M.-H. Lee *et al.*, "Ferroelectricity of $HfZrO_2$ in energy landscape with surface potential gain for low-power steep-slope transistors," *IEEE J. Electron Devices Soc.*, vol. 3, no. 4, pp. 377–381, Jul. 2015.
[10] J. Müller *et al.*, "Ferroelectricity in simple binary ZrO_2 and HfO_2," *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, Aug. 2012.
[11] X. Zhang *et al.*, "Inductive crystallization effect of atomic-layer-deposited $Hf_{0.5}Zr_{0.5}O_2$ films for ferroelectric application," *Nanoscale Res. Lett.*, vol. 10, p. 25, Jan. 2015.
[12] J. Müller *et al.*, "Ferroelectricity in yttrium-doped hafnium oxide," *J. Appl. Phys.*, vol. 110, no. 11, pp. 1–5, Dec. 2011.
[13] S. Mueller *et al.*, "Incipient ferroelectricity in Al-doped HfO_2 thin films," *Adv. Funct. Mater.*, vol. 22, no. 11, pp. 2412–2417, Jun. 2012.
[14] M. H. Park *et al.*, "Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature," *Appl. Phys. Lett.*, vol. 102, no. 24, pp. 1–5, Jun. 2013.
[15] J. Müller *et al.*, "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 99, no. 11, Sep. 2011, Art. no. 112901.
[16] J. Wang and T.-Y. Zhang, "Size effects in epitaxial ferroelectric islands and thin films," *Phys. Rev. B, Condens. Matter*, vol. 73, no. 14, pp. 1–11, Apr. 2006.
[17] J. Müller *et al.*, "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 99, no. 11, Sep. 2011, Art. no. 112901.
[18] M. H. Park *et al.*, "Effect of forming gas annealing on the ferroelectric properties of $Hf_{0.5}Zr_{0.5}O_2$ thin films with and without Pt electrodes," *Appl. Phys. Lett.*, vol. 102, no. 11, Mar. 2013, Art. no. 112914.
[19] T. Schenk *et al.*, "Electric field cycling behavior of ferroelectric hafnium oxide," *ACS Appl. Mater. Interfaces*, vol. 6, no. 22, pp. 19744–19751, Nov. 2014.
[20] M. H. Park *et al.*, "Effect of Zr content on the wake-up effect in Hf1-xZrxO2 films," *ACS Appl. Mater. Interfaces*, vol. 8, no. 24, pp. 15466–15475, Jun. 2016.
[21] D. Zhou *et al.*, "Wake-up effects in Si-doped hafnium oxide ferroelectric thin films," *Appl. Phys. Lett.*, vol. 103, no. 19, Nov. 2013, Art. no. 192904.
[22] E. Yurchuk *et al.*, "Charge-trapping phenomena in HfO_2-based FeFET-type nonvolatile memories," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016.
[23] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Compact model for ferroelectric negative capacitance transistor with MFIS structure," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1366–1374, Mar. 2017.
[24] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," in *IEDM Tech. Dig.*, Washington, DC, USA, 2011, pp. 255–258.
[25] C. Hu, S. Salahuddin, C.-I. Lin, and A. I. Khan, "0.2V adiabatic NC-FinFET with 0.6mA/μm I_{ON} and 0.1nA/μm I_{OFF}," in *Proc. IEEE Device Res. Conf.*, Columbus, OH, USA, 2015, pp. 39–40.
[26] G. Pahwa *et al.*, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance—Part II: Model validation," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4986–4992, Dec. 2016.
[27] H. Ota *et al.*, "Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2016, pp. 318–321.

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