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UHD AMOLED Driving Scheme of Compensation Pixel and Gate Driver Circuits Achieving High-Speed Operation

CHIH-LUNG LIN [1,2] (Member, IEEE), PO-SYUN CHEN [1], MING-YANG DENG [1], CHIA-EN WU [1], WEN-CHING CHIU [1], AND YU-SHENG LIN [1]

1 Department of Electrical Engineering, National Cheng Kung University, Tainan 701-01, Taiwan
2 Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan 701-01, Taiwan

CORRESPONDING AUTHOR: C.-L. LIN (e-mail: cllin@mail.ncku.edu.tw)

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ABSTRACT This paper presents a new driving scheme for active-matrix organic light-emitting diode displays. A pixel circuit based on this driving scheme was developed to compensate for the threshold voltage and mobility variations of low-temperature polycrystalline-silicon thin-film transistors (TFTs), eliminate image flickering and current-resistance voltage drops, and suit ultrahigh-definition (UHD) resolution applications. A new gate driver with a concise 6T1C structure is also proposed to realize the driving scheme in practice. Fabricated TFTs and OLEDs were measured to establish models. Simulations using these models demonstrate that the proposed pixel circuit achieves uniform OLED current regardless of undesirable influences at UHD resolution.

INDEX TERMS Active-matrix organic light-emitting diode (AMOLED), low-temperature polycrystalline-silicon thin-film transistors (LTPS TFTs).

I. INTRODUCTION

Achieving an ultra-high-definition (UHD) resolution (3840×2160) for active-matrix organic light-emitting diode (AMOLED) displays is a mainstream goal of the display industry in the near future [1]-[3]. To develop such high-resolution AMOLED displays, high-speed operation of pixel circuits is becoming the major requirement [4]. Low-temperature polycrystalline-silicon thin-film transistors (LTPS TFTs) are recommended for pixel circuits because of their high mobility and excellent current-driving capability to support high-speed operation of display panels [5], [6]. Nevertheless, the non-uniform electrical characteristics of LTPS TFTs among pixels, including threshold voltage (V_{TH}) and mobility variations, induce OLED current fluctuations, resulting in serious image mura [7]. To date, various pixel circuits compensating for V_{TH} variations have been developed [8]–[10], but few of these can be applied in UHD displays because they require a long programming time to detect the threshold voltage of TFTs. In 2007, Chaji and Nathan [11] proposed the parallel addressing scheme to increase the scanning speed of a panel without limiting the programming time. By dividing the compensation operation from data input operation, the pixel circuits in adjacent rows can execute the V_{TH} compensation in parallel without signals from the data line. As a result, the distributing time of pixels in a row line for scanning, called one scan time, is only the "data input period" rather than the whole programming time, which benefits high-resolution displays requiring a short scan time. However, the driving scheme accompanies complicated circuit operations and complicated control signals in the V_{SS} line, which causes circuit instability. Furthermore, having the OLED turned-on during the programming period in [11] would cause image flickering and deteriorate the contrast ratio of the displays. For high-end AMOLED displays, the mobility variations of TFTs and the power line IR drop must be solved to realize high image quality. However, for pixel circuits using internal compensation methods, it is challenging to simultaneously support V_{TH} compensation, mobility compensation, power line IR drop compensation, and parallel addressing scheme. Therefore,

TABLE 1. Comparison between prior methods and proposed scheme.

Method	Characteristics
6T1C [8]	1. Compensation of V_{TH} shift 2. Flicker free 3. Incapability of high-speed operation
4T2C [11]	1. Compensation of V_{TH} shift 2. Parallel addressing in SVGA resolution 3. Complicated signal design in V_{SS}
4T2C [3]	1. Compensation of V_{TH} shift and luminance drop 2. Parallel addressing in FHD resolution 3. Low contrast ratio induced by flicker
This work	1. Compensation of TFT V_{TH} and μ shift 2. Flicker free and no power line I-R drop 3. New high-speed scheme in UHD resolution

external compensation methods have received much attention recently [4], [7], [15]. By designing an external detecting system out of the pixel array, the various variations in pixels can be sensed and compensated for, to produce uniform OLED current. The corresponding pixel structures could, alternately, be made simpler than those adopting internal compensation methods. However, this type of driving scheme is demanding for designers, given the requirement of a heavy algorithm and complicated detecting circuit that must be highly accurate.

This work proposes a new pixel circuit with a novel driving scheme. The proposed driving scheme supports the high-speed operation of pixel circuits and is capable of compensating for the variations in threshold voltage and mobility of TFTs. The flickering phenomenon and the effects of voltage drops in the power lines can also be eliminated. A new gate driver circuit with a simple 6T1C structure was developed to generate the special signal, G[n], of the new driving scheme. For flexibility, the time interval of the two pulses in G[n] can be adjusted to provide adequate compensation time for the proposed pixel circuit. Table 1 depicts a comparison between prior methods and the proposed driving scheme. Among these methods, only the proposed driving scheme carries out high-speed operation with constant V_{DD} and V_{SS}, free from flickering, no requirement of extra reference line, and V_{TH}/ mobility/ V_{DD} compensation.

II. PROPOSED PIXEL CIRCUIT OPERATION

Figs. 1(a) and 1(b) show the proposed pixel circuit and the new driving scheme, respectively. Five p-type LTPS TFTs and two storage capacitors are used, and V_{DD} and V_{SS} are the constant power supply and constant common electrode, which enhance circuit operation stability. The stages of the proposed driving scheme are initialization, V_{TH} compensation, data input, and emission. For V_{DATA} shown in Fig. 1(b), one set of V_{DATA} signals is composed of two voltage levels: $V_{REF}[n+2]$ and $V_{data}[n]$. $V_{REF}[n+2]$ is the reference voltage for pixel circuits in the [n+2]th row, and $V_{data}[n]$ is the data voltage for pixel circuits in the [n]th row. V_{REF} and V_{data} of different rows can be combined (e.g., $V_{REF}[n+3]$ and $V_{data}[n]$, or $V_{REF}[n+4]$ and $V_{data}[n]$) by adjusting the time interval of the two low levels in G[n], namely the

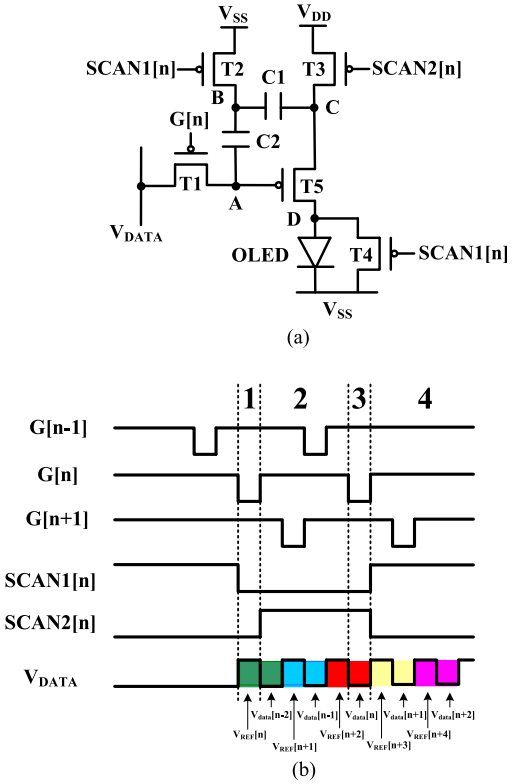

FIGURE 1. (a) Proposed pixel circuit and (b) driving scheme.

duration of V_{TH} compensation. Therefore, the V_{TH} compensation period can be adequately designed according to designer requirement regardless of the display resolution.

The operation of the proposed pixel circuit is described as follows. In the initialization stage, the values of G[n], SCAN1[n], and SCAN2[n] are low to turn on all TFTs. $V_{REF}[n]$ is applied to node A from the V_{DATA} line. Meanwhile, the voltages of node B (V_B), node C (V_C), and node D (V_D) are reset to voltages near V_{SS}, V_{DD}, and V_{SS}, respectively. During the V_{TH} compensation stage, G[n] and SCAN2[n] become high to turn off T1 and T3. Because T2 remains on, to hold V_B at V_{SS}, V_A is maintained at V_{REF} invariably by C2. Subsequently, V_C is discharged through T5 and T4 until T5 is turned off. At the end of this stage, V_C reaches $V_{REF}[n]+|V_{TH\_T5}|$, where V_{TH_T5} is the threshold voltage of T5. In the data input stage, G[n] is low again to turn on T1. $V_{data}[n]$ is input to node A through T1, and T5 is then turned on because the source-gate voltage of T5 (V_{SG_T5}), which is $V_C-V_A = V_{REF}[n]+|V_{TH\_T5}|-V_{data}[n]$, is larger than $|V_{TH\_T5}|$. As a result, node C starts discharging according to the following equation

$$C1 \cdot \frac{dV_{SG\_T5}}{dt} + \frac{k_{T5}}{2}\left(V_{SG\_T5} - |V_{TH\_T5}|\right)^2 = 0 \qquad (1)$$

To obtain V_{SG_T5}, let $V_{SG\_T5} = Z+|V_{TH\_T5}|$, and substitute it into Eq. (1), yielding,

$$V'_{SG\_T5} = \frac{-k_{T5}}{2C1}Z^2 \qquad (2)$$

Let $P = 1/Z \Rightarrow Z' = -Z^2P'$, and substitute it into Eq. (2), yielding,

$$-Z^2P' = \frac{-k_{T5}}{2C1}Z^2 \tag{3}$$

Therefore, P can be expressed as

$$P = \frac{k_{T5}}{2C1}T + A \tag{4}$$

where T is the discharging time and A is a constant. Substituting Eq. (4) into $P = 1/Z$ yields,

$$Z = \frac{1}{\frac{k_{T5}}{2C1}T + A}, \ where\ A = \frac{1}{V_{REF}[n] - V_{data}[n]} \tag{5}$$

Therefore, V_{SG_T5} could be expressed as

$$V_{SG\_T5}(t = T) = \frac{1}{\frac{k_{T5}}{2C1}T + \frac{1}{V_{REF}[n] - V_{data}[n]}} + |V_{TH\_T5}| \tag{6}$$

The varying voltage during the discharging time, ΔV_U, is given by

$$\begin{aligned} \Delta\ V_U &= V_{SG\_T5}(t = T) - V_{SG\_T5}(t = 0) \\ &= V_{REF}[n] - V_{data}[n] - \frac{1}{\frac{k_{T5}}{2C1}T + \frac{1}{V_{REF}[n] - V_{data}[n]}} \end{aligned} \tag{7}$$

where k_{T5} is $\mu \cdot C_{OX} \cdot (W/L)_{T5}$. Therefore, ΔV_U is dependent on k_{T5} involving the mobility of T5 [3]. Notably, T4 is turned on continuously during programming; consequently, the OLED can stay off to enhance the contrast ratio of displays. In the emission stage, G[n] and SCAN1[n] are high to turn off T1, T2, and T4, and SCAN2[n] is low to turn on T3. Because V_{SG_T5} in this stage is identical to that in the data input stage, the OLED current determined by V_{SG_T5} can be expressed as

$$\begin{aligned} I_{OLED} &= \frac{k_{T5}}{2}\left(V_{SG_T5} - \left|V_{TH_T5}\right|\right)^2 \\ &= \frac{k_{T5}}{2}\left[V_{REF}[n] + \left|V_{TH\_T5}\right| - V_{data}[n]\right. \\ &\qquad \left. -\ \Delta V_U - \left|V_{TH\_T5}\right|\right]^2 \\ &= \frac{k_{T5}}{2}\left(V_{REF}[n] - V_{data}[n] - \Delta V_U\right)^2 \end{aligned} \tag{8}$$

According to Eq. (8), the OLED current is independent of the threshold voltage of T5 and the IR voltage drop in the power line. Moreover, as the mobility of T5 increases, k_{T5} and ΔV_U also increase, which suppress the rise of OLED current. As a result, the effect of the mobility variation of the TFT can be ameliorated. Additionally, there is no image flickering during programming by the turned-on T4.

III. PROPOSED GATE DRIVER OPERATION

SCAN1[n] and SCAN2[n] in Fig. 1(b) can be simply generated by common gate drivers with proper timing adjustment of clocks. In contrast, the gate driver to produce the special G[n] signal needs to be newly developed with its timing, as shown in Fig. 2(a) and (b). Fig. 2(c) shows the left side part of dual-side driving configuration for the proposed driving scheme. One row stage is composed of two gate driver circuits, including the proposed 6T1C gate driver

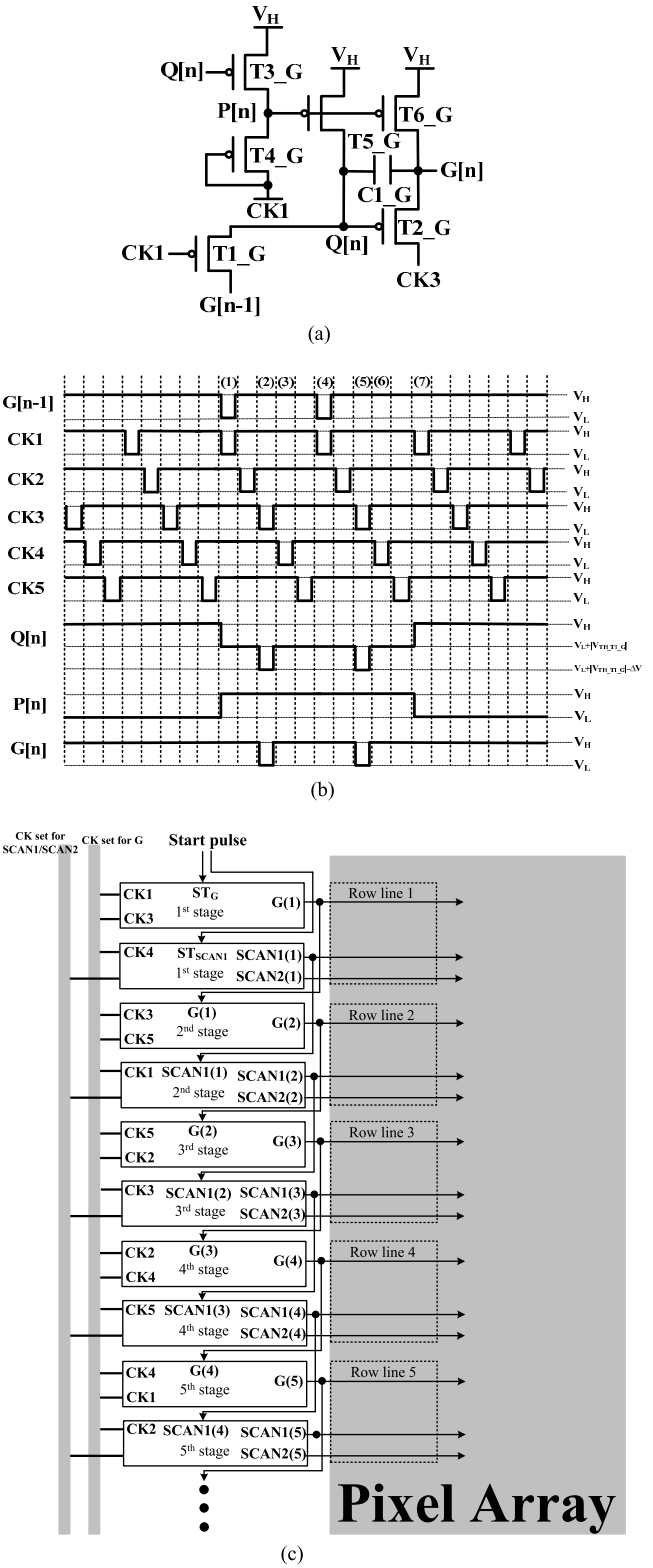

FIGURE 2. (a) Proposed gate driver circuit and (b) its timing diagram. (c) Block diagram of left side in dual-side driving configuration. CK1–CK5 in timing diagram correspond to CK set for G herein.

TABLE 2. Design parameters of proposed pixel circuit.

Parameter	Value	Parameter	Value
SCAN1 (V)	−10 ~ 20	$(W/L)_{T1\text{-}T4}$(μm)	3 / 3
SCAN2 (V)	−10 ~ 20	$(W/L)_{T5}$(μm)	4 / 15
G[n] (V)	−10 ~ 20	$(W/L)_{TOLED}$(μm)	5 / 18
V_{DATA} (V)	−3 ~ 0	C1 (pF)	0.15
V_{REF} (V)	1	C2 (pF)	0.15
V_{DD} / V_{SS} (V)	8 / −3	C_{OLED} (pF)	0.5

for generating G[n], and a general gate driver circuit for generating SCAN1[n] and SCAN2[n]. The time interval between two pulses in G[n] can be adjustable by collocating different driving clocks, For this study, it was set to four times the pulse width, therefore, five clocks CK1∼CK5 were used. T1_G, T2_G, and C1_G compose the pull-down circuit, and T3_G to T6_G compose the pull-up circuit. Because LTPS TFTs have stable electrical characteristics and almost no threshold voltage shift after stress [13], the proposed gate driver suppresses G[n] distortion through the dc stabilization. The main operation can be divided into seven stages which are described as follows. In stage (1), the first pulse of G[n-1] from the previous gate driver is applied to Q[n] through T1_G; therefore, Q[n] is discharged to $V_L + |V_{TH\_T1\_G}|$. Meanwhile, because T3_G is also turned on by Q[n], P[n] is charged to a high voltage near V_H and then turns off T5_G and T6_G. In stage (2), CK3 becomes low to discharge G[n] from V_H. Through C1_G coupling, Q[n] is further decreased to $V_L + |V_{TH\_T1\_G}| - \Delta V$ and enhances the driving capability of T2_G. Thus, G[n] is completely discharged to V_L and transferred to the [n]th row line and the gate driver of the next stage. In stage (3), G[n] and Q[n] are charged back to V_H and $V_L + |V_{TH\_T1\_G}|$ respectively by CK3. In stage (4), the second pulse of G[n-1] from the previous gate driver stabilizes the low level of Q[n], and in stage (5), CK3 becomes low again, to discharge G[n]. Simultaneously, Q[n] couples to $V_L + |V_{TH\_T1\_G}| - \Delta V$ to completely discharge G[n] to V_L. Hence, the second pulse of G[n] is applied to the [n]th row line and gate driver of the next stage. In stage (6), G[n] returns to V_H, and Q[n] is boosted to $V_L + |V_{TH\_T1\_G}|$. In stage (7), CK1 is low, to turn on $T1_G$; consequently, Q[n] is charged to V_H. In addition, P[n] is reduced by CK1 and turns on $T5_G$ and $T6_G$, which are responsible for stabilizing Q[n] and G[n], respectively. After these main operations, Q[n] and G[n] might have fluctuations caused by the clock feedthrough of CK3. To avoid this, P[n] is held at $V_L + |V_{TH\_T4\_G}|$ by CK1 to turn on $T5_G$ and $T6_G$ continuously. The dc stabilization by $T5_G$ and $T6_G$ forces Q[n] and G[n] at V_H robustly to suppress the CK3 feedthrough. Consequently, the proposed gate driver circuit can realize low levels of G[n] twice per frame through the simple 6T1C structure and stabilize G[n] and Q[n] through the dc driving of T5_G and T6_G.

IV. RESULTS AND DISCUSSION

Fig. 3 shows the measured transfer characteristics of the driving TFT, which were fitted to establish TFT models

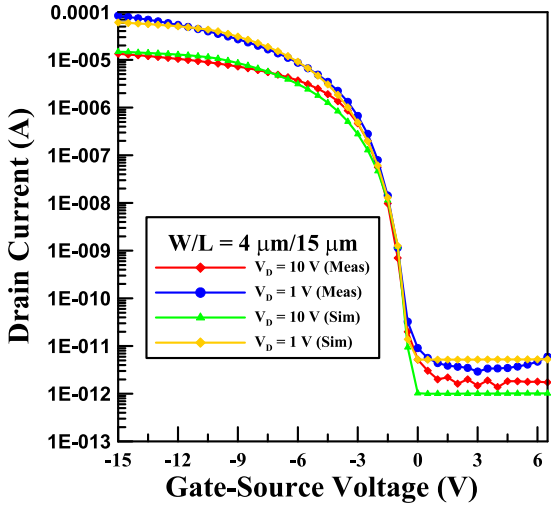

FIGURE 3. Measured I-V characteristics of LTPS TFT with W/L = 4 μm / 15 μm at VDS = 1 V and 10 V.

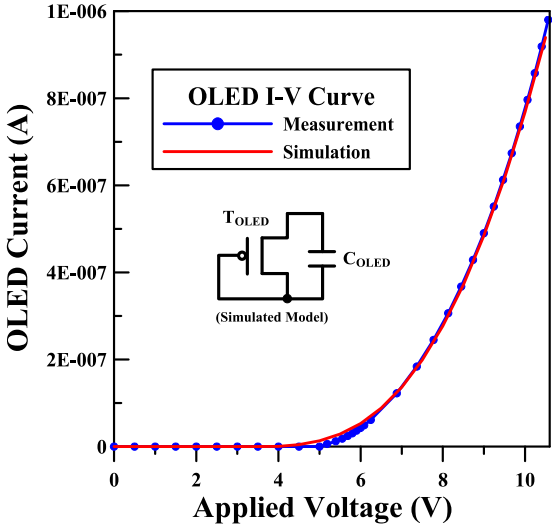

FIGURE 4. Measured I-V characteristics of OLED.

(Rensselaer Polytechnic Institute model, LEVEL = 62) in an HSPICE simulator. The sub-threshold swing, on/off current ratio, threshold voltage, and field-effective mobility are 0.437 V/decade, 9.6×10^6, −1.25 V, and 85 $cm^2/V{\cdot}s$, respectively. The luminance efficiency of standard fabricated OLED device is 33.63 cd/A, and its electrical characteristics are shown in Fig. 4. It was emulated by a diode-contacted TFT of W/L = 5 μm/18 μm and a parallel capacitor of 0.5 pF. All the design parameters are listed in Table 2. In general, the reference voltage for the driving TFT in V_{TH} compensation is applied and held by the data line or extra reference line [10], [13], [14]. However, using reference voltage from data line causes a long scan time for one row, and adding extra reference line reduces the aperture ratio of pixels. In this study, although the reference voltage of the driving TFT in the V_{TH} compensation stage, $V_{REF}[n]$, is provided by the V_{DATA} line, the operation of

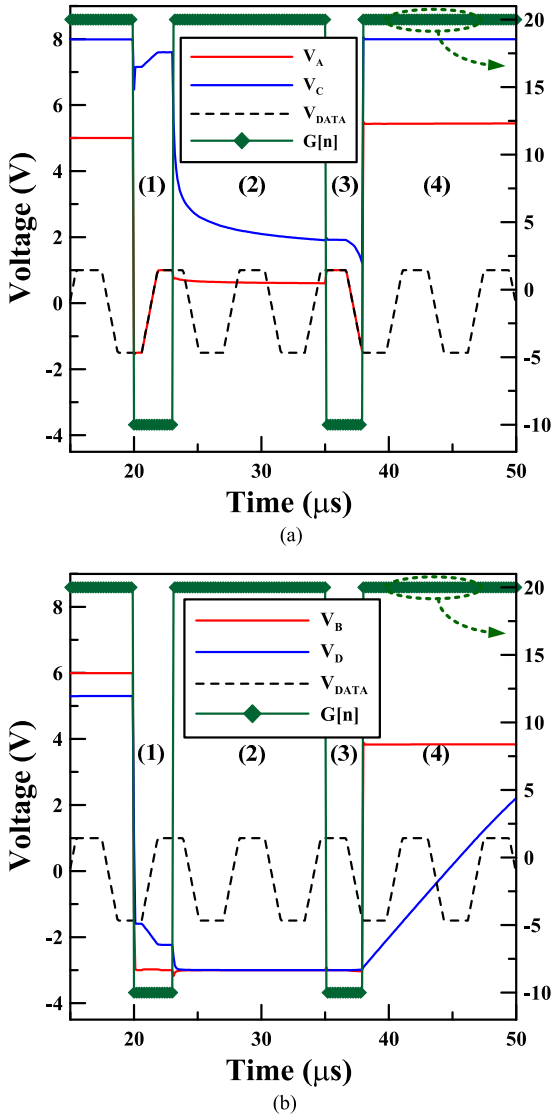

FIGURE 5. Simulated transient waveforms of (a) nodes A, C (b) nodes B, D, data line, and G[n] of proposed pixel circuit.

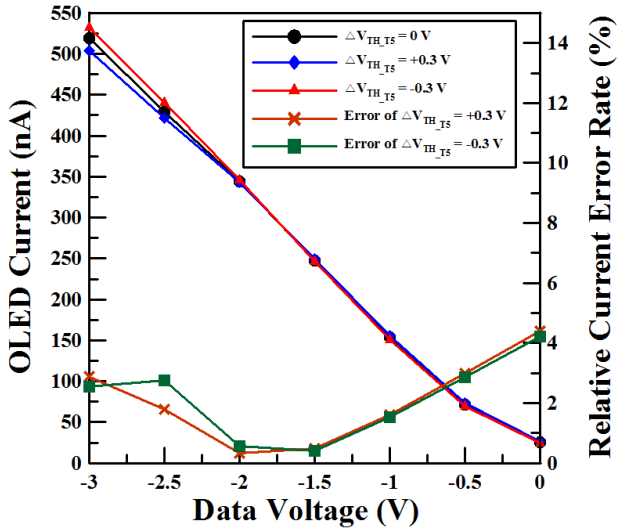

FIGURE 6. Output characteristic and relative current error rates of proposed pixel circuit as ΔVTH_T5 are ±0.3 V.

the V_{DATA} line is not limited by compensation time because $V_{REF}[n]$ can be held in the V_{TH} compensation stage by C2 instead of the V_{DATA} line, or any reference line. As a result, the compensation time of the proposed pixel circuit is independent of display resolution; meanwhile, the aperture ratio is not sacrificed. In real panel fabrication, it is difficult to observe how the proposed pixel circuit compensates for the V_{TH} variations or the mobility variations exactly because the variation contribution from V_{TH} ariations or mobility variations is ambiguous. Thus, HSPICE simulation is executed to investigate the performance of the proposed pixel circuit with these two variations. Fig. 5 presents the simulated waveforms of the proposed pixel circuit. At the end of stage (1), V_C and V_D reach 7.16 V and −1.60 V respectively when V_{DD} and V_{SS} are set to 8 V and −3 V. T5 is in the "on" state during initialization, and remains on throughout stage (2), discharging node C until V_C reaches $V_{REF}[n]+|V_{TH\_T5}|$. In addition, the voltage across OLED is 1.40 V ($V_D - V_{SS}$) in stage (1). This applied voltage reveals the off state of OLED with its turn-on voltage of around 4 V. Although the OLED is off during initialization, a constant current of up to 13.1 μA flows through T4 in stage (1). The power consumption caused by this current is evaluated to 13.1 μA × 11V($V_{DD} - V_{SS}$) × 3(R/G/B) × 3840 (columns) = 1.66 W. Fig. 6 shows the OLED currents of the proposed pixel circuit when threshold voltage variations of T5 (ΔV_{TH_T5}) are ±0.3 V and the mobility is unvaried. The proposed pixel circuit maintains stable current despite ΔV_{TH_T5}, verifying the compensation of the threshold voltage variations. As for mobility variations, the proposed pixel circuit executes mobility compensation through source-gate voltage discharging of T5 (ΔV_U) in the data input period. The mobility variations ($\Delta\mu$) of the driving TFT were modulated from +25% to −25%, and the threshold voltage was unvaried. With constant $V_{REF}[n] = 1$ V and $V_{data} = -1.5$ V, Fig. 7 shows the interdependence between ΔV_U and I_{OLED} when the discharging time is set to 0.3 μs. According to the simulation results, a −25% variation in mobility induces a ΔV_U of 0.2680 V, and a 25% shift in mobility increases it to 0.2723 V. The corresponding I_{OLED} still slightly decreases with TFT mobility owing to the nonlinear relationship between TFT mobility and OLED current. Namely, the proposed driving scheme cannot completely compensate for the mobility variation. In spite of the partial compensation for mobility variations, acceptable error rates of less than 2 % shown in Fig. 8(a) indicate the effective compensation for mobility variations in this work. Next, the V_{DD} of the proposed pixel circuit was changed from 8 V to 7.5 V to imitate the voltage drop in the power line induced by parasitic loads. Fig. 8(b) displays the OLED current versus V_{DD} drop. Different data voltages were applied to investigate the influence of a V_{DD} drop at high, middle, and low gray

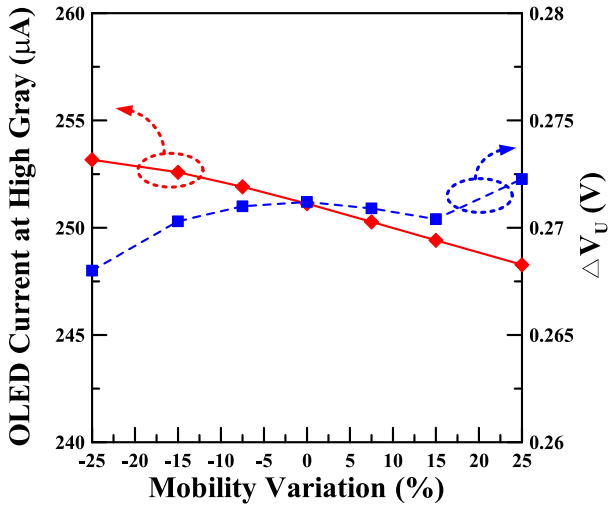

FIGURE 7. ΔV_U and I_{OLED} when mobility of T5 shifts from −25% to + 25%.

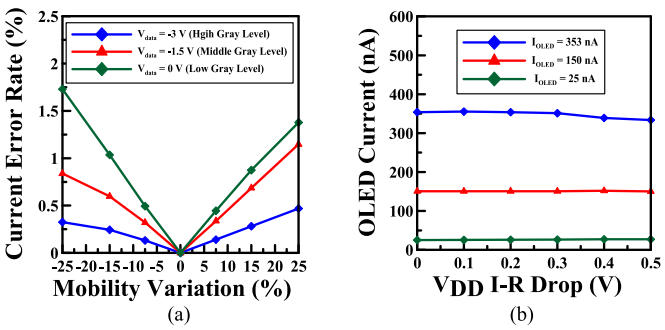

FIGURE 8. (a) Relative current error rates of different V_{data} when mobility of T5 varies ± 25%. (b) OLED currents of different gray levels when V_{DD} drops 0.5 V.

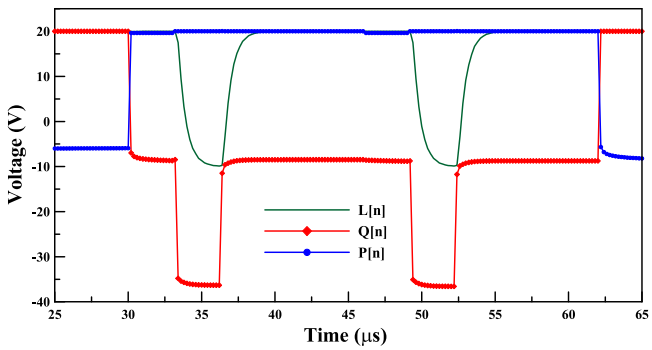

FIGURE 9. Simulated waveforms of Q[n], P[n], and L[n] nodes.

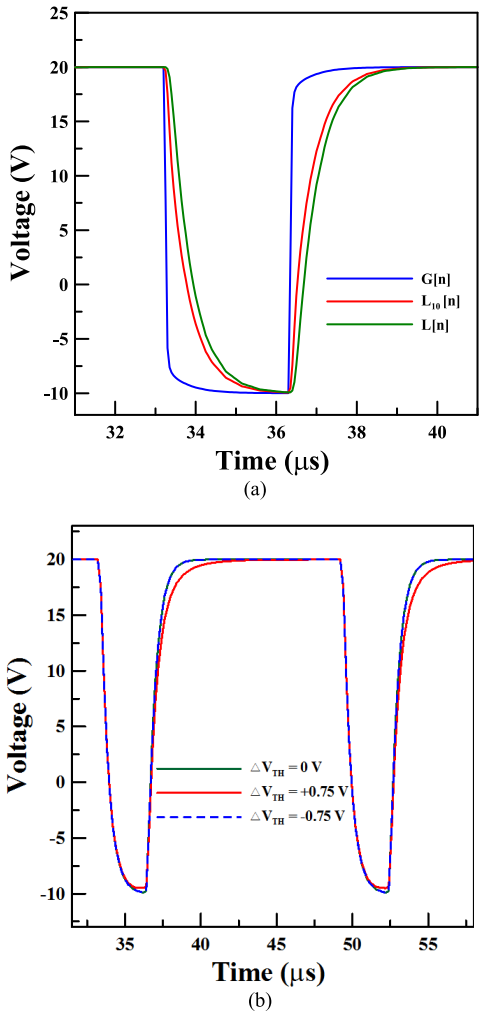

FIGURE 10. (a) Simulated waveforms at G[n], L10[n], and L[n] nodes in RC network. (b) Waveform of L[n] with different VTH variations of TFTs.

TABLE 3. Design parameters of proposed gate driver circuit.

Parameter	Value	Parameter	Value
V_H (V)	20	$(W/L)_{T2}$(μm)	300 / 5.5
CK1-CK5 (V)	−10 ~ 20	$(W/L)_{T3}$(μm)	80 / 5.5
C1_G (pF)	1.5	$(W/L)_{T4}$(μm)	10 / 40
$(W/L)_{T1}$(μm)	50 / 5.5	$(W/L)_{T5/T6}$(μm)	10 / 5.5

levels. Maximum current errors at high and low gray levels are 5.75% and 8.62% respectively, revealing an effective suppression in the current fluctuation. These results verify the compensation capability of the proposed pixel circuit under variations in TFT characteristics and power supply in AMOLED displays.

The proposed gate driver circuit was simulated with the design parameters listed in Table 3. Five-phase nonoverlapping clocks drive the proposed gate driver circuit with a clock frequency of 62.5 kHz. The resistive and capacitive loads of the row lines were set to 27 kΩ and 167 pF to match the specifications of 15-inch LTPS UHD displays. This work adopts the dual-side driving of gate driver for loading reduction, which reduces half resistance and capacitance of a row line, becoming 13.5 kΩ and 83.5 pF. In the simulation, the RC network comprises 20 stages of the RC circuit to emulate the realistic resistive and capacitive line loadings. Fig. 9 shows the simulated waveforms of Q[n], P[n], and the farthest node in the RC network L[n]. The output voltage swing ranges from −10 V to +20 V, and the rising time and falling time are 1.161 μs and 1.164 μs, respectively. According to the simulations, the two pulses of

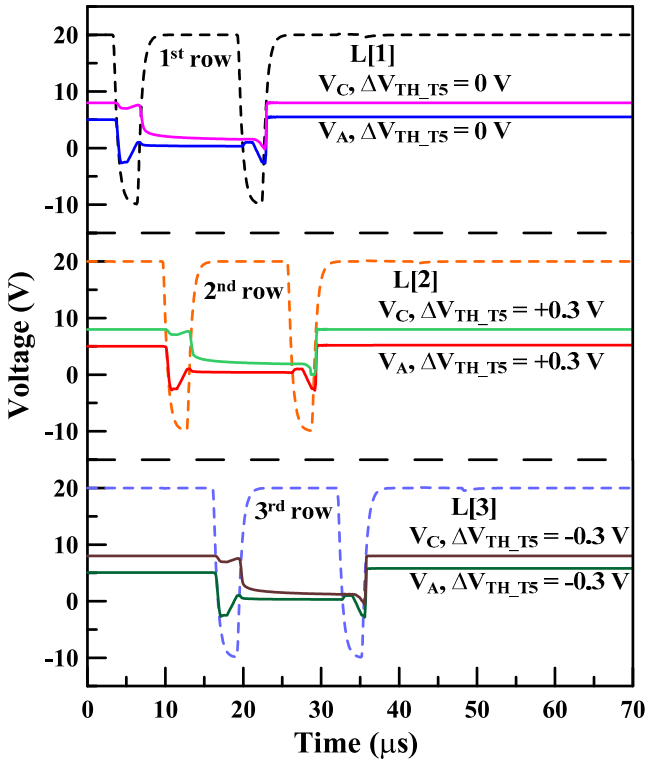

FIGURE 11. Simulated operations of proposed pixel circuit for array mode (one column × three rows) with varying VTH of driving TFT at the same gray level (V_{DATA} = −2.5 V).

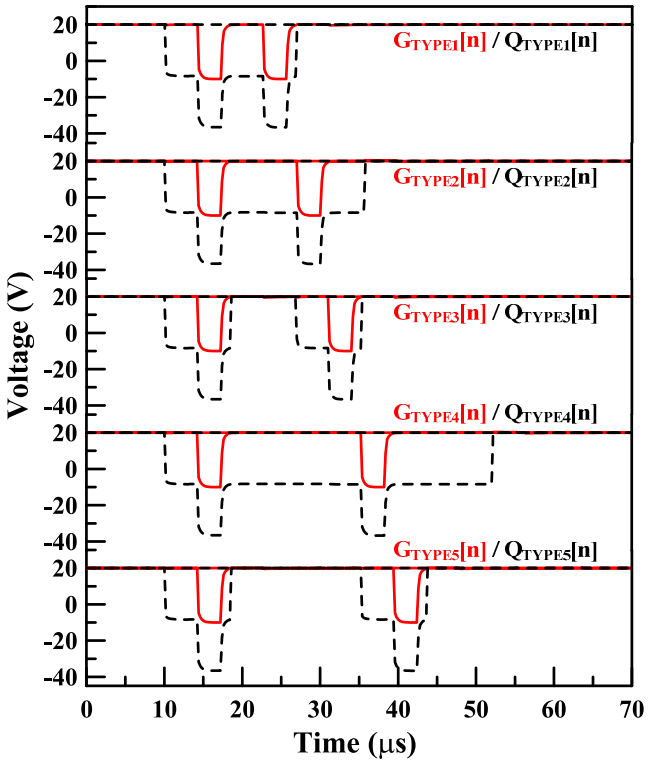

FIGURE 12. Five types of output signal using different driving clocks, which means adjustment of time interval of two output pulses.

G[n] could be successfully produced for use in the proposed driving scheme. Notably, because of the clock feedthrough of CK1, P[n] has a slight drop occurring between the two pulses of L[n]. However, this phenomenon does not affect Q[n] and L[n] because T5_G and T6_G remain turned off in this period. Fig. 10(a) plots the gate pulse in different positions of the RC network to elucidate the loading effect, where L_{10}[n] denotes the tenth node in the 20-stage RC network. In Fig. 10(b), L[n] is presented with more serious V_{TH} variations of ± 0.75 V in each TFT to the distortion. It could be seen that L[n] of +0.75 V V_{TH} variation is more distorted than that of −0.75 V variation because the TFT characteristics are near the depletion mode. Although variations in V_{TH} influence the output signal, the proposed gate driver works normally because the operation of the TFTs in the linear region allows larger variations in characteristics than does the operation of the driving TFT of the pixel circuit in the saturation region. To further investigate the array-mode operation of the proposed driving scheme, an 1×3 matrix with a $\Delta V_{TH_{T5}}$ of ±0.3 V was simulated, as shown in Fig. 11. The 6T1C gate driver circuit was applied to drive the 5T2C pixel circuit, and the results show that the proposed pixel circuits in different rows successfully detect the variations in $V_{TH_{T5}}$ and maintain the corresponding V_A level in the emission step. Fig. 12 demonstrates five types of G[n] and the corresponding Q[n] generated by the proposed gate driver circuit with different driving clocks. The proposed gate driver circuit can generate G_{TYPE1}[n], G_{TYPE3}[n], and G_{TYPE5}[n] through two-phase driving clocks (CK and XCK); G_{TYPE2}[n] is produced by the three-phase driving clocks (CK1, CK2, and CK3). The time interval of the two pulses in G[n] can be adjusted by adopting different driving clocks while the gate driver structure does not need to be modified. The proposed gate driver circuit could be introduced to other driving schemes that require control signals with pulses twice per frame.

V. CONCLUSION

A novel driving scheme including a new 5T2C pixel circuit and a concise 6T1C gate driver circuit is proposed for use in AMOLED displays. With only three control signals, the proposed scheme can support high-speed operation of the panel, compensate for threshold voltage and mobility variations, and eliminate image flickering and V_{DD} I-R drops. In addition, the proposed gate driver circuit produces a special G[n] signal in which the time interval of the two pulses can be adjusted by adopting different driving clocks. The simulated results based on fabricated devices verify the feasibility of the proposed driving scheme.

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CHIH-LUNG LIN (M'07) received the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Taiwan, in 1993 and 1999, respectively. In 1999, he joined AU Optronics, where he researched on driving waveform design and system circuit design of plasma-display panels. In 2001, he began researching integrated circuit design. He joined the faculty of National Cheng Kung University, in 2004, where he is currently a Professor with the Department of Electrical and Engineering. His current research emphases are in the areas of pixel circuit design for AMOLED and BPLCD, gate driver circuit design for AMLCD, and flexible display circuit.

PO-SYUN CHEN received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2011, 2013, and 2017, respectively. His research focuses on the pixel circuit and gate driver circuit for AMOLED, TFT-LCD, BPLCD, and optical pixel sensor circuit.

MING-YANG DENG received the B.S. degree in electronic engineering from the National Chin-Yi University of Technology, Taichung, Taiwan, in 2014, and the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2016, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include the pixel circuit design for AMOLED and BPLCD and the gate driver circuit design for AMLCD.

CHIA-EN WU received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2011, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include optical pixel sensor circuit and gate driver circuit design on glass for AMLCD.

WEN-CHING CHIU received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2011, where he is currently pursuing the Ph.D. degree. His current research interests include software development and hardware design of the integrated system for senior-focused assist, and pixel detection system for AMOLED.

YU-SHENG LIN received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2017, where he is currently pursuing the M.S. degree. His research focuses on the system circuit design for AMOLED and AMLCD displays.