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Electrostatically Doped DSL Schottky Barrier MOSFET on SOI for Low Power Applications

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ABSTRACT In this paper, we propose and simulate a novel Schottky barrier MOSFET (SB-MOSFET) with improved performance in comparison to the conventional SB-MOSFET. The proposed device employs charge plasma/electrostatic doping-based dopant segregation layers (DSLs) by using metal extensions (Hafnium) at the source and drain top and bottom edges. The metal hafnium induces charge plasma and hence realizes DSLs adjacent to source and drain regions. These charge plasma DSLs reduce the tunneling width and hence enhances the performance of the proposed device. The proposed electrostatically doped DSL-based SB-MOSFET has all the advantages of the conventional SB-MOSFET and it outperforms the state of the art doped DSL-based MOSFET. A two-dimensional calibrated simulation study has shown that the ON current (I_{ON}), I_{ON}/I_{OFF} ratio, subthreshold-swing and cutoff frequency (f_T) of the proposed device have been increased by ∼420 times, ∼1000 times, 14.5%, and 290 times in comparison to conventional SB-MOSFET, respectively. The transient analyses have shown that a reduction by 16 times in ON delay and 6 times in OFF delay in the proposed device-based inerter in comparison to the conventional SB-MOSFET-based inverter.

INDEX TERMS Electrostatically doped, charge plasma, source extensions, Schottky barrier, DSL, SOI.

I. INTRODUCTION

Tte aggressive scaling of MOS devices has improved the performance of MOSFET based integrated circuits in terms of speed, packing density, power dissipation, cost etc. However, the continuous scaling of device dimensions in sub-22/18 nm range is extremely difficult due to short channel effects (SCE), leakage current increase, self-heating effects, reliability issues, requirement of abrupt doping profiles and shallow junctions etc. [1]–[5]. In order to address these issues, ultra-thin fully depleted silicon on insulator (SOI) MOSFET, halo-doped fully depleted SOI, ground-plane fully depleted SOI and multiple-gate structures have been developed. Among them ultra-thin fully depleted SOI MOSFET is the most promising because of best SCE suppression capability and planar structure [4]–[6]. However, as the thickness of the silicon film is reduced it significantly increase the source/drain series resistance (R_{SD}), which is being considered as one of the biggest hurdle in realizing highly scaled devices and in keeping Moore's law valid.

The R_{SD} problem can be addressed by increasing the doping of source/drain (S/D) or by increasing the area of source/drain regions, like raised source/drain (R_{SD}). However, both these solutions lead to a fabrication complexity in devices [7]–[10]. A potential way to address the RSD problem is to replace the doped source/drain regions by metals or metal silicide. Metal source/drain devices are planner structure, with reduced series RSD, results in abrupt junctions and can be fabricated at lower temperature [6]–[10]. However, metal source/drain MOS devices show poor ON state performances due to Schottky barrier at the metal semiconductor junction. The requirement of zero Schottky barrier height is an important requirement for having higher ON state performance [20]–[29]. The dopant segregation layer (DSL) has been used in the conventional SB-MOSFET [11]–[15] to reduce the Schottky barrier height and width and has improved the ON current performance significantly. However, realizing a doped DSL is difficult, it increases the fabrication complexity and also increases the thermal budget [14], [15].

In this paper, we propose and simulate a novel structure of SB-MOSFET having DSLs at the source and drain sides of the channel. The DSLs are not doped ones, however, are being realized by using two metal extensions each at the top and bottom of metallic source and drains, which induce n-type charge plasma [16]–[20] adjacent to metallic source and drain regions. The proposed device has been named as electrostatically doped dopant segregation layer Schottky barrier MOSFET (ED-DSL-SB-MOSFET). The proposed ED-DSL-SB-MOSFET is a single gate device, employs metallic source/drain with two extensions and hafnium oxide as gate dielectric. The source and drain regions consists of three parts; main source/drain, source/drain extension1 (Extn1) and source/drain extension2 (Extn2). Erbium silicide is used to realize metallic source and drain regions and hafnium with work function 3.7eV is being used as S/D extensions at the top and bottom. The metallic S/D extensions induce charge plasma and are responsible for the reduction in SB widths which in turn increases the tunneling in the proposed devices.

A calibrated 2D simulation of the proposed ED-DSL-SB-MOSFET has been done and its performance has been compared with conventional SB-MOSFET and the doped DSL-SB-MOSFET [14]. A significant improvement in ON current (I_{ON}), I_{ON}/I_{OFF} and the cutoff frequency (f_T) by 420 times, 100 times and 290 times respectively have been achieved in the proposed device in comparison to the conventional SB-MOSFET. At circuit level two CMOS inverters have been designed using the proposed and the conventional SB-MOSFETs. The transient analysis has been performed using the mixed mode simulation feature of the Atlas simulator. It has been observed that significant reduction in ON and OFF delays are achieved in the proposed device in comparison to the conventional one. An important issue with the proposed device is the fabrication complexity. However, as the fabrication technology is maturing day by day, the proposed device can be fabricated with relative ease. The paper is divided into five sections. Section II discusses various device structures studied in this work. Various results are discussed in Section III. The circuit level implementation of various devices is done in Section IV. The work is calculated in Section V.

II. DEVICE STRUCTURES AND SIMULATION SETUP

Fig. 1 shows the device schematics of the conventional and the proposed devices. Fig. 1(a) is the conventional SB-MOSFET and Fig. 1(b) is the conventional doped DSL based SB-MOSFET by Patil and Qureshi [14]. Fig. 1(c) is the proposed asymmetric ED-DSL-SB-MOSFET where two extensions have been employed at the top and bottom of metal source regions. Fig. 1(d) is the proposed symmetric device ED-DSL-SB-MOSFET where metal extensions have been employed at the top and bottom of metallic source and drain regions. All the device structures have gate length (L_G) of 50nm and the source and drain are made up of Erbium silicide ($ErSi_{1.7}$), with work function of 4.5eV. The other device parameters used include gate oxide thickness

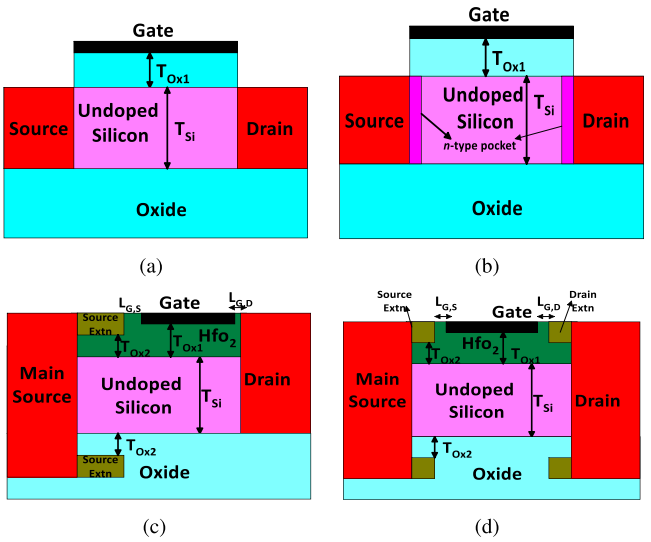

FIGURE 1. Device structures of (a) Conv. SB-MOSFET (b) Conv. DSL-SB-MOSFET (c) proposed asymmetric ED-DSL-SB-MOSFET with extension at source side (d) Proposed symmetric ED-DSL-SB-MOSFET with source and drain extensions.

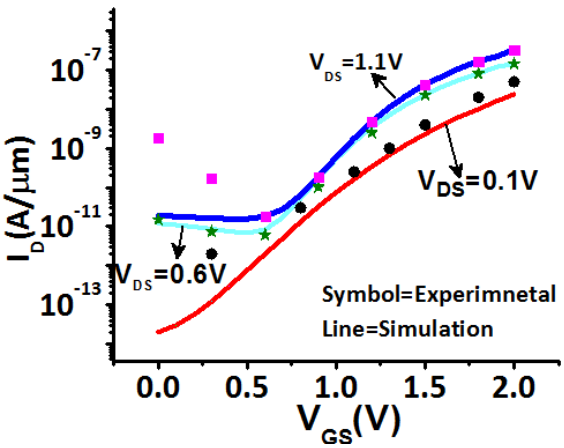

FIGURE 2. Calibration against the work done using experimental data as reported in [27].

T_{OX1} of 2nm, silicon film thickness T_{Si} of 10nm and the gate metal work-function of 4.65eV. Besides, the source and drain extensions have length of $L_{S,Extn}$ =$L_{D,Extn}$=3nm and the oxide thicknesses under these extension is T_{OX2}=1.0 nm. The work function used for main source and drain is 4.5eV, whereas for the extensions is 3.7eV (Hf). An important requirement for creating charge plasma in thin silicon film under source extension lengths is to keep silicon film thickness within Debye length [16].

III. RESULTS AND DISCUSSION

The proposed and the conventional devices have been simulated by using the device simulator Atlas [21]. The various models used in simulation study include *fldmob, conmob, drift diffusion, fermi, srh, BGN, consrh, and ust*. The field and concentration dependent mobilities have been captured by using *fldmob* and *conmob* mobility models. For capturing the transport process drift diffusion model has been used.

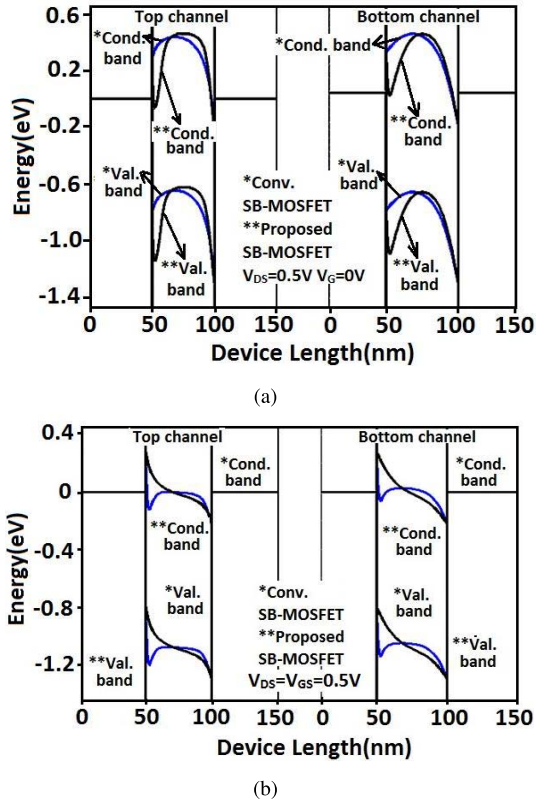

FIGURE 3. **Band diagram of Schottky Barrier MOSFET and the proposed ESD-DSL-SB-MOSFET in (a) under OFF condition (V_{DS}=0.5V V_{GS}=0V) and (b) under ON condition (V_{DS}=0.5V V_{GS}=0.5V).**

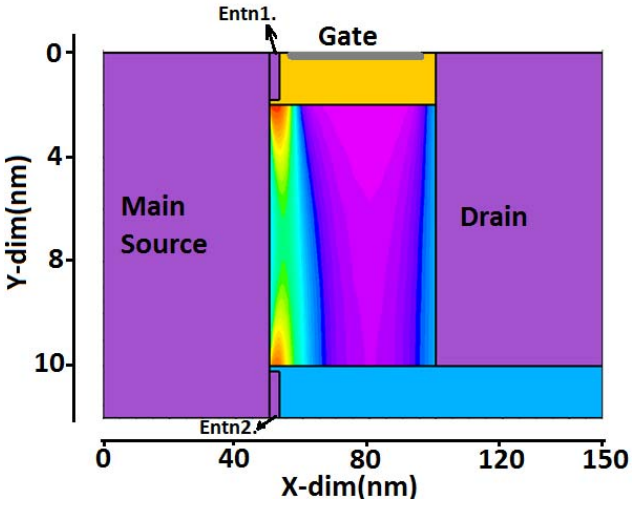

FIGURE 4. **Profile of ED-DSL-SB-MOSFET device.**

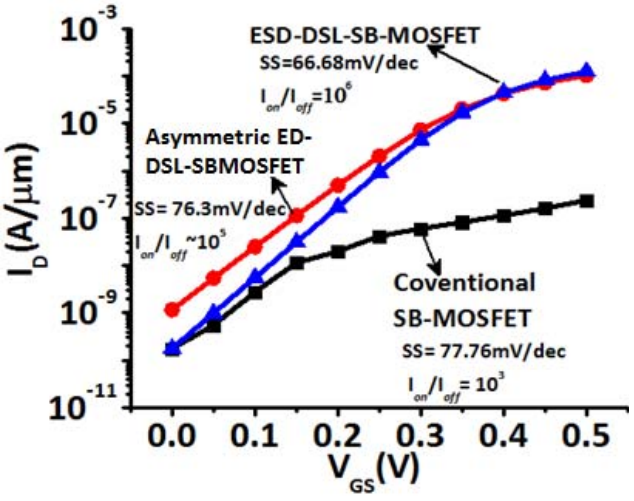

FIGURE 5. **Transfer characteristics of conventional SB-MOSFET, DSL-SB-MOSFET, and the proposed ED-DSL-SB-MOSFET.**

The Schottky tunneling phenomena has been captured by using *ust* model in the simulation. The simulation study over here is a calibrated one using the experimental data as reported in [27]. Fig. 2 shows a perfect agreement between the results reported in [27] and the simulated ones.

The energy band profile of the proposed ED-DSL-SB-MOSFET is shown in Fig. 3, in both the ON and OFF states. It clearly shows the thinning of the barrier width due to charge plasma DSL created by the source extensions at the top and bottom in an asymmetric ED-DSL-SB-MOSFET in comparison to the conventional SB-MOSFET, as shown in Fig. 3. Fig. 4 shows the profile of charge plasma by using source extensions at the top and bottom of the proposed asymmetric ED-DSL-SB-MOSFET.

The transfer characteristics of three devices are shown in Fig. 5. It clearly shows significantly improved performance in the proposed device in comparison to the conventional one. The ON current (for V_{GS} = 0.5V and V_{DS} = 0.5V) in the proposed symmetric ED-DSL-SB-MOSFET devices is of the order of $\sim 1.2 * 10^{-3}$A/μm, is $\sim$420 times higher than that of the conventional SB-MOSFET. The I_{ON}/I_{OFF} ratio is 1000 times higher in the proposed one in comparison to the conventional SB-MOSFET. Further there is improvement in subthreshold slope in the proposed device in comparison the conventional SB-MOSFET.

Further, we compared the performance of our proposed ED-DSL-SB-MOSFET device with the state of the art DSL-SB-MOSFET; it is clear that ED-DSL-SB-MOSFET shows significant improvement I_{ON}/I_{OFF} (10 times) ratio and sub-threshold slope (SS) ($\sim$12%) in comparison to state of the art DSL-SB-MOSFET.

The output characteristics of the proposed asymmetric and symmetric ESD-DSL-SB-MOSFET devices are shown in Fig. 6. For the asymmetric one, the drain current shows some dependence on V_{DS} due to channel length modulation effect. Further, it shows offset for lower V_{DS} due asymmetric nature of the ED-DSL-SB-MOSFET device, as shown in Fig. 6(a). This offset in the output characteristics of the proposed ED-DSL-SB-MOSFET has detrimental effects at circuit level and can cause reduction in the noise margin of the inverter. The offset problem can be mitigated by using symmetric device structure as shown in Fig. 1(d). Fig. 6(b)

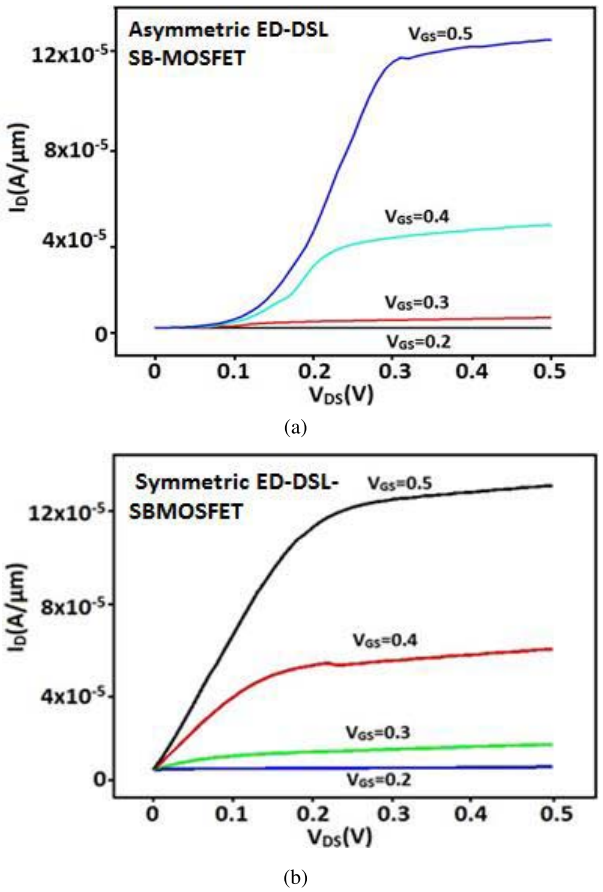

FIGURE 6. Output characteristics of (a) proposed asymmetric ED-DSL-SB-MOSFET and (b) proposed symmetric ED-DSL-SB-MOSFET.

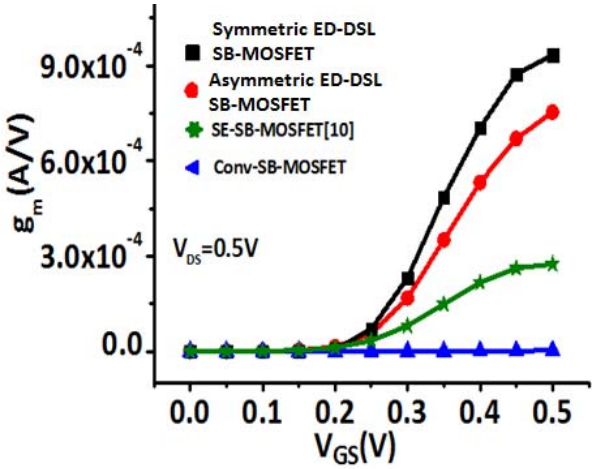

FIGURE 7. Transconductance of the proposed ED-DSL-SB-MOSFET, DSL-SB-MOSFET and Conventional SB-MOSFET devices.

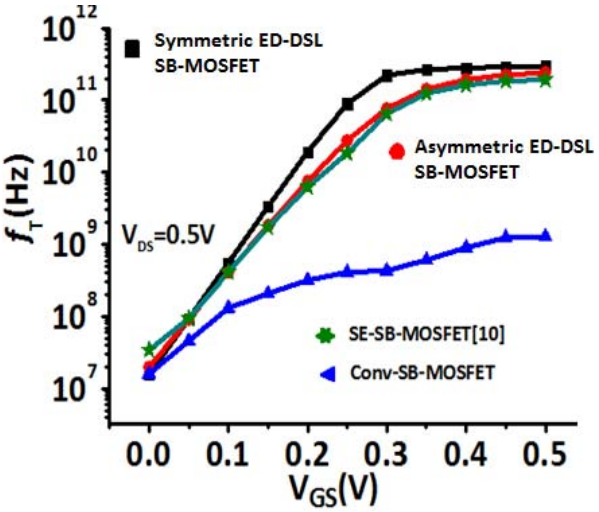

FIGURE 8. Cutoff frequency (f_T) of the proposed ED-DSL-SB-MOSFET, DSL-SB-MOSFET and Conventional SB-MOSFET devices.

shows the output characteristics of the symmetric ED-DSL-SB-MOSFET device without offset. The absence of offset in the proposed ED-DSL-SB-MOSFET device can be attributed to the smaller voltage drop in the drain side due to charge plasma DSL layer under drain extension.

Fig. 7 presents the transconductance (gm) plot as a function of V_{GS} for all the devices. It is clear that the higher gm is obtained in the proposed symmetric ED-DSL-SB-MOSFET in comparison to other devices. The higher transconductance can be attributed to the thinning of the Schottky tunneling width in the proposed devices due to creation of charge plasma DSL. The higher gm, thin tunneling width by electrostatically doped pocket, DSLs, have resulted in higher cutoff frequency (f_T) in the proposed ED-DSL-SB-MOSFET device in comparison to conventional DSL-SB-MOSFET and SB-MOSFET devices. Fig. 8 clearly shows that the f_T of the proposed ED-DSL-SB-MOSFET device (290GHz) is ∼290 times higher than the conventional SB-MOSFET (∼1GHZ) and DSL-SB-MOSFET (∼230GHZ) devices respectively.

Fig. 9 shows the influence of gate length (L_G) on the I_{ON}/I_{OFF} ratio and the SS of the proposed ED-DSL-SB-MOSFET and the DSL-SB-MOSFET devices. Although the I_{ON}/I_{OFF} ratio decreases in both the devices, however, the decrease is higher in the conventional doped DSL-SB-MOSFET than that observed in the proposed symmetric MOSFET. The value of I_{ON}/I_{OFF} ratio is higher at each gate length in the proposed device than in the conventional device. The SS also degrades with L_G scaling, however, it degrades more in the conventional one than in the proposed.

Fig. 10 compares an important performance measuring parameter which is the transconductance efficiency (gm/I_D) for all the devices. This value is highest in the proposed symmetric ED-DSL-SB-MOSFET in comparison to others. This can be attributed to the highest gm in the proposed symmetric ED-DSL-SB-MOSFET. The proposed asymmetric device has the second best gm/I_D parameter.

The value of source extension metal work-functions plays an important role in improving the performance of the ED-DSL-SB-MOSFET. Fig. 11 shows the effect of source extension metal work-function (WF) on I_{ON}/I_{OFF} ratio and f_T. It has been observed that increase in metal work-function

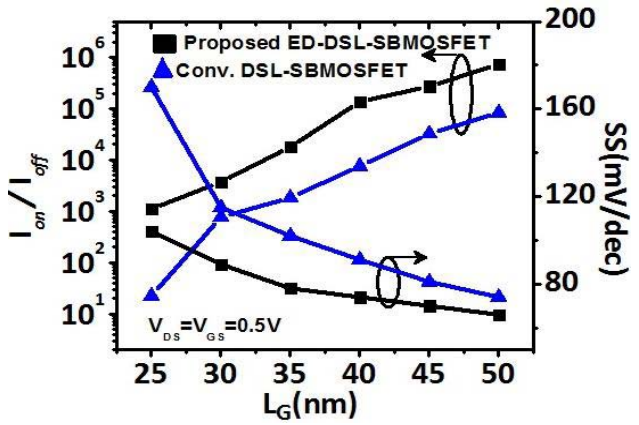

FIGURE 9. Effect of gate length (L_G) on I_{ON}/I_{OFF} ratio and SS of both the devices.

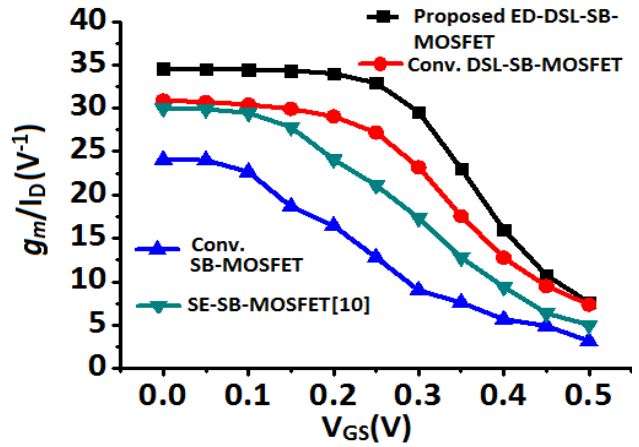

FIGURE 10. Plot of gm/I_D vs V_{GS}.

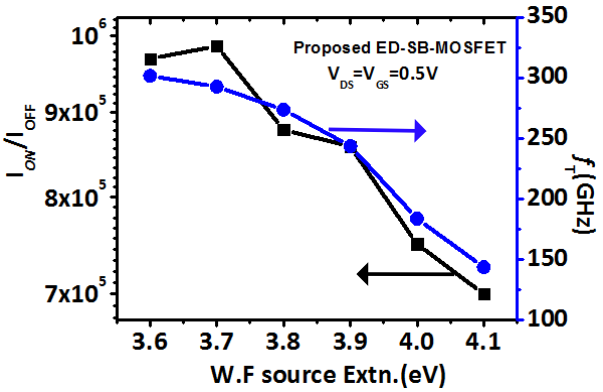

FIGURE 11. Effect of WF on the performance of the proposed device.

decreases the I_{ON}/I_{OFF} ratio and f_T of the ED-DSL-SB-MOSFET. This can be attributed to the decrease in electron concentration beneath of the source extensions, as source extension metal work-function is increased.

The short channel analyses of the proposed and the conventional devices have been performed. Fig. 12 shows the

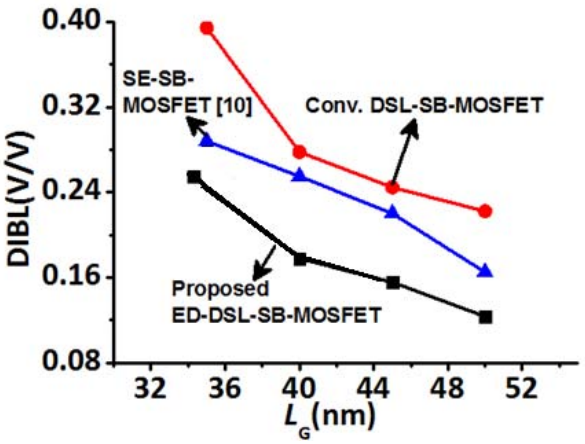

FIGURE 12. SCE analyses of proposed ED-DSL-SB-MOSFET, DSL-SB-MOSFET and SE-SB-MOSFET [10].

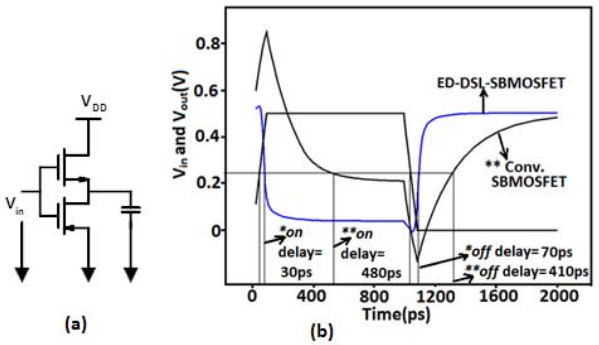

FIGURE 13. (a) CMOS based Inverter and (b) Transient examination of the ED-DSL-SB-MOSFET conventional SB-MOSFET.

magnitude of drain induced barrier lowering (DIBL) in the proposed ED-DSL-SB-MOSFET, DSL-SB-MOSFET and SE-SB-MOSFET devices when the gate length is scaled. It has been observed that the magnitude of DIBL is least in the proposed ED-DSL-SB-MOSFET in comparison to state of the art devices DSL-SB-MOSFET and SE-SB-MOSFET [10]. The effect of charge plasma and high k dielectric at the top is responsible for lowering the DIBL in the proposed ED-DSL-SB-MOSFET.

IV. CIRCUIT LEVEL PERFORMANCE INVESTIGATION

The performance of the proposed and the conventional devices has been investigated at the circuit level. The circuit level performance has been checked by designing CMOS inverters using the proposed ED-DSL-SB-MOSFET and the conventional SB-MOSFET devices. A comparison of the transient response of the inverters consisting of the proposed ED-DSL-SB-MOSFET and conventional SB-MOSFET is shown in Fig. 13. To get an idea about the total propagation delay caused by the inverters, we extracted the ON and OFF delays and it has been observed that the ON delay of the ED-DSL-SB-MOSFET (=30ps) based CMOS inverter is considerably small in comparison to the conventional

SB-MOSFET (=455ps) based inverter. On the other hand OFF delay in the proposed ED-DSL-SBMOSFET (=70ps) based inverter is nearly one 6^{th} as compared to conventional SB-MOSFET (=410ps) based inverter configuration. The small delay observed in the proposed ED-DSL-SB-MOSFET can be attributed to the high driving capability in the symmetric ED-DSL-SB-MOSFET.

V. CONCLUSION

In this work, novel electrostatically doped DSL Schottky barrier MOSFETs have been designed and simulated. The proposed device employ metal silicide source/drain regions with charge plasma based dopant segregation layers (DSL). Earlier conventional doping based DSLs have been used. However, the DSLs used in the proposed devices have been realized by using electrostatic doping or charge plasma concept. Two types of the ED-DSL-SB-MOSFETs have been designed, symmetric and asymmetric. Both the structures use charge plasma concept for the realization of DSLs and metallic source/drain regions, hence there are no doping related issues and can be fabricated at low temperatures. On comparing the ED-DSL-SB-MOSFET and conventional SB-MOSFET, it has been observed that ED-DSL-SB-MOSFET outperforms all the all conventional devices.

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