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An Innovative Indicator to Evaluate DRAM Cell Transistor Leakage Current Distribution

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ABSTRACT This paper is the first to propose an innovative method for measuring variations in dynamic random access memory (DRAM) cell transistors. Structural dispersion induces an extremely high cell leakage current, which determines aspects of DRAM performance such as refresh time (tREF). However, no method is currently available for evaluating variations, which is a serious problem in developing DRAM. Although the average leakage current from a test element group has been used as an index for determining cell leakage, it does not provide the distribution of unit cell leakage current. We find that cell leakage distribution can be calculated from the slope of the retention time-fail bit plot (defined as TF slope). A steep slope indicates a narrow cell leakage distribution, which corresponds to a narrower structural distribution, and therefore a long tREF. Using statistical models and experiments based on extensive data, our results confirm this relationship. Another impact and contribution of TF slope are that the development period can be saved because a wrong decision (which process is better) can be avoided. This method is used successfully as an indicator to estimate selected processes and to facilitate DRAM development.

INDEX TERMS DRAM, cell transistor, leakage current distribution, gate-induced drain leakage current (GIDL), process variation, refresh time, time-fail bit plot (TF slope), retention time.

I. INTRODUCTION

Leakage current is very sensitive to structural variations. It is exponentially proportional to the electric field (e-field), which depends on the distance between each node. Cell structure distributions determine cell characteristics such as leakage current and refresh time (tREF). The tREF is a significant factor in dynamic random-access memory (DRAM) chip performance. DRAM developers have struggled to find a proper index for analyzing leakage current that could define the outer bounds of tREF.

The leakage current of extreme tail cells (i.e., $10^{-7}-10^{-5}$ probability) can be very large (more than 10-100 times the average leakage current) [1]. Because extreme tail cells have a relatively short retention time, they determine tREF of a DRAM chip. Here retention time means how long a cell can hold data. Some cells with excessive leakage currents generate failure data-bit address (FBT), which means defective cells. This case is known as a tail bit. If the proportion of tail bits exceeds several thousand per gigabit (Gb), redundancy resources can be completely spent, and result in the DRAM chip no longer functioning.

The gate-induced drain leakage current (GIDL) is known to be major cell leakage current. To monitor GIDL, a test element group (TEG) is used. However, GIDL of a unit cell is so small (0.1–10 fA/cell) that it is impossible to measure each cell leakage current. A cell array block in TEG comprises many cells (>100,000 approximately), with a total leakage current greater than the measurement limitations of the instrument (approximately 10 pA). Thus, we can obtain the average GIDL (total leakage current divided by the number of cells of array in TEG). Currently, GIDL in TEG is the only indicator for predicting tREF. However, the average GIDL cannot give any information regarding GIDL distribution (i.e., the large leakage current of extreme tail cells). Therefore, mismatches between the average GIDL in TEG and tREF has been reported [2]. Using statistical models and

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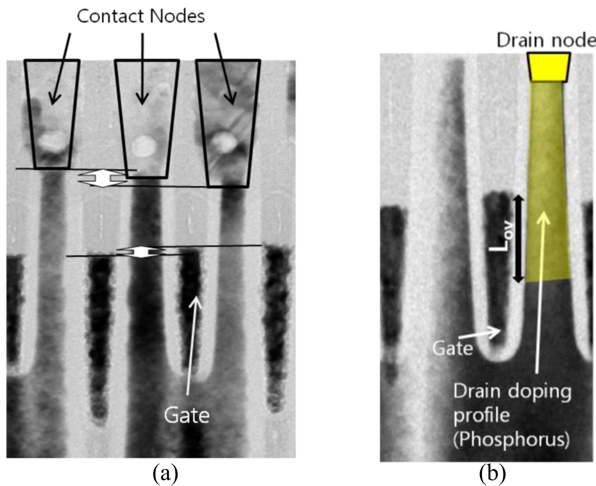


FIGURE 1. (a) Transmission electron microscope (TEM) image of DRAM cells. There is always structure and process-induced variations. Ideally, gate materials in a buried-channel-array transistor (BCAT) have a uniform depth. However, depths actually differ from each other because of process variations. (b) The overlap length between drain node and gate edge (Lov) in a DRAM cell transistor.

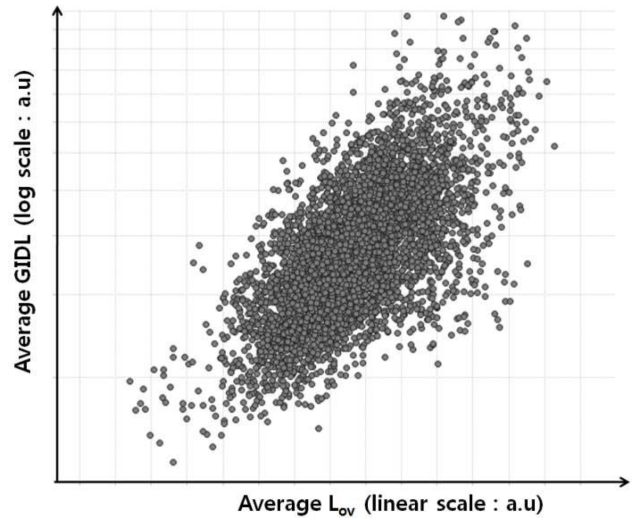


FIGURE 2. Average GIDL increases exponentially with L_{ov} (experimental data). Average GIDL and Lov are measured with TEG. L_{ov} is calculated from overlap capacitance between gate and drain (indirect method).

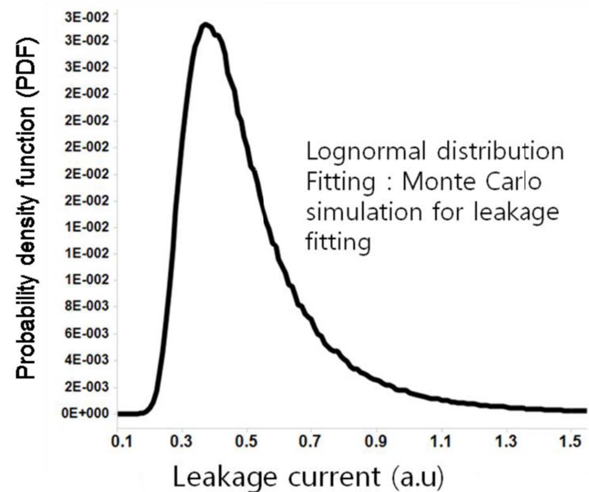


FIGURE 3. Lognormal distribution in a DRAM cell. Every transistor leakage current follows a lognormal distribution.

experimentation, this study is the first to analyze the reason for this mismatch between GIDL in TEG and tREF and calculate large cell leakage current at low probability which determines tREF, Additionally, we propose a new index for evaluating structural distribution, which is a crucial index for analyzing structure/process variations. We also study the cell variations that affect tREF and investigate how to evaluate this distribution.

II. CELL LEAKAGE MECHANISM AND STRUCTURAL VARIATIONS

Hurkx *et al.*'s [3] model explains the cell leakage mechanism as being related to trap energy level, trap density, and e-field. If a stronger e-field exists in the source or drain of the cell (S/D), it may induce a large leakage current and seriously degrade tREF. Structural variations always exist in DRAM cell arrays, inducing the leakage current distribution (Fig. 1(a)). The leakage current (i.e., GIDL) is exponentially proportional to the overlap length between drain node and gate edge (L_{ov}), because L_{ov} affects the electric field as shown in Fig. 1(b). Fig. 2 shows the experimental results of the relationship between GIDL and L_{ov} in a DRAM cell transistor. Therefore, structural variations induce L_{ov} variations, which is the main factor in leakage current variations.

Leakage current is a function of the number of defects, trap energy level, and e-field [3]. Each factor is assumed to have a normal Gaussian distribution in DRAM cells. Therefore, the leakage current distribution should follow a lognormal distribution, as shown in Fig. 3 [4]. Leakage distribution originates from structural variations. Several methods, including indirect methods, can be used to measure the leakage current distribution. Images from the transmission electron microscope (TEM) or the scanning electron microscope (SEM) can provide direct information about the vertical cell structures influencing cell leakage (Figs. 1(a) and 1(b)), but these images cannot be used to quantify leakage current.

Another method is to measure cell array leakage using TEG (Fig. 4), as mentioned above. Since each cell current is so small (lower than the limitations of the measurement instrument), in order to measure cell leakage (specifically, GIDL), many cells (over 100,000) are combined. The gates of each cell are combined and the same voltage can be applied to the gates (negative bias is applied in order to measure GIDL). All drains are combined as well. Although the GIDL of each cell is very small, GIDL in an array cell is sufficiently large to measure. If the measured leakage current is divided by the number of array cells, the average GIDL can be determined. This is a typical way to measure GIDL.

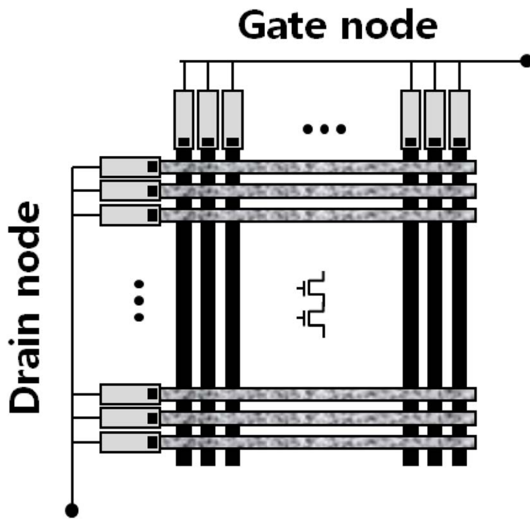


FIGURE 4. Schematic of a TEG module. TEG is typically located in the scribe lane. Average GIDL and L_{ov} can be measured with TEG.

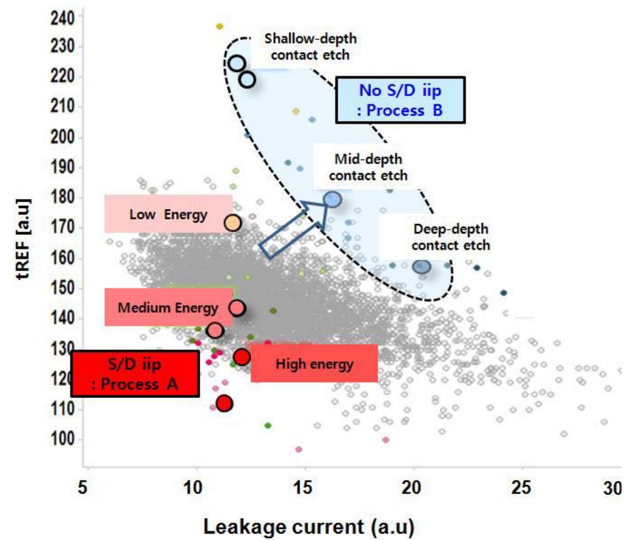


FIGURE 5. tREF vs. GIDL plot. The GIDL (X axis) is measured from TEG in this plot. Theoretically, tREF should be inversely proportional to GIDL. However, Process B does not follow this trend.

TEG is the only tool used to directly measure cell leakage. In general, the retention time of each cell is inversely proportional to leakage current because the charge of each cell capacitor can be eliminated by leakage current from cell transistor. However, there can be discordance between average GIDL from TEG and tREF from DRAM chip (Fig. 5), which means that the relationship between tREF and average leakage current cannot be simply predicted. Ion implantation process (iip) can affect cell leakage current, too. The S/D iip process (Process A) can make the S/D doping profile broad, which causes a weak e-field when voltage is applied. Therefore, the GIDL of Process A becomes smaller than that of the no S/D iip process (Process B) because the e-field at S/D of Process B increases due to the abrupt doping profile. However, contrary to the expectation, the tREF of Process A is shorter than that of Process B. This phenomenon can be explained by the distribution of cell leakage. As mentioned above, a GIDL determined from TEG reveals only an average value. S/D iip cannot help inducing severe random dopant fluctuation (RDF) due to high ion implantation energy [5]. Dopant distribution from RDF causes L_{ov}distribution, which becomes the main reason of cell leakage current distribution. The average GIDL at Fig. 5 is measured from TEG, which means average cell leakage current. Though Process A has low e-field (i.e., low average GIDL), it can be affected by severe RDF (i.e., large cell leakage current distribution). With Process A, the tREF can be improved as S/D iip energy decreases. The tREF with Process B also increases as drain etch depth becomes shallow as shown in Fig. 5.

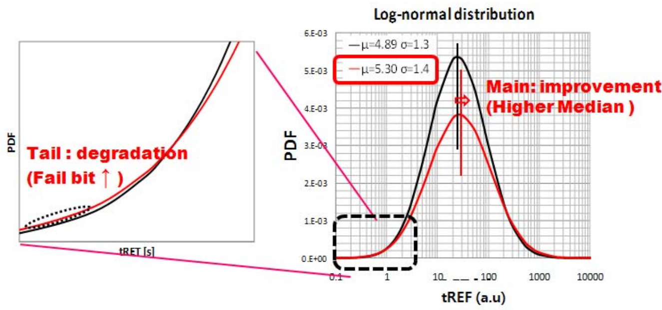
Although it is crucial to identify the leakage distribution in chip, it is very difficult to measure it using TEG. Therefore, a novel model should be considered with statistics. Cell leakage has a lognormal distribution (Fig. 3) and ranges from a very small (<0.1 fA) to a very large (hundreds of fA) leakage current in the DRAM cell arrays, which consist of several Gb.

III. LEAKAGE DISTRIBUTION

If a unit cell loses its data because of leakage, its results can be counted as an FBT with retention time. Although leakage current depends on e-field and defect density, it varies from cell to cell because of structural variations. Leakage current is exponentially related to e-field, and defect and e-field are assumed to have normal Gaussian distributions in the DRAM chip. Therefore, the leakage current distribution follows a lognormal distribution [4].

Fig. 6 shows how the leakage current distribution influences the fail bit-retention time plot. As the cell leakage distribution worsens (i.e., the standard deviation (σ) grows), the extreme tail cells have a higher leakage current, even for a smaller mean value (μ).

Fig. 7 shows the simulated plots. Lognormal distributions with different μ and σ values are determined by statistical theory [6]. As mentioned above, a very high leakage current in extreme tail cells causes a low tREF. We define the slope herein as the time–FBT slope (TF slope), and $1/\sigma$ is proportional to the TF slope in the low CDF region ($<10^{-5}$), as shown in Fig. 7. The TF slope indicates the retention time variation of tail cells and indicates cell leakage current variations. Because process-induced structural variations influence the leakage current distribution, it is possible to estimate process stability based on the TF slope. The mismatch between GIDL in TEG and tREF (Fig. 5) can be understood by the TF slope. In Fig. 8, he cell leakage distribution plot changes with standard deviation. Inverse error function can be expressed as many ways [7]. Because the interested region is focused on extremely low probability ($< 10^{-5}$; < 10,000 fail bits out of 1giga bits), the



$$Log-normal_distribution$$
$$CDF(x)=\frac{1}{2}\left[1+erf\left(\frac{\ln x-\mu}{\sigma\sqrt{2}}\right)\right]$$
$$Mean(x)=E(x)=\exp\left(\mu+\frac{1}{2}\sigma^2\right)$$
$$Stdev(x)=\exp\left(\mu+\frac{1}{2}\sigma^2\right)\sqrt{\exp(\sigma^2)-1}=E(x)\sqrt{\exp(\sigma^2)-1}$$
$$Mode(x)=\exp(\mu-\sigma^2)$$
$$Median(x)=\exp(\mu)$$

FIGURE 6. The relation between the leakage current distribution and fail bit plot with retention time. The μ and σ are arbitrarily chosen for understanding.

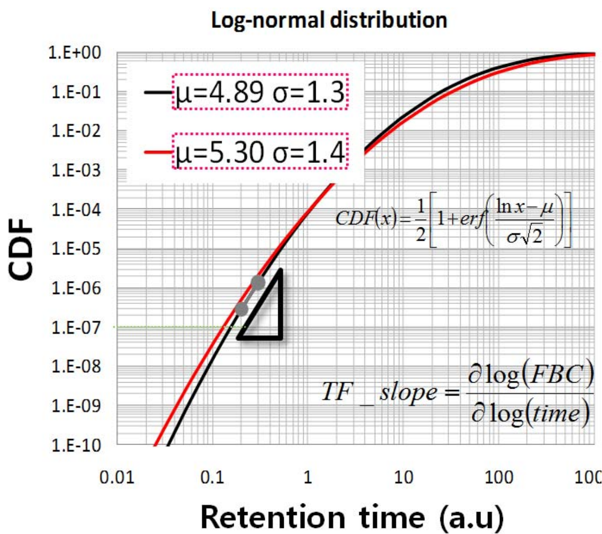
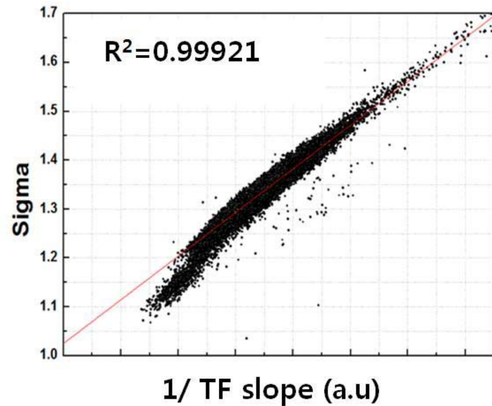


FIGURE 7. Simulated lognormal distribution with different mean value (μ) and standard deviation (σ). The x-and y-axes are the log scales of time and CDF, respectively.



$$y=\frac{1}{2}\left[1+erf\left(\frac{\ln x-\mu}{\sigma\sqrt{2}}\right)\right], x=time, y=CDF\ (or\ _FailureBits)$$

$$\frac{1}{\sigma}=\sqrt{2}\times\frac{erf^{-1}(2y_2-1)-erf^{-1}(2y_1-1)}{\ln(x_2)-\ln(x_1)}$$
$$\approx\sqrt{2}\times\frac{(-1.35543+0.33366\times\log(y_2))-(-1.35543+0.33366\times\log(y_1))}{\ln(x_2)-\ln(x_1)}$$
$$=\sqrt{2}\times 0.33366\times\frac{\log(y_2)-\log(y_1)}{\ln(x_2)-\ln(x_1)}$$
$$\propto(tRET-slope)$$

FIGURE 8. The relationship between the 1/(TF slope) and standard variation. This relationship has been demonstrated statistically and experimentally. Inverse error function can be expressed as many ways. In this approximate expression, a logarithmic function is selected which is extracted using a data analysis software such as Origin [8].

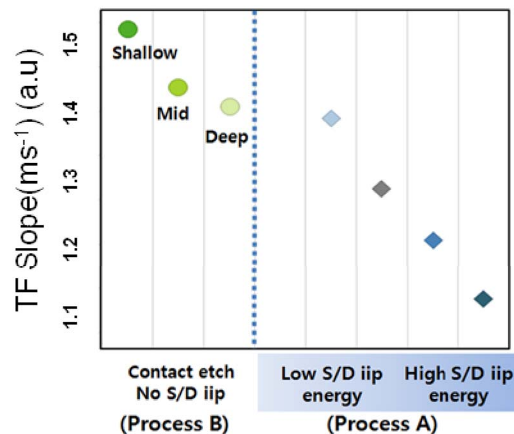


FIGURE 9. The TF slopes for each process are compared; As S/D iip energy or contact etch depth decreases, the TF slope increases (i.e., the distribution is improved).

approximate expression is selected as a logarithmic function. We use a data analysis software such as Origin [8] which can be much simpler than Maclaurin series in this region. A small variation causes the retention time–FBT plot to have a steeper slope.

IV. IMPACT AND CONTRIBUTION

In Fig. 9, the TF slopes of Processes A and B (from Fig. 5) are compared. The TF slope of Process B is much steeper than that of Process A. Thus, Process B has smaller variations, although their average leakage currents (i.e., GIDL in TEG) are larger than that of Process A. The DRAM tREF increases with the TF slope.

Process variation or damages are estimated with TF slope. Drain contact node depth variation induced by process affects cell leakage variation obviously as mentioned before. The drain node depth can be measured with a bunch of TEM images (more than 100 points). The sigma of node depth is well matched with TF slope as shown in Fig. 10. TF slope

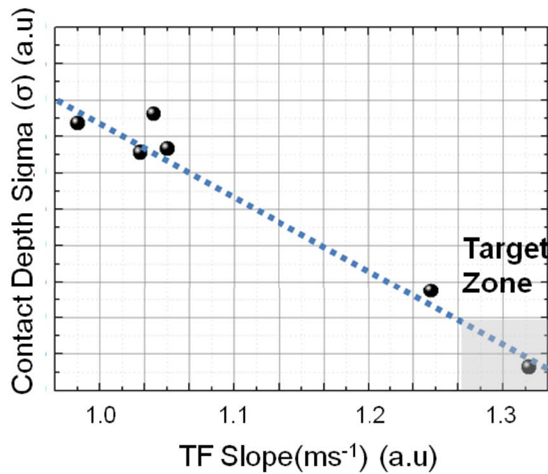


FIGURE 10. The TF slopes with process variation. Process window can be provided with TF slope.

can provide the process guideline. In DRAM development, process with low TF slope has been excluded, therefore the development period can be saved because a wrong decision (which process is better) can be avoided.

Thus, the TF slope can play an important role in estimating new processes (e.g., S/D iip or drain node contact etch process, see Figs. 9 and 10) with respect to the distribution, and provides the first proper index for doing so. This development represents a significant advance.

V. CONCLUSION

In this paper, we demonstrate for the first time that the TF slope is an outstanding index for evaluating cell leakage distributions induced by structural/process variations. Because retention time is directly derived from cell leakage, the standard variation of the leakage current is inversely proportional to the slope of the retention time–the FBT plot. To date, GIDL in TEG has been the only measurement available for estimating cell leakage currents. But this measurement provides only the average leakage current of the cell array and yields no information about any extreme tail cell leakage. As a result, undesirable processes may be chosen, which could delay project development. We explained the mismatch between GIDL in TEG and tREF in this study. GIDL in TEG indicates only an average leakage current, but tREF is determined by the extreme cell leakage (i.e., distribution). Despite the process selected to decrease the average leakage current (low GIDL in TEG), tREF can be low if its process has a large distribution. Low TF slope indicates large process variations.

The TF slope is a very effective indicator for estimating processes in terms of the cell leakage distribution. The TF slope represents a significant contribution to DRAM development and contributes DRAM lead time reduction.

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