

Received 29 June 2017; revised 16 August 2017; accepted 2 October 2017. Date of publication 6 October 2017; date of current version 26 April 2018. The review of this paper was arranged by Editor H. Wakabayashi.

Digital Object Identifier 10.1109/JEDS.2017.2760344

Pretreatment Effects on High-k/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS Interface Properties and Their Physical Model

CHIAKI YOKOYAMA¹, CHI-YU CHANG¹ (Member, IEEE), MITSURU TAKENAKA² (Member, IEEE), AND SHINICHI TAKAGI² (Member, IEEE)

¹ Department of Electrical and Electronic Engineering, University of Tokyo, Tokyo 113-0032, Japan

² Department of Electrical Engineering and Information Systems, School of Engineering, University of Tokyo, Tokyo 113-0032, Japan

CORRESPONDING AUTHOR: C. YOKOYAMA (e-mail: cyokoyama@mosfet.t.u-tokyo.ac.jp)

This work was supported by JST CREST, Japan, under Grant JPMJCR1332.

ABSTRACT The electrical and physical properties of atomic layer deposition high-k (Al_2O_3 and HfO_2) / $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x = 0.53, 0.7,$ and 1) MOS interfaces with $(\text{NH}_4)\text{S}_y$, BHF, and HF pretreatment are examined. It is found that, as the In content (x) becomes higher, $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interfaces with BHF and HF cleaning show better C - V characteristics and lower interface state density (D_{it}) than with $(\text{NH}_4)\text{S}_y$ pretreatment. Also, the amounts of arsenic oxides, evaluated by X-ray photoelectron spectroscopy, at the high In content $\text{Al}_2\text{O}_3/\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interfaces are found to increase with BHF and HF cleaning than with $(\text{NH}_4)\text{S}_y$ cleaning. These results suggest that arsenic oxides can contribute to passivation of high-k/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interface defects and the decrease in D_{it} for $x = 0.7$ and 1 . Finally, we propose a physical model to explain the relationship between possible interface defects responsible for D_{it} and the pretreatment effects with the different In contents.

INDEX TERMS BHF, C - V , D_{it} , HF, InAs, InGaAs, MOS interface, $(\text{NH}_4)\text{S}_x$, pre-cleaning, pre-treatment.

I. INTRODUCTION

Since 1960s, the scaling law for Si MOSFETs has contributed to the integration of modern LSI. However, because of the physical properties of Si, the performance enhancement due to the scaling law is reaching its limitation [1]. As new methods which do not rely on the scaling law, high-mobility semiconductor channels with high-k insulators are attracting much attention. Especially, $\text{In}_x\text{Ga}_{1-x}\text{As}$ with $x = 0.53$ to 1 has high electron mobility, and so it is expected as a channel material of future n -channel MOSFETs. However, high-k/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ interfaces have the much higher interface state density (D_{it}) than the SiO_2/Si interface due to some defects [2]–[4]. Interface states at MOS interfaces degrade the drive current and the sub-threshold swing of MOSFETs. Since this problem is very serious, it is important to reduce the amount of D_{it} [5] at the high-k/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ interfaces.

Several directions for reducing D_{it} at the high-k/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ interfaces have already been proposed. One preferable direction for realizing better interfaces is the

removal of the native oxides of $\text{In}_x\text{Ga}_{1-x}\text{As}$, because the poor $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interface quality is often attributed to the low quality native oxides. In order to clean semiconductor surfaces or reduce amounts of the native oxides, a pre-cleaning treatment is usually performed before deposition of gate insulators on substrates [6], [7]. Especially, S cleaning ($(\text{NH}_4)\text{S}_y$ pre-treatment) is commonly used for atomic layer deposition (ALD) $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface formation [8]–[10]. This is because sulfur atoms passivate the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces after removing the native oxides and prevent the surfaces from oxidation in the air [11], [12]. This is attributable to a strong surface passivation nature of Sulfur atoms.

Furthermore, it is well recognized that TMA ($\text{Al}(\text{CH}_3)_3$), which is commonly used in Al_2O_3 ALD as a precursor, can remove the native oxides in an early stage of Al_2O_3 ALD, which is called the self-cleaning effect of TMA [13]. As a result, the combination of Sulfur cleaning and Al_2O_3 ALD using TMA have been considered as one of the optimum gate insulator formation processes for realizing the native oxide

free In $_{0.53}$ Ga $_{0.47}$ As surfaces. Thus, this process has been commonly used for In $_{0.53}$ Ga $_{0.47}$ As MOS interface formation so far.

On the other hand, it has recently been reported that BHF cleaning can produce lower D_{it} at HfO $_2$ /InAs [14] and Al $_2$ O $_3$ /ultra-thin InAs/GaSb [15] MOS interfaces than S cleaning. These results suggest that the optimum pre-cleaning can be dependent on the In content (x) of In $_x$ Ga $_{1-x}$ As. However, there is no systematic study on the pre-cleaning effects of In $_x$ Ga $_{1-x}$ As with changing the In content. In addition to the technological importance, these data are expected to be quite informative to better understanding of physical origins of D_{it} at In $_x$ Ga $_{1-x}$ As MOS interfaces. Therefore, in this paper, we examine the ALD high- k (Al $_2$ O $_3$, HfO $_2$)/In $_x$ Ga $_{1-x}$ As MOS interfaces properties with different In contents ($x = 0.53, 0.7,$ and 1) by changing the pre-treatment among (NH $_4$)S $_y$, BHF, and HF [16]. Here, HF cleaning is also examined in this work to discriminate the effects of NH $_4$ F and HF on the MOS interface properties by comparing the results of BHF and HF cleaning.

II. EXPERIMENTS

Al $_2$ O $_3$ /In $_x$ Ga $_{1-x}$ As MOS capacitors ($x = 0.53, 0.7,$ and 1) were fabricated with S, BHF, or HF cleaning. In addition, HfO $_2$ /In $_x$ Ga $_{1-x}$ As MOS capacitors ($x = 0.53$ and 1) were also prepared with S or BHF cleaning in order to examine the influence of the difference in gate insulators. The treatment was carried out just by soaking the substrates into each wet chemical solution. The each soaking time of the substrates in the S, BHF, and HF cleaning was 5 min, 15sec, and 15sec after acetone cleaning. The concentration of (NH $_4$)S $_y$, BHF and HF were 0.6-1%, 22% and 50%, and the temperatures of all solutions were room temperature (R.T.). Fig. 1 shows the process flow of the MOS capacitors and the schematic illustrations of the starting substrates. The three types of the starting substrates were prepared. Two of them had n -type epitaxial In $_x$ Ga $_{1-x}$ As layers on InP substrates, grown by metal organic vapor phase epitaxy (MOVPE). The structures were composed of 500-nm-thick Si-doped ($N_D \sim 5 \times 10^{15} \text{ cm}^{-3}$) n -In $_{0.53}$ Ga $_{0.47}$ As grown on n^+ -InP(001) and of 300-nm-thick Si-doped ($N_D \sim 3 \times 10^{16} \text{ cm}^{-3}$) n -In $_{0.7}$ Ga $_{0.3}$ As grown on n^+ -InP(001). Since the thickness of the In $_{0.7}$ Ga $_{0.3}$ As layer is thicker than the critical thickness, strain is fully relaxed. According to the previous results [17], [18], In $_{0.7}$ Ga $_{0.3}$ As n -MOSFETs fabricated on fully-relaxed In $_{0.7}$ Ga $_{0.3}$ As/InP substrates have shown the good electrical characteristics, suggesting that dislocations or defects generated by fully relaxation of the In $_{0.7}$ Ga $_{0.3}$ As substrates could not have any significant influence on the MOS interface properties. Also, the third starting substrates were un-doped ($N_D \sim 2 \times 10^{16} \text{ cm}^{-3}$) n -InAs substrates.

90-cycle-Al $_2$ O $_3$ ($\sim 9.4\text{nm}$) was deposited by ALD at 200 °C on each substrate after S, BHF, or HF cleaning. The precursors for Al $_2$ O $_3$ were TMA and H $_2$ O as the liquid sources. Also, 100-cycle-HfO $_2$ ($\sim 9.3\text{nm}$) was deposited by ALD at 200 °C on n -In $_{0.53}$ Ga $_{0.47}$ As and n -InAs substrates

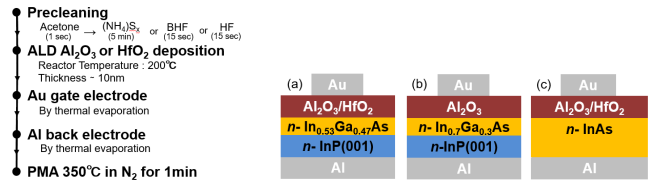


FIGURE 1. Process flow of In $_x$ Ga $_{1-x}$ As ((a) $x = 0.53,$ (b) $x = 0.7,$ and (c) $x = 1$) MOS capacitors and the schematic illustrations of the starting substrates.

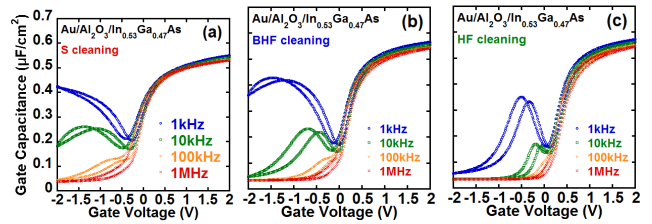


FIGURE 2. C-V characteristics of Au/Al $_2$ O $_3$ /In $_{0.53}$ Ga $_{0.47}$ As MOS capacitors with (a) S cleaning, (b) BHF cleaning, and (c) HF cleaning measured at R.T.

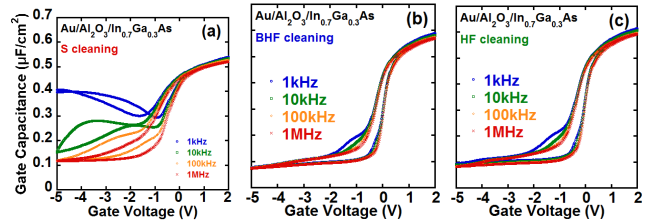


FIGURE 3. C-V characteristics of Au/Al $_2$ O $_3$ /In $_{0.7}$ Ga $_{0.3}$ As MOS capacitors with (a) S cleaning, (b) BHF cleaning, and (c) HF cleaning measured at 180 K.

after S or BHF cleaning. The precursor and the oxidant of ALD HfO $_2$ were Hf[N(C $_2$ H $_5$)CH $_3$] $_4$ (TDMAHf) and H $_2$ O, respectively. Next, the Au gate electrode was formed and Al was deposited as the back contact by thermal evaporation. Finally, we performed post metallization annealing (PMA) at 350 °C for 1 min in N $_2$ ambient for all the MOS capacitors to improve the interface properties.

In order to examine the electrical properties of the MOS interfaces, we performed C-V measurements and estimated D_{it} for all the MOS capacitors with a gate area $\sim 3 \times 10^{-4} \text{ cm}^2$ by using the Terman method and the conductance method. Also, XPS analyses were performed to investigate the MOS interface structures.

III. RESULTS AND DISCUSSIONS

The C-V characteristics at the measurement frequencies of 1 k, 10 k, 100 k and, 1 MHz for the ALD Al $_2$ O $_3$ /In $_x$ Ga $_{1-x}$ As MOS capacitors. Fig. 2 shows the C-V characteristics of Al $_2$ O $_3$ /In $_{0.53}$ Ga $_{0.47}$ As MOS capacitors with (a) S cleaning, (b) BHF cleaning, and (c) HF cleaning measured at R.T. Fig. 3 and Fig. 4 also show the C-V curves of Al $_2$ O $_3$ /In $_{0.7}$ Ga $_{0.3}$ As and Al $_2$ O $_3$ /InAs MOS capacitors, respectively, with (a) S cleaning, (b) BHF cleaning,

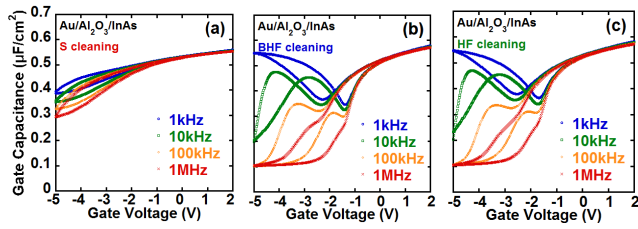


FIGURE 4. C - V characteristics of Au/ Al_2O_3 /InAs MOS capacitors with (a) S cleaning, (b) BHF cleaning, and (c) HF cleaning measured at 180 K.

and (c) HF cleaning. Here, the measurement temperature is 180 K. As the In content becomes higher, the response frequency of minority carriers becomes higher because of the narrower bandgap and, thus, the minority carrier response more clearly appears with increasing the In content. Therefore, the lower temperature is used for the C - V measurements at $x = 0.7$ and 1. Here, we measured the C - V characteristics at different low temperatures and checked if the C - V characteristics under the high-frequency limit can be obtained at 1 MHz. This is because the measured C - V characteristics are analyzed by the Terman method for extracting the energy distribution of interface states. The maximum capacitance of $\sim 0.6 \mu\text{F}/\text{cm}^2$ for each sample showed almost no differences. The hysteresis in the C - V characteristics becomes larger with an increase in the In content, suggesting that the amount of slow traps increases as the In content becomes higher. At $x = 0.53$, there seems no significant difference among these three types of cleaning. The small frequency dispersions in the accumulation regions and the depletion regions, and the steep capacitance changes at 1 MHz indicate the good MOS interface properties for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

At $x = 0.7$, the smaller frequency dispersion in the depletion and inversion regions are observed with BHF and HF cleaning than with S cleaning. The smaller humps in the weak inversion region with BHF/HF cleaning than with S cleaning also suggest smaller D_{it} for BHF/HF cleaning. Furthermore, the capacitance of InAs ($x = 1$) with S cleaning does not change significantly, meaning that the surface potential is almost pinned because of a large amount of D_{it} . Since the capacitance value in the accumulation region with S cleaning is close to the oxide capacitance, a large amount of interface states locates around from the conduction band edge to mid gap. In BHF cleaning and HF cleaning, on the other hand, much larger capacitance change is observed. These results clearly show that the interface properties with BHF cleaning or HF cleaning are much better than those with S cleaning. In addition, there is no difference between BHF cleaning and HF cleaning.

Next, in order to further examine if the surface treatment before ALD is the essential factor or not for the difference in the interface properties, the gate insulator is changed from ALD Al_2O_3 to ALD HfO_2 . Here, we evaluated the C - V characteristics of the $\text{HfO}_2/\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x = 0.53$

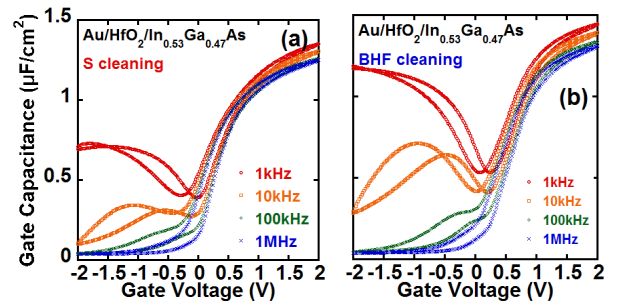


FIGURE 5. C - V characteristics of Au/ HfO_2 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with (a) S cleaning and (b) BHF cleaning measured at R.T.

and 1) MOS capacitors, treated by S cleaning and BHF cleaning. Fig. 5 and Fig. 6 show the C - V characteristics for $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors measured at R.T. and HfO_2/InAs MOS capacitors measured at 150 K, respectively, treated by (a) S cleaning and (b) BHF cleaning. In the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors, the C - V curves with S cleaning are superior to those with BHF cleaning. The difference seems to be more evident than that in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs, shown in Fig. 1. These differences of the cleaning effect on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ between Al_2O_3 and HfO_2 are attributable to any difference of surface chemistry in Al_2O_3 and HfO_2 ALD such as the reduction power of the precursors or the reactions of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface and the precursors. It is found, on the other hand, in the HfO_2/InAs MOS capacitors that the C - V curves with BHF cleaning shows better characteristics in terms of the interface properties than those with S cleaning in higher In content, which is the same trend as observed in the Al_2O_3 MOS capacitors. We can conclude from these results that the present results and trends are inherent properties of $\text{In}_x\text{Ga}_{1-x}\text{As}$ surfaces treated by S, BHF and HF, irrespective of the gate insulators.

In order to quantitatively examine the interface properties, the energy distribution of D_{it} was estimated by the Terman method using the 1 MHz C - V curves. In the analysis using the Terman method, we adopted the conventional semi-classical model, where the Poisson's equation and the Boltzmann distribution under a parabolic band model considering only the Γ valley for the conduction band were employed for calculating the carrier concentrations and the potentials. Also, the quantum effect in MOS accumulation layers has not been taken into consideration. As a result, the accuracy of D_{it} inside the conduction band would be questionable in the present calculations.

Fig. 7 (a), (b), and (c) show the energy distributions of D_{it} at the $\text{Al}_2\text{O}_3/\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interfaces with the In content of 0.53, 0.7, and 1, respectively. Here, the energy of the conduction band edge (E_c) of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$, and InAs is positioned at 0.76 eV, 0.59 eV, and 0.36 eV, respectively. First, at $x = 0.53$, as shown in Fig. 7 (a), there is no significant difference in D_{it} near the conduction band

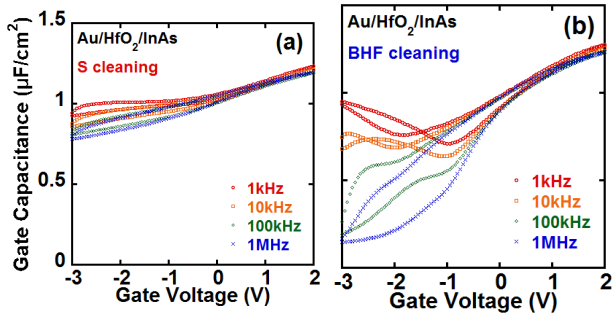


FIGURE 6. C-V characteristics of Au/HfO₂/InAs MOS capacitors with (a) S cleaning and (b) BHF cleaning measured at 150 K.

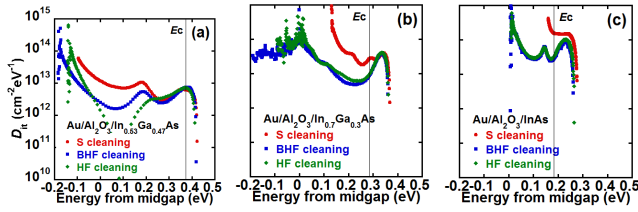


FIGURE 7. Energy distributions of D_{it} of Au/Al₂O₃/In_xGa_{1-x}As ((a) $x = 0.53$, (b) $x = 0.7$, and (c) $x = 1$) with S cleaning, BHF cleaning, and HF cleaning, evaluated by the Terman method.

edge among the three cleaning methods. Note that D_{it} evaluated by the conductance method is typically shown in this energy range. On the other hand, BHF and HF cleaning provide lower D_{it} around the mid gap and in the valence band side than S cleaning. At $x = 0.7$, as shown in Fig. 4 (b), D_{it} with BHF and HF cleaning becomes lower even near the conduction band edge than those with S cleaning. Furthermore, this trend becomes stronger for the In content of 1, as shown in Fig. 7 (c). These results mean that, as the In content (x) of $\text{In}_x\text{Ga}_{1-x}\text{As}$ is higher, D_{it} with BHF/HF cleaning becomes lower than with S cleaning. The same results were also confirmed in D_{it} evaluated by the conductance method. Fig. 8 shows the energy distributions of D_{it} , evaluated by the conductance method, with (a) S cleaning, (b) BHF cleaning, and (c) HF cleaning. Note that D_{it} for Al₂O₃/InAs MOS capacitors treated by S cleaning could not be obtained by the conductance method because of no detectable conductance peak. This is attributable to the response frequency of interface states higher than 1 MHz through the strong pinning of surface potential around the conduction band edge. As a result, we can conclude that, with increasing the In content, BHF and HF cleaning are more effective in reducing D_{it} at the $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interfaces than S cleaning. However, it is also observed that the amount of D_{it} itself becomes larger as a whole with an increase in the In content.

It is found, on the other hand, that there is no significant difference between BHF cleaning and HF cleaning, especially for the In content of 0.7 and 1. Thus, we can also conclude from this result that HF-based species are playing

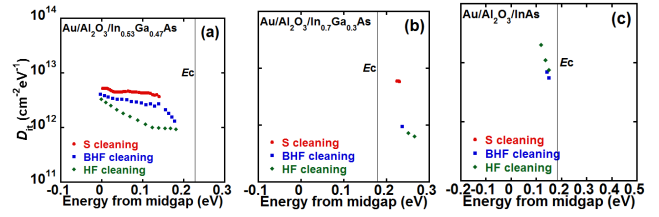


FIGURE 8. Energy distributions of D_{it} of Au/Al₂O₃/In_xGa_{1-x}As ((a) $x = 0.53$, (b) $x = 0.7$, and (c) $x = 1$) with S cleaning, BHF cleaning, and HF cleaning, evaluated by the conductance method.

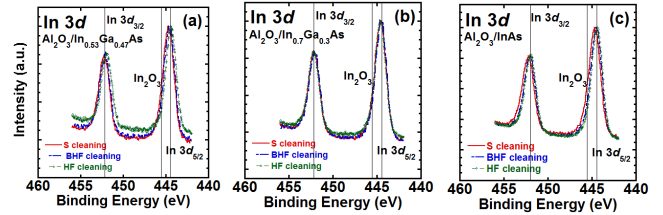


FIGURE 9. In 3d spectra in XPS analysis on Au/Al₂O₃/In_xGa_{1-x}As ((a) $x = 0.53$, (b) $x = 0.7$, and (c) $x = 1$) with S cleaning, BHF cleaning, and HF cleaning. The In 3d spectra are composed of the spectra from In 3d_{5/2} and In₂O₃.

a more essential role in the effects of the surface treatment on D_{it} than NH₄F-based species.

In order to examine the physical origin of the In content dependence of the pre-cleaning effects, x-ray photoemission spectroscopy (XPS) was conducted at a take-off angle of 90° for the Al₂O₃/In_xGa_{1-x}As ($x = 0.53, 0.7, \text{ and } 1$) MOS interfaces. AlK α was used for this measurement. Al₂O₃ films with the thickness of around 1 nm were deposited on In_xGa_{1-x}As substrates after each cleaning by ALD, in order to analyze the interface structure. PMA was performed at 350 °C for 1 min in N₂ ambient after ALD deposition. Fig. 9, 10, and 11 show the In 3d, the Ga 2p, and the As 2p spectra, respectively, of Al₂O₃/In_xGa_{1-x}As MOS interfaces with (a) $x = 0.53$, (b) $x = 0.7$, and (c) $x = 1$ under the different cleaning treatments. Here, the In 3d core level can be regarded as composed of the three components, In 3d_{3/2} (451.7eV), In 3d_{5/2} (444.3eV), and In₂O₃ (445.3eV). Also, the Ga 2p core level can be regarded as composed of the two peaks, Ga (1118.0eV) and Ga₂O₃ (1119.0eV). As shown in Fig. 9 and Fig. 10, the In 3d and the Ga 2p peaks have asymmetric shapes as a function of the binding energy, indicating the existence of In and Ga oxides. However, there is no significant difference for the In 3d and the Ga 2p spectra among the three different In contents and the three different surface treatments. These results mean that the chemical bonding conditions of In and Ga atoms at the MOS interfaces are not significantly modulated by the surface treatment, irrespective of the In or Ga content.

Fig. 11 shows the As 2p spectra for the Al₂O₃/In_xGa_{1-x}As MOS interfaces with (a) $x = 0.53$, (b) $x = 0.7$, and (c) $x = 1$. Here, the As 2p core level can be regarded as composed of the two spectra from As (1323.5eV) and As₂O₃ (1327.0eV).

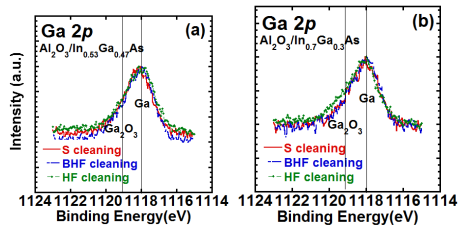


FIGURE 10. Ga 2p spectra in XPS analysis on Au/Al₂O₃/In_xGa_{1-x}As ((a) $x = 0.53$ and (b) $x = 0.7$) with S cleaning, BHF cleaning, and HF cleaning. The Ga 2p spectra are composed of the spectra from Ga and Ga₂O₃.

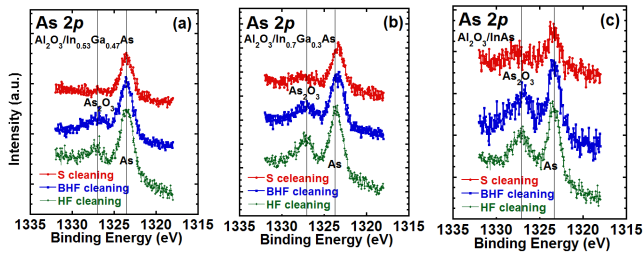


FIGURE 11. As 2p spectra in XPS analysis on Au/Al₂O₃/In_xGa_{1-x}As ((a) $x = 0.53$, (b) $x = 0.7$, and (c) $x = 1$) with S cleaning, BHF cleaning, and HF cleaning. The As 2p spectra are composed of the spectra from As₂O₃ and As.

It is found in the As 2p spectra, on the other hand, that the amount of arsenic oxides (As₂O₃) increases in BHF and HF cleaning with an increase in the In content, while the amount of arsenic oxides is much smaller in S cleaning. Judging from the correlation of the XPS data with the $C\text{-}V$ characteristics and the D_{it} results, we can interpret that this As₂O₃ could work for the passivation of Al₂O₃/In_xGa_{1-x}As MOS interface states. Also, the difference in the In_xGa_{1-x}As surface conditions, observed in the XPS results, among the different surface treatments can be explained as follows. In S cleaning, S atoms terminate the In_xGa_{1-x}As surface, and protect the surface, particularly, surface As atoms from oxidation prior and during Al₂O₃ deposition [12]. Thus, the amount of oxides at the interface is smaller. On the other hand, BHF cleaning or HF cleaning just cleans the surface and does not cap the surface with anything, resulting in easy oxidation of the surface in the air and/or during ALD. As a result, the amount of As oxides can be larger with BHF or HF cleaning than with S cleaning.

As described in the introduction, the removal of “native” oxide has been regarded as important for reduction in D_{it} at In_xGa_{1-x}As MOS interfaces. However, there have also been some recent reports on low D_{it} at oxide-rich In_xGa_{1-x}As MOS interfaces like this paper. For the HfO₂/In_{0.53}Ga_{0.47}As MOS interfaces [19], As₂O₃-rich In_{0.53}Ga_{0.47}As interfaces formed at lower HfO₂ ALD temperature of 150–200 °C, where higher amounts of As oxides are observed in the XPS spectra, exhibit lower D_{it} . Also, the HfO₂/InAs MOS capacitors [20] have been reported to show the good characteristics for InAs surfaces exposed to oxygen and

intentionally terminated with oxygen atoms before HfO₂ deposition. Here, very low D_{it} ($\sim 2.2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) has been obtained over the whole bandgap of InAs. Additionally, it has recently been found that crystalline-like oxides grown on III-V surfaces would have a great potential to improve the MOS interface [21], [22], and that stable (3×1) crystalline oxide layers on InAs can be combined with ALD HfO₂ growth at 100 °C [23]. Actually, this group also have succeeded in lowering D_{it} of HfO₂/In_{0.53}Ga_{0.47}As MOS interfaces by intentionally forming crystalline-oxide-rich surfaces before depositing HfO₂ [24]. As a result, these reports suggest that oxide-rich In_xGa_{1-x}As MOS interfaces can yield low D_{it} under a specific condition. In addition, these results imply that the physical origin of D_{it} at In_xGa_{1-x}As MOS interfaces is not unique, but multiple origins of D_{it} may exist and, thus, that several factors can affect each origin in a different way.

Based on the above discussions, we propose a physical interpretation of the relationship between pre-treatment and possible interface defects responsible for D_{it} . Fig. 12 shows a schematic view of the energy distributions of D_{it} to explain this physical model. It should be noted here that, as the In content (x) of In_xGa_{1-x}As becomes higher, the energy of the conduction band bottom is shifted toward to lower energy, while the energy of the valence band top is almost the same, independent of x .

Meanwhile, according to the theoretical calculations of the energy levels of possible defects responsible for D_{it} at In_xGa_{1-x}As MOS interface [25], As-As dimer states locate near the conduction band edge of In_{0.53}Ga_{0.47}As, while As dangling bond (DB) states locates near the valence band edge of In_{0.53}Ga_{0.47}As and InAs, as indicated in Fig. 12. The continuous energy distribution of D_{it} could be interpreted as a spread of discrete defect levels due to the variations in bond lengths and bond angles around the defects [26]. As a result, we can assume the observed continuous U-shaped energy distribution of D_{it} as superposition of multiple peak distributions with a spread, originating in specific discrete defect levels. The downward-convex D_{it} distribution near the conduction band edge has been confirmed by many previous works including [27].

Under the above interpretation of the energy distribution of D_{it} , the interface states near the conduction band of In_{0.53}Ga_{0.47}As can be attributed to As-As defect bonds, while those in the midgap and valence band side can be ascribed to As dangling bonds. Here, when the In content (x) increases, the In_xGa_{1-x}As conduction band edge moves to the lower energy, as indicated in Fig. 12. Then, in the present assignment of the physical origins of D_{it} , the dominant origin of D_{it} can change from As-As dimer bonds to As dangling bonds.

This interpretation can explain the experimental results, obtained in this study, appropriately as follows. The effectiveness of BHF/HF cleaning on D_{it} reduction with higher In content indicates that BHF/HF cleaning is contributing to reduction in the density of As dangling bonds, which can be

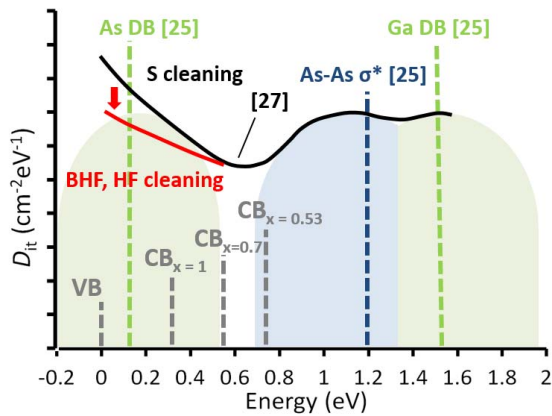


FIGURE 12. The model of the energy distribution of D_{it} around $\text{In}_x\text{Ga}_{1-x}\text{As}$ energy level with possible origin of D_{it} such as As dangling bond or Ga dangling bond.

a dominant origin of D_{it} with higher In content. As a result, the dependence of the effective surface treatment on the In content can be explained by the change in the dominant physical origin of D_{it} . Also, the existence of higher amounts of As_2O_3 observed in BHF/HF cleaning suggests that this As_2O_3 can passivate As dangling bond states through oxygen termination of dangling bonds. In addition, higher D_{it} observed in higher In content even with BHF/HF cleaning is attributable to the increase in D_{it} due to As dangling bond states with the energy closer to the valence band edge, shown in Fig. 12.

IV. CONCLUSION

We studied the electrical and physical properties of the high-k (Al_2O_3 , HfO_2)/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x = 0.53, 0.7, \text{ and } 1$) MOS interfaces with $(\text{NH}_4)_2\text{S}_y$, BHF, and HF treatments. It was found from the C - V characteristics and the D_{it} result that, as the In content (x) in $\text{In}_x\text{Ga}_{1-x}\text{As}$ becomes higher, BHF/HF cleaning is more effective in reducing D_{it} at the $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interfaces than S cleaning. There was no essential difference in the MOS interface properties between BHF and HF cleaning, revealing that HF-based species play a main role in BHF cleaning. It was found from the XPS analyses that the amount of As_2O_3 becomes larger in BHF/HF cleaning with increasing the In content. This result suggests that As_2O_3 can work for the reduction in D_{it} at the $\text{In}_x\text{Ga}_{1-x}\text{As}$ surfaces. Finally, we propose a physical interpretation of D_{it} and its physical origin to explain the present experimental results. With an increase in the In content, the dominant origin of D_{it} can change from As-As dimers to As dangling bonds, which can be a reason of the change in the effective surface treatment with higher In content. Also, the lower D_{it} with BHF/HF cleaning is attributable to the effective passivation of As dangling bonds with oxygen atoms, which can be supported by the formation of As_2O_3 , observed in XPS.

ACKNOWLEDGMENT

The authors would like to thank Dr. M. Yokoyama, Dr. O. Ichikawa, Dr. H. Yamada, and Dr. T. Yamamoto in Sumitomo Chemical Corporation for their cooperation.

REFERENCES

- [1] D. A. Buchanan, "Scaling the gate dielectric: Materials, integration, and reliability," *IBM J. Res. Develop.*, vol. 43, no. 3, pp. 245–264, May 1999.
- [2] W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, "Unified mechanism for Schottky-barrier formation and III-V oxide interface states," *Phys. Rev. Lett.*, vol. 44, no. 6, pp. 420–423, Feb. 1980.
- [3] M. D. Pashley, K. W. Haberem, R. M. Feenstra, and P. D. Kirchner, "Different Fermi-level pinning behavior on n- and p-type GaAs(001)," *Phys. Rev. B, Condens. Matter*, vol. 48, no. 7, pp. 4612–4615, Aug. 1993.
- [4] J. Robertson and L. Lin, "Bonding principles of passivation mechanism at III-V-Oxide interfaces," *Appl. Phys. Lett.*, vol. 99, no. 22, pp. 1–3, Nov. 2011.
- [5] P. D. Ye, "Main determinants for III-V metal-oxide-semiconductor field-effect transistors (invited)," *J. Vac. Sci. Technol.*, vol. 26, no. 4, pp. 697–704, Jul./Aug. 2008.
- [6] H.-C. Chin, X. Liu, X. Gong, and Y.-C. Yeo, "Silane and ammonia surface passivation technology for high-mobility $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 973–979, May 2010.
- [7] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces," *J. Appl. Phys.*, vol. 108, no. 12, pp. 1–5, Dec. 2010.
- [8] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3 , HfO_2 and HfAlO as gate dielectrics," presented at the IEDM, Washington, DC, USA, 2007, pp. 637–640. [Online]. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4419020>
- [9] Y. Urabe *et al.*, "Correlation between channel mobility improvements and negative V_{th} shifts in III-V MISFETs: Dipole fluctuation as new scattering mechanism," presented at the IEDM, San Francisco, CA, USA, 2010, pp. 6.5.1–6.5.4. [Online]. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5703310>
- [10] R. Suzuki *et al.*, "Effect of sulfur treatment on $\text{HfO}_2/\text{InGaAs}$ MOS interfaces properties," presented at the SSDM, 2011, pp. 941–942. [Online]. Available: https://confit.atlas.jp/guide/event-ing/ssdm2011/E-8-3/public/pdf_archive?type=in
- [11] L. Lamagna *et al.*, "Effects of surface passivation during atomic layer deposition of Al_2O_3 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates," *Microelectron. Eng.*, vol. 88, no. 4, pp. 431–434, Apr. 2011.
- [12] M. Yokoyama, R. Suzuki, N. Taoka, M. Takenaka, and S. Takagi, "Impact of surface orientation on (100), (111)A, and (111)B InGaAs surfaces with in content of 0.53 and 0.70 and on their $\text{Al}_2\text{O}_3/\text{InGaAs}$ metal-oxide-semiconductor interface properties," *Appl. Phys. Lett.*, vol. 109, no. 18, pp. 1–4, Oct. 2016.
- [13] H. D. Trinh *et al.*, "The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition $\text{Al}_2\text{O}_3/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor capacitor," *Appl. Phys. Lett.*, vol. 97, no. 4, pp. 1–3, Jul. 2010.
- [14] D. Wheeler *et al.*, "Deposition of HfO_2 on InAs by atomic-layer deposition," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1561–1563, Jul./Sep. 2009.
- [15] K. Nishi *et al.*, "Effects of buffered HF cleaning on metal-oxide-semiconductor interface properties of $\text{Al}_2\text{O}_3/\text{InAs/GaSb}$ structures," *Appl. Phys. Exp.*, vol. 8, no. 6, pp. 1–4, Jun. 2015.
- [16] C. Yokoyama, C.-Y. Chang, M. Takenaka, and S. Takagi, "In content dependence of pre-treatment effects on $\text{Al}_2\text{O}_3/\text{In}_x\text{Ga}_{1-x}\text{As}$ MOS interface properties," presented at the EDTM, Toyama, Japan, 2017, pp. 23–25. [Online]. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7947493>
- [17] S. Kim *et al.*, "Strained $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor field-effect transistors with epitaxial based biaxial strain," *Appl. Phys. Lett.*, vol. 100, no. 19, pp. 1–3, Apr. 2012.

- [18] S. Kim *et al.*, "Self-aligned metal source/drain In_xGa_{1-x}As n-metal-oxide-semiconductor field-effect transistors using Ni-InGaAs alloy," *Appl. Phys. Exp.*, vol. 4, no. 2, pp. 1–3, Feb. 2011.
- [19] R. Suzuki *et al.*, "Impact of atomic layer deposition temperature on HfO₂/InGaAs metal-oxide-semiconductor interface properties," *J. Appl. Phys.*, vol. 112, no. 8, pp. 1–5, Oct. 2012.
- [20] C. H. Wang *et al.*, "InAs hole inversion and bandgap interface state density of $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at HfO₂/InAs interfaces," *Appl. Phys. Lett.*, vol. 103, no. 14, pp. 1–4, Oct. 2013.
- [21] M. P. J. Punkkinen *et al.*, "Oxidized In-containing III-V (110) surfaces: Formation of crystalline oxide films and semiconductor-oxide interfaces," *Phys. Rev. B, Condens. Matter*, vol. 83, no. 19, pp. 1–6, May 2011.
- [22] M. Tuominen *et al.*, "Oxidized crystalline (3 × 1)-O surface phases of InAs and InSb studied by high-resolution photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 106, no. 1, pp. 1–4, Jan. 2015.
- [23] X. Qin, W.-E. Wang, M. S. Rodder, and R. M. Wallace, "In situ surface and interface study of crystalline (3×1)-O on InAs," *Appl. Phys. Lett.*, vol. 109, no. 4, pp. 1–4, Jul. 2016.
- [24] X. Qin, W.-E. Wang, R. Droopad, M. S. Rodder, and R. M. Wallace, "A crystalline oxide passivation on In_{0.53}Ga_{0.47}As (100)," *J. Appl. Phys.*, vol. 121, no. 12, pp. 1–8, Mar. 2017.
- [25] J. Robertson, Y. Guo, and L. Lin, "Defect state passivation at III-V oxide interfaces for complementary metal-oxide-semiconductor devices," *J. Appl. Phys.*, vol. 117, no. 11, pp. 1–10, Mar. 2015.
- [26] T. Sakurai and T. Sugano, "Theory of continuously distributed trap states at Si-SiO₂ interfaces," *J. Appl. Phys.*, vol. 53, no. 4, pp. 2889–2896, Apr. 1981.
- [27] N. Taoka *et al.*, "Influence of interface traps inside the conduction band on the capacitance–voltage characteristics of InGaAs metal-oxide-semiconductor capacitors," *Appl. Phys. Exp.*, vol. 9, no. 11, pp. 1–4, Nov. 2016.



CHI-YU CHANG (M'17) received the B.S. degree in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2009, and the M.S. and Ph.D. degrees in electrical engineering and information systems from the University of Tokyo, Tokyo, Japan, in 2013 and 2016, respectively. His research interests include high-k/In_{0.53}Ga_{0.47}As MOS interface and MOSFETs.



MITSURU TAKENAKA (M'02) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1998, 2000, and 2003, respectively, where he is currently an Associate Professor with the Department of Electrical Engineering and Information Systems.



CHIAKI YOKOYAMA received the B.S. degree in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2017, where she is currently pursuing the M.S. degree with the Department of Electrical Engineering and Information Systems. Her current research interest includes high-k/In_xGa_{1-x}As MOS interfaces.



SHINICHI TAKAGI (M'93) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984, and 1987, respectively, where he is currently a Professor with the Department of Electrical Engineering and Information Systems, School of Engineering.