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A Novel Reconfigurable Sub-0.25-V Digital Logic Family Using the Electron-Hole Bilayer TFET

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ABSTRACT We propose and validate a novel design methodology for logic circuits that exploits the conduction mechanism and the presence of two independently biased gates ("n-gate" and "p-gate") of the electron-hole bilayer tunnel field-effect transistor (EHBTFET). If the device is designed to conduct only under certain conditions, e.g., when $V_{\text{n-gate}} = V_{\text{DD}}$ and $V_{\text{p-gate}} = 0$, it then shows an "XOR-like" behavior that allows the implementation of certain logic gates with a smaller number of transistors compared to conventional CMOS static logic. This simplifies the design and possibly results in faster operation due to lower node capacitances. We demonstrate the feasibility of the proposed EHBTFET logic for low supply voltage operation using mixed device/circuit simulations including quantum corrections.

INDEX TERMS Band-to-band tunneling, tunnel field-effect transistor (TFET), 2D-2D tunneling, quantum mechanical simulation, logic circuits.

I. INTRODUCTION

Tunnel FETs (TFET) has emerged as one of the most prominent steep slope switch [1], [2]. However most practical implementations suffer from very low ON currents [3]. The electron-hole bilayer TFET (EHBTFET) addressed this issue by utilizing the so-called *line tunneling* [4] for which the band-to-band tunneling (BTBT) takes place over the entire region covered by the gate. The EHBTFET [5] consists of a semiconductor layer sandwiched between two asymmetrically placed gates, n- and p-gate to induce 2D electron and hole gases (2DEG and 2DHG), respectively (see Fig. 1 (a, b and d)). Initial circuit performance assessment was made in [5] for Ge EHBTFET where it was benchmarked against a virtual double gate Ge MOSFET using inverters. Modeling of the device including quantum mechanical treatment of subband alignment and subband-to-subband tunneling was presented in [6]. Further on, the non-idealities unforeseen by the semi-classical tools and their possible solutions [7], [8] were identified. These studies have shown that steep switching characteristics are retained provided suitable counter-measures are put in place to suppress lateral leakage.

Another important feature of the EHBTFET is the independent biasing of the n- and p-gates. Typically, a positive (negative) bias needs to be applied to n-gate (p-gate) to induce the electron-hole subband alignment in the overlap region, although different configurations are certainly possible with appropriate choice of the gate metal workfunctions. Another property of the EHBTFET, that is shared by many other TFET structures, is the ambipolarity [9], [10], i.e., the same device can be used as a pull-up (p-type) or a pull-down (n-type) device. Therefore, it could be possible to achieve a CMOS-like functionality by using a single device. Moreover, since the EHBTFET is a symmetric device (i.e., both electrons and holes contribute to conduction mechanism), n-type and p-type static behavior is almost symmetric as well if gate workfunctions are chosen appropriately.

No reports about the fabrication of the EHBTFET have been presented so far. However, possible fabrications strategies have been devised such as the fin EHBTFET [11]. Also, recently developed vertical epitaxial growth techniques such as template-assisted selective epitaxy (TASE) [12],

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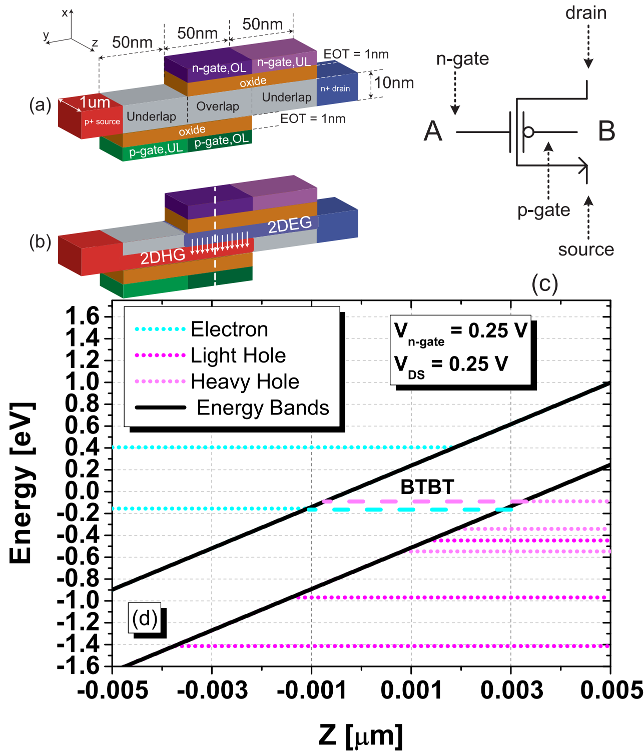


FIGURE 1. (a) Sketch of the hetero-gate InGaAs EHBTFET (b) Working principle of the EHBTFET. The white arrows indicate the direction of BTBT. (c) EHBTFET circuit symbol for the EHBTFET denoting the corresponding electrodes. (d) The band profile of the EHBTFET along the vertical direction in the overlap region (see the dashed line on Fig. 1(b)) for the ON state. The calculated subband energies for the electron and hole states are denoted as dotted lines.

which allows for high quality III-V devices integrated on a Si substrate can be utilized.

In this paper, we propose a novel logic family exploiting distinguishing features of the EHBTFET, namely the independent biasing and the steep slope switching. The EHBTFET logic makes use of the independent biasing property to implement complex logic functions with a reduced number of transistors. This is similar to the proposal in [13] that however assumes TFET architectures different than the EHBTFET. We demonstrate the operation of various logic circuits using quantum-corrected mixed-mode TCAD simulations.

II. SIMULATION APPROACH

We use Sentaurus Device [14] to perform the static and transient simulations. Due to very strong quantization and to BTBT taking place between two quantized states (z tunneling), a proper treatment of the quantization effects is necessary. To this end, we make use of a recently proposed method [15] to mimic subband quantization in the semiconductor by using the Physical Model Interface (PMI) of Sentaurus Device [14]. The model modifies the conduction and valence band edges near the semiconductor/oxide interface thus shifting the onset of tunneling in a consistent way with the predictions of the quantum mechanical (QM) simulations [6]. This enables the TCAD tool to predict both the vertical current (wanted) as well as the lateral one (leakage, unwanted) BTBT current which stems from the fact that quantization is less severe in the underlap region [16]. Using such an approach allows us to include quantum effects properly in the mixed-mode circuit simulation environment. However, it should be noted that the charge densities are still calculated semiclassically.

III. DEVICE WORKING PRINCIPLE & CIRCUIT SIMULATIONS

The device structure, the main dimensions and circuit schematic of the $In_{0.53}Ga_{0.47}As$ EHBTFET is given in Fig. 1. We take the electron effective mass, the heavy hole effective mass and the bandgap as $m_e = 0.042$ m_0, $m_{hh} = 0.457$ m_0 and $E_G = 0.751$ eV respectively. We utilize the heavy hole mass for the quantization model to determine the subband energy. On the other hand, the light hole mass ($m_{lh} = 0.052$ m_0) is used for BTBT model since the conduction and heavy hole subbands are connected in the imaginary dispersion with a hole effective mass much closer to the light hole one [16]. To prevent the lateral leakage that deteriorates the SS, we utilize the hetero-gate configuration [8] with $\Phi_{n-gate,OL} = 3.225$ eV and $\Phi_{n-gate,UL} = 3.9$ eV whereas we use $\Phi_{p-gate,OL} = 6.225$ eV and $\Phi_{p-gate,UL} = 5.75$ eV. The overlap (OL) workfunction values are chosen to align the subband energies in such a way that conduction occurs at $V_{n-gate} = V_{DD}$ and $V_{p-gate} = 0$. Similarly, the underlap (UL) workfunctions are optimized such that the induced energy barrier only delays the diagonal leakage path without harming the ON current of the device. Unless otherwise stated, we set $V_{DD} = 0.25$ V.

The transfer characteristics for the n- and p-gates are given in Fig. 2 (a). Comparison against the results obtained by the 1-D quantum-mechanical model based on the effective mass approximation [6] indicates an excellent match in the current levels and good match in the tunneling onset voltages (max. difference $\sim$ 20 mV). For the n-gate sweep, p-gate is kept at 0 V; similarly for the p-gate sweep, n-gate is kept at V_{DD}. The device exhibits few mV/dec switching slope for over eight decades of current for both n- and p-gate sweeps. Note that the QM results predict an abrupt switching once subband get aligned. This is due to two main reasons: i) band-tail states are not included [17], ii) the simulation is 1D, whereas 2D simulations show a finite point SS [7] that can be however be reduced using the hetero-gate structure [8].

By comparing the n- and p- sweep, we see that ON current, switching slope and the tunneling onset voltages are almost symmetric, signaling that n-type (pull-down) and p-type (pull-up) performances are comparable and the same device can be used for both purposes. The output characteristics for pull-up (source node charges from 0 to 0.25 V) and pull-down (drain node discharges from 0.25 V to 0) cases given in Fig. 2 (b) indicate a good overall match with the QM simulations as well as negligible superlinearity [18]. The

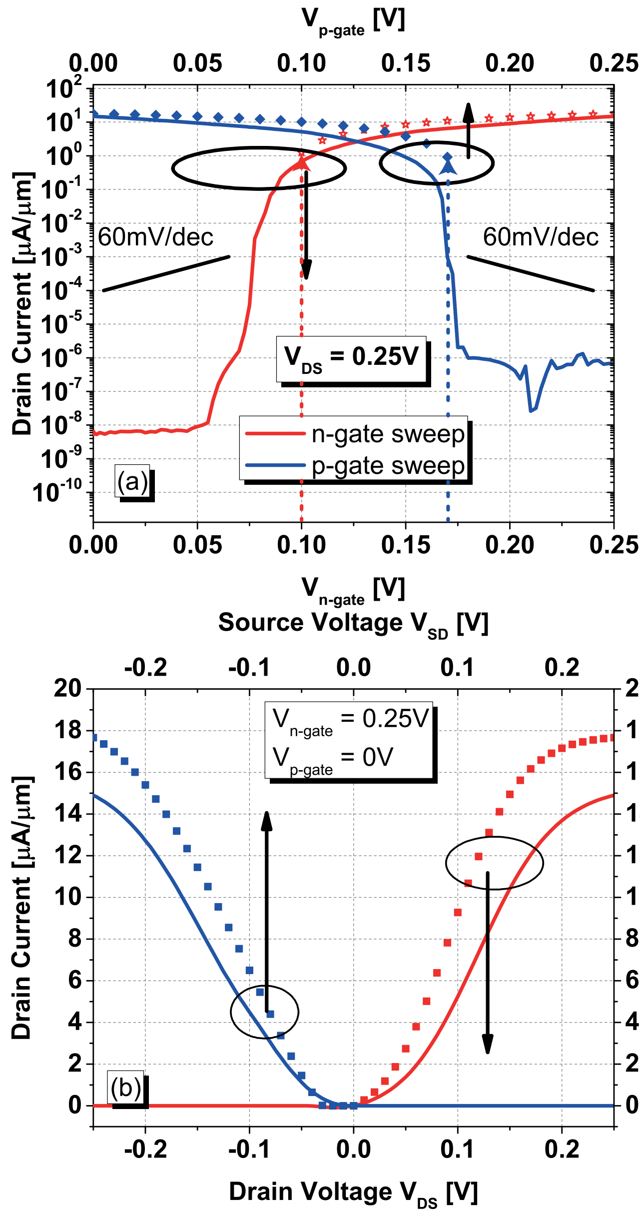


FIGURE 2. (a) Transfer characteristics of the InGaAs EHBTFET for (red) n-gate sweep with $V_{p-gate} = 0$ V and (blue) p-gate sweep with $V_{n-gate} = 0.25$ V. The vertical dashed lines for QM results indicate the quasi-abrupt switching since 1-D QM model cannot predict lateral leakage [7] (b) Pull-up (blue line and symbols) and pull-down (red line and symbols) output characteristics for the EHBTFET. For both plots, symbols indicate the results obtained by the quantum mechanical model described in [6] while lines are the results of TCAD simulations including the quantum corrections proposed in [15].

output resistance for the pull-up behavior exhibits slightly lower output resistance since the valence band profile in the region controlled by the p-gate is not fully pinned by the inversion charge. These said, it should be noted that the EHBTFET suffers from the partially unidirectional conduction that is shared by all TFETs, as evidenced in Fig. 2 (b). This, in certain cases, may result in excess charging of the circuit nodes [19] which cannot be discharged.

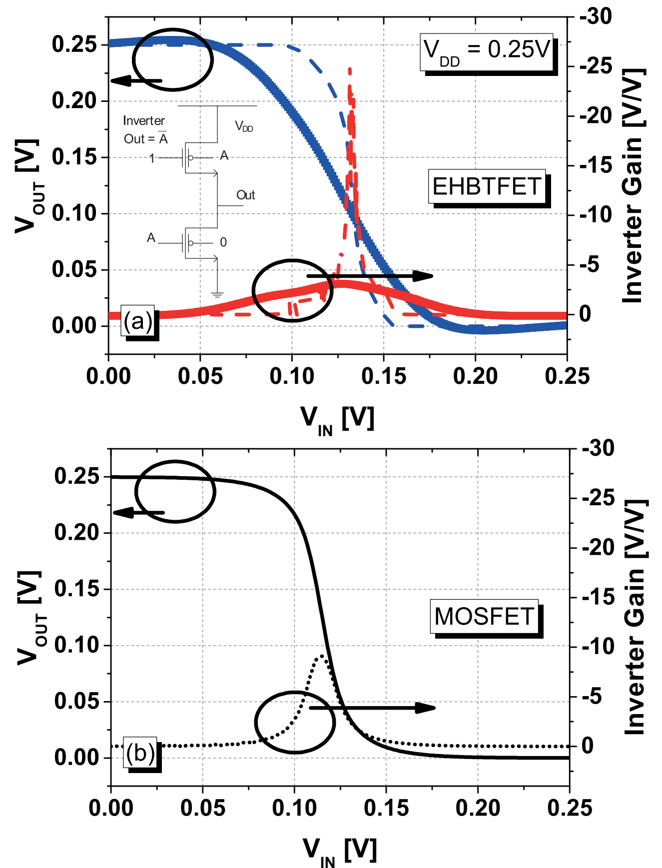
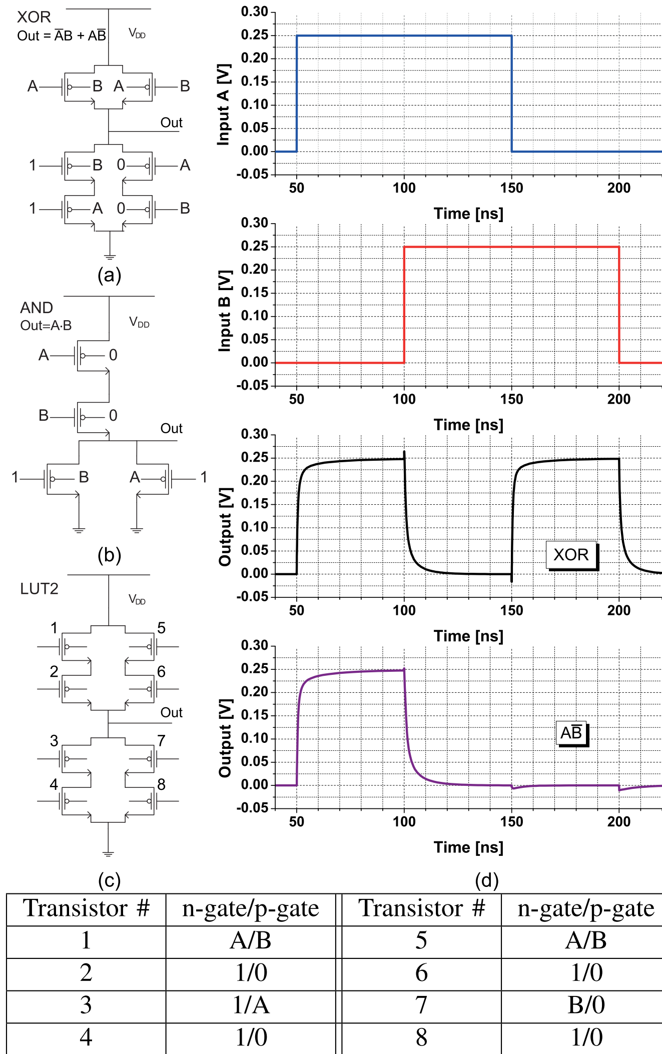


FIGURE 3. (a) Voltage transfer characteristic (VTC, blue line and symbols) and inverter gains (red line and symbols) of the EHBTFET inverter for a supply voltage $V_{DD} = 0.25$ V using the workfunctions (WF) given in the manuscript (symbols) or using optimized WFs for pull-up and pull-down transistors (line). The WF values for this latter case are $\Phi_{n-gate,OL} = 3.3$ eV, $\Phi_{p-gate,OL} = 6.3$ eV (pull down) and $\Phi_{n-gate,OL} = 3.15$ eV, $\Phi_{p-gate,OL} = 6.15$ eV (pull up). The circuit schematic for the inverter using the EHBTFET is given in the inset. Plot (b): same as in Fig. 3(a), but for a MOSFET inverter. NMOS (PMOS) device width and length are 1 μm (1.5 μm) and 30 nm (30 nm) respectively. For the p- and n-TFETs the width is 1 μm.

Fig. 3 (a) depicts the voltage transfer characteristic (VTC) of an inverter made up of the EHBTFET described above as both pull-up and pull-down devices, showing sufficient inverter gain and noise margins. We have verified in Fig. 3(a) that the inverter gain and the noise margins can be vastly improved by utilizing two different EHBTFET devices optimized for pull-up and pull-down behavior respectively. Fig. 3 (b) presents the VTC characteristics for an inverter using a 28nm CMOS technology. It indicates similar inverter gains when compared to the EHBTFET with the same pull-up/pull-down devices, whereas dramatically lower than the EHBTFET inverter using optimized workfunctions (dashed lines in Fig. 3(a)). For the remainder of the paper, we will present results for the case with same device used for both pull-up and pull-down.

The main idea behind the EHBTFET logic stems from the observation that the EHBTFET conducts only when $V_{n-gate} = V_{DD}$ and $V_{p-gate} = 0$. If we denote the input



Transistor #	n-gate/p-gate	Transistor #	n-gate/p-gate
1	A/B	5	A/B
2	1/0	6	1/0
3	1/A	7	B/0
4	1/0	8	1/0

FIGURE 4. Circuit schematic for (a) XOR (b) AND (c) LUT2 gates. (d) Transient simulation input and output waveforms of (black) XOR (purple) LUT2 programmed as $A\bar{B}$ using $V_{DD} = 0.25$ V. The corresponding input signals for LUT2 implementing $A\bar{B}$ are indicated in the table. The circuits have 30fF of capacitive loads at their output nodes. The results indicate extremely fast switching (~ 10 ps) even at low supply voltage.

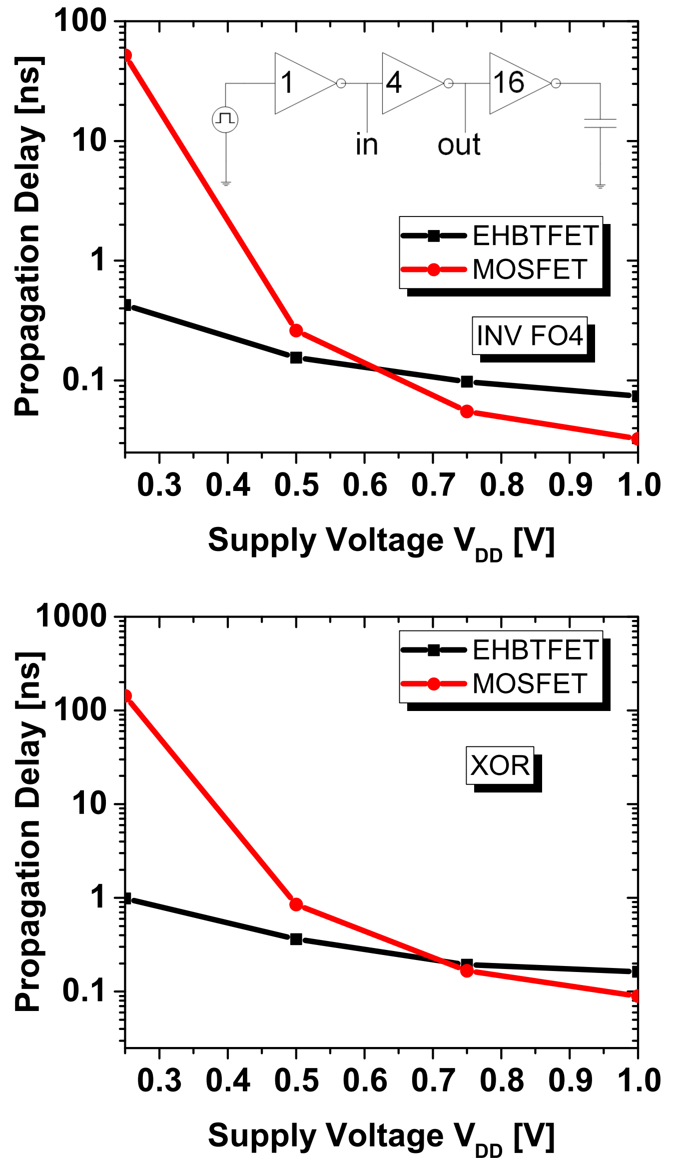


FIGURE 5. Worst case delays as a function of the supply voltage V_{DD} for (Top) fan-out-4 Inverter (Bottom) XOR circuits. The black (red) lines indicate EHBTFET logic (CMOS, 28nm FD-SOI) implementations. Both circuits have 30 fF of load capacitance.

signals at n-gate and p-gate as A and B, the condition for conduction is fulfilled only when $F = A\bar{B}$. This allows us to implement $A\bar{B}$ terms using one transistor showing n-type (conducts when the n-gate input is 1) and p-type (conducts when the p-gate input is 0) behavior. Fig. 4 (a & b) presents two-input XOR and AND gates implemented with the EHBTFET logic. This flexibility allows for a sizable reduction in the number of transistors for logic gates. For instance, the XOR gate requires 6 transistors in EHBTFET logic compared to 12 transistors in conventional static CMOS logic (including the inverters required to obtain the inverted input signals) and the AND gate requires 4 transistors vs 6 transistors. The XOR circuit operation is verified through transient simulations whose waveforms are given in Fig. 4 (d).

Fig. 4 (c) shows the EHBTFET implementation of the LUT2, a building block for most FPGAs [20]. It allows for implementing any 2-input logic function by multiplexing the inputs A and B as well as '1' and '0' bits to the gates of the 8 transistors. The same number of transistors is needed also for conventional CMOS, but inverters are needed if $\overline{A}$ and $\overline{B}$ are required. In the EHBTFET case, instead, we can exploit the n- and p-gates to eliminate the inverters. As an example we show the implementation of the function $A\overline{B}$ using the LUT2 circuit with corresponding input signals (see table in Fig. 4) and resulting transient simulations (Fig. 4(d)).

Fig. 5 compares the simulated worst case delays (τ) for varying supply voltages for the EHBTFET logic and 28nm

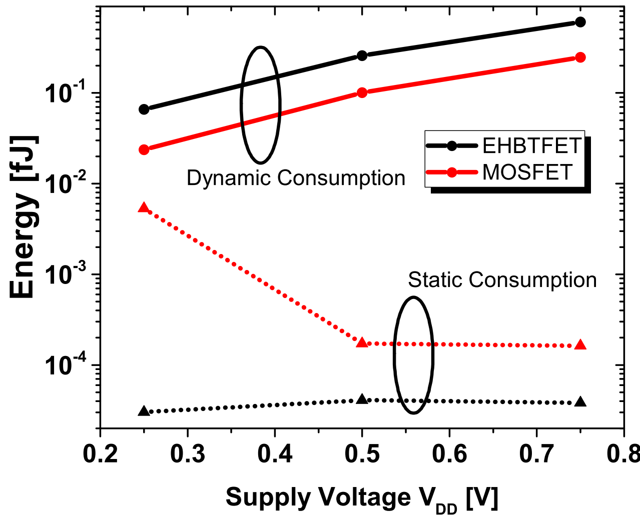


FIGURE 6. **Dynamic (solid lines) and static (dotted lines) energy consumption per switching event. The black (red) lines indicate EHBTFET logic (CMOS, 28nm FD-SOI) implementations. Both circuits have 30 fF of load capacitance.**

fully depleted silicon on insulator (FD-SOI) CMOS process. We note that we did not utilize the standard cell libraries, but rather designed standard CMOS implementations of the inverter and XOR gates. For fair comparison, we fixed the width of each CMOS transistor at 1 μm and varied the gate length for adjusting the driving strength of the transistors for the optimum and balanced rise and fall time behavior. We compare the worst case timings for fan-out-4 [21] inverter delays in Fig. 5(Left). As commonly done [22], [23], we simulate an inverter chain where the driving strength quadruples between each stage (see the inset in Fig. 5(Left)) and we report the worst case delay of the middle stage. It is seen that for both circuits, the EHBTFET outperforms the CMOS implementation for low supply voltages ($V_{DD} < 0.5$ V), where it is able to deliver higher drive current than the CMOS counterpart. Note that the supply voltage region where the EHBTFET implementation outperforms the CMOS counterpart is increased for the case of XOR, due to the reduced transistor count. As the supply voltage increases, CMOS performance improves dramatically thanks to the increasing ON current of the CMOS transistors.

Finally, in Fig. 6 we compare the energy per switching (EPS) metric of the two technologies. Specifically, we extract the current flowing in the pull-up transistor of the middle stage of the FO4 inverter chain and then assume an activity factor $\alpha = 0.01$ [2]. The total energy is calculated as the sum of static and dynamic energy consumption, using the following formula:

$$E_{TOT} = \underbrace{\alpha \int_T I_D(t)\, V_{DD} dt}_{\text{dynamic}} + \underbrace{\int_T I_{stat} V_{DD} dt}_{\text{static}} \quad (1)$$

where we use $T = 10\tau$ for each case, τ being the propagation delay at the given V_{DD} shown in Fig. 5. I_{stat} is taken as the average of the output-high and output-low static leakage current values. It is seen that the dynamic energy consumption for the EHBTFET is higher than its CMOS counterpart, due to larger gate capacitance of the EHBTFET. However, we see that EHBTFET is able to provide significant improvements for the static power consumption, mainly due to shorter switching times. In the CMOS case, the longer switching time at low V_{DD} drastically increases the static energy even if the OFF current slightly decreases as V_{DD} is scaled. In the EHBTFET, instead, the lower OFF current as V_{DD} is scaled results in slightly decreasing static energy consumption.

IV. CONCLUSION

We have proposed and validated a new low supply voltage circuit design topology using the EHBTFET architecture by fully exploiting the inherent symmetry and high trans-conductance resulting from the steep switching slope. Through mixed-mode simulations with quantum mechanical corrections, we have shown that the EHBTFET logic is able to implement any complex logic function using a same size, identical pull-up and pull-down transistors and with a reduced number of transistors compared to the conventional static CMOS logic. To assess the effective area saving of this logic compared to conventional CMOS, a suitable fabrication process with associated layout rules should be devised. In addition, an extensive analysis of the scalability of EHBTEFT is needed, to asses if one can significantly reduce the gate length compared to what is used here. However, beside that, our results indicate that the EHBTFET logic is a promising alternative to the current MOSFET technology especially for low supply voltage and low switching activity scenarios. Co-integration with CMOS can be foreseen, although suitable level shifters may be needed to interface the low-V_{DD} EHBTFET logic with the higher V_{DD} CMOS sections of the system.

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