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Experimental and Numerical Evaluation of R_{ON} Degradation in GaN HEMTs During Pulse-Mode Operation

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ABSTRACT The on-resistance (R_{ON}) degradation in normally-OFF GaN high electron mobility transistors has been evaluated both experimentally and by means of numerical simulations by analyzing its drift during device pulse-mode operation. Experimental data showed that the device R_{ON} measured during the on-time interval of the switching period increased with time resulting in a thermally activated process with an activation energy $E_A = 0.83$ eV. For the first time, numerical simulations have been carried out in order to evaluate the device R_{ON} drift during pulse-mode operation and to understand the physical phenomena involved. A good qualitative agreement between experimental and simulated data has been obtained when considering in the simulated device simply a hole trap located at 0.83 eV from the GaN valence-band, an energy level which has been linked in previous works to carbon-doping within the GaN buffer.

INDEX TERMS Wide band gap semiconductors, numerical simulation, carbon doping, trapping phenomena.

I. INTRODUCTION

GaN-Based high electron mobility transistors (HEMTs) are of great interest for the achievement of power devices with both low on-resistance (R_{ON}) and low-switching losses for high efficiency switching applications [1], [2].

One of today most critical issues of GaN HEMTs is their R_{ON} increase when exposed to high drain biases in OFF-state conditions [3]. While said increase has been associated to the presence of carbon-doping within the GaN buffer layers [4], [5], a clear understanding of the physical phenomena involved, i.e., electrons trapping [6] or holes emission [7], is still missing in the literature. Indeed, a clear demonstration by numerical simulation of the trapping/detrapping mechanism and the monitoring of R_{ON} drift during DUT pulse-mode operation have not yet been published. Note that this last point is also crucial in order to understand the effect of trapping phenomena occurring in GaN HEMTs when operated into a scenario which is similar to their use in power conversion circuits.

Aim of this paper is to present for the first time a clear correlation between the experimental R_{ON} increase experienced by normally-OFF GaN HEMTs during pulse-mode operation and numerical simulations which takes into account only the presence of a carbon-related acceptor-like hole-trap within the device GaN buffer layer [7]. As it will be shown in the following, R_{ON} degradation can be explained by the build-up of a negative charge within the buffer layer due to a hole-emission process which leads to negatively ionized acceptor-like traps.

II. EXPERIMENTAL RESULTS

The cross-section of the normally-OFF GaN HEMTs tested in this paper is reported in figure 1. Normally-OFF operation in said devices is achieved by a full recess of the AlGaN barrier layer and the formation of a metal-dielectric-semiconductor stack in the device gate region. Further details on the fabrication process are reported in [8]. Concerning the device buffer-layers, a 4.7μm thick GaN layer is first grown

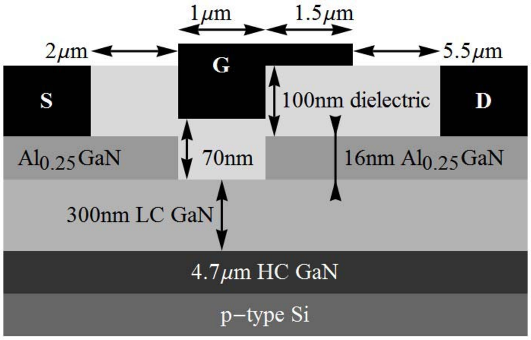

FIGURE 1. Cross section of the normally-OFF GaN HEMT structure used for the experimental evaluation of R_{ON} degradation during pulse-mode operation.

with a nominal $3x10^{18}cm^{-3}$ high-carbon concentration (HC) followed by a 300nm thick GaN layer with a nominal $3x10^{16}cm^{-3}$ low-carbon concentration (LC). The low carbon-concentration close to the AlGaN/GaN interface is adopted in order to prevent excessive depletion of the 2DEG within the structure.

Devices R_{ON} was evaluated by measuring its value while the devices were operated in pulse-mode condition with a 1kHz switching frequency by means of a pulsed "on-the-fly" (OTF) characterization [9].

The technique used in this work is similar to the on-the-fly R_{ON} measurement described in [3] with the exception that shorter on- and off-time have been used. Particularly, the devices were continuously switched with a period T_S = 1ms, which is roughly three order of magnitude lower than the 1.05s period used in [3], between off-state (i.e., V_{DSoff} = 100V, V_{GSoff} = -3V) and on-state (i.e., V_{DSon} = 1V, V_{GSon} = 2.5V) with a 1% duty-cycle, resulting in a 10μs T_{ON} time interval. Due to hardware limitations the recording of the R_{ON} values started after approximately 100ms from the beginning of the pulse-mode operation. Further details on the drain- and gate- voltage waveform applied as well as on the experimental setup adopted are reported in [10]. Devices R_{ON} evolution was thus evaluated at five different temperatures, from 40°C to 60°C with a 5°C step. As can be seen in Fig. 1, devices R_{ON} increased by approximately a 30% within the first 30s of pulse-mode operation at 40°C before flattening out. Increasing the temperature yielded a speed-up in the observed R_{ON} transients, suggesting that the physical mechanism leading to the observed R_{ON} degradation might be related to a trap emission-process. R_{ON} transients time constants were then evaluated by evaluating the peaks of the associated $dR_{ON}/d(\log(t))$ signals [11], see figure 2. Based on the extracted time constant the Arrhenius plot reported in the inset of figure 2 was obtained, which yielded a 0.83eV activation energy with an associated capture cross-section of approximately $4x10^{-15}cm^{-2}$.

III. NUMERICAL SIMULATIONS

At this point numerical simulations were carried out by means of the commercial simulator DESSIS-ISE with the aim of investigating the possible mechanism leading to the observed R_{ON} degradation during the device pulse-mode operation. In order to reduce the total simulation time and solve some convergence issues, two simplifications were adopted.

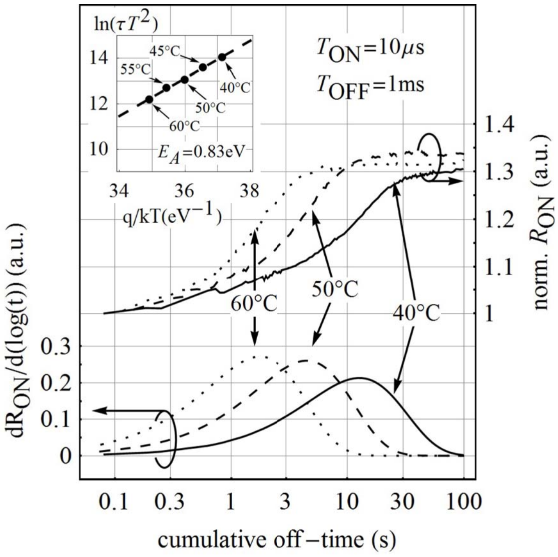

FIGURE 2. Experimental R_{ON} transient and their corresponding $dR_{ON}/d(\log(t))$ signals obtained by continuously switching the DUT between off-state and on-state conditions with a 1kHz switching frequency. The recorded R_{ON} transient results to be thermally activated with a 0.83eV activation energy as can be inferred from the Arrhenius plot reported in the inset.

The first one concerned the device structure used for simulation which is depicted in figure 3 and that is described in the following. The gate-source and gate-drain access region were modeled by removing the AlGaN layers and by inserting within the first 50nm from the dielectric/GaN interface a constant n-type doping level in order to emulate the missing 2DEG at the AlGaN/GaN interface of the real device. Doping levels were adjusted in order to obtain a $7x10^{12}cm^{-2}$ sheet charge concentration, corresponding to the experimental data obtained on the tested structure. Said doping was not inserted below the device gate region. Note that in this way the "real" and "simplified" structures are the same at least for what concerns the gate region.

The second simplification was instead introduced in order to reduce the amount of switching transients to be simulated which in the experimental setup corresponds to approximately 100 thousand of on to off and off to on transitions for a 100s cumulative off-time. Particularly, the pulse-mode operation was simulated by adopting a T_S of 100ms while T_{ON} was maintained at 10μs. Even with this simplification on the waveform timing more than thousand on to off and off to on transitions were simulated in order to reach the experimentally used 100s cumulative off-time.

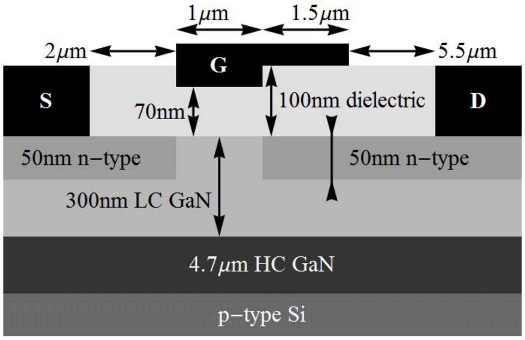

FIGURE 3. Cross section of the simplified device structure used for numerical simulation of the R_{ON} degradation during pulse-mode operation. AlGaN barrier is removed and the presence of the 2DEG in the gate-source and gate-drain access region is emulated by inserting a 50nm n-type doped layer corresponding to a $7x10^{12}cm^{-2}$ sheet charge concentration.

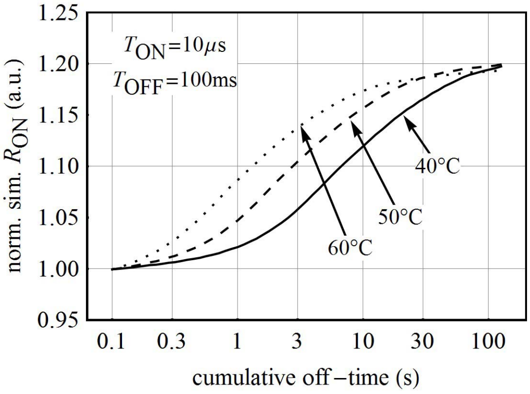

FIGURE 4. Simulated R_{ON} transients obtained by continuously switching between off-state and on-state conditions the simplified device structure used for the numerical simulation analysis. A good qualitative agreement is obtained with experimental data.

A final crucial step in the setup of the simulated structure was the selection of the traps scenario to be included within the semiconductor layers. As shown in [7], trapping phenomena in Carbon-doped GaN layers can be reproduced by adopting an acceptor-like hole-trap level whose concentration is however almost two order of magnitude lower than the nominal Carbon doping level of the GaN layers. Following the proposed scenario in [7] we inserted inside the LC and HC GaN layers of the simulated structure an acceptor-like hole-trap with a 0.6% concentration with respect to the nominal values, i.e., $1.8x10^{14}cm^{-3}$ and $1.8x10^{16}cm^{-3}$ for the LC and HC layers, respectively. Although the 0.6% ratio between the trap and carbon doping concentrations might not be strictly correct, other authors have also observed ratios in the order of few percent between the hole-trap and the nominal carbon doping concentrations [12], [13]. Our choice of the 0.6% ratio based on the results presented in [7] might thus be a little bit optimistic with respect to the experimental data, thus leading to a possibly lower R_{ON} degradation. Finally, the trap energy and capture cross-section adopted in the simulation were obtained by the experimental Arrhenius plot depicted in figure 2. In particular, the hole-trap was located at 0.83eV from the GaN valence-band while its associated capture cross-section was set to $4x10^{-15}cm^{-2}$ as experimentally obtained.

As can be seen in figure 4, the simulated "on-the-fly" R_{ON} measurements nicely reproduce the experimental results obtained both in terms of the transient nature of its increase as well as in terms of its temperature dependence. These results strongly suggest that the R_{ON} degradation observed is caused by Carbon-related acceptor-like hole-traps.

The physical mechanism leading to the observed degradation can be explained as follows. When the device experiences the first off-state interval, the hole-emission process within the GaN buffer starts to take place. This process temporarily stops during the first on-state interval. In this phase, i.e., the first on-state interval, holes could potentially be recaptured by the traps however this process is unlikely to happen since there is not a hole-source providing them. This statement is in agreement also with previous works. Particularly, Uren *et al.* [14] predicted that in the absence of any significant source of holes, the charged buffer will never go back to its equilibrium condition, thus leaving unaltered the negative charge, which in our case is caused by the ionized acceptor traps whom experienced hole emission, during the on-state phase. When the device will then be switched-off again, the hole-emission process will restart from the point where it stopped, i.e., the end of the first off-state time interval. As time passes by, since only hole-emission takes place during the off-state time interval and no hole-capture occurs during the on-state ones, the amount of ionized acceptor will increase until reaching an equilibrium condition which will leave the Carbon-doped buffer negatively charged leading to the experimentally and numerically observed R_{ON} increase. Although not specifically linked to the presence of GaN carbon-doped layers, the lack of a hole-source was also considered as the cause for the onset of device R_{ON} degradation in GIT devices presented in [15]. Similar to our work, in [15] the R_{ON} degradation has been linked to an acceptor hole-trap which, by experiencing a hole-emission process when large drain voltages are applied, leads to the onset of a negatively charged region in the GaN buffer resulting in a significant increase of the device R_{ON}. The solution proposed in [15] in order to overcome said R_{ON} increase was given by the introduction of an embedded drain contact on a p-type GaN region. Said modified structure, named HD-GIT in [15], allows a hole-injection process from the drain terminal which counteracts the hole-emission one from the buffer acceptor traps thus contributing in lowering the negative charge build-up in the GaN buffer. As a consequence, thanks to the hole-injection process, the HD-GIT devices experienced a lower R_{ON} degradation when exposed to high drain voltages.

IV. COMMENTS ON THE SIMPLIFIED STRUCTURE

Concerning the adoption of n-doped GaN layers instead of the AlGaN/GaN we would like to stress that this simplification is not strictly correct if the R_{ON} drift phenomena has to be reproduced in a quantitative way.

Nevertheless, our aim was to stress that, at least in a qualitative way, the R_{ON} degradation even during pulse-mode operation can simply be associated to the solely carbon-related hole-trap, which is located in the buffer layer, and to support this statement by means of numerical simulations.

When we thus look at reproducing the phenomena in a qualitative way a thin n-doped GaN layer forming a thin 3DEG layer has a similar behavior of the 2DEG forming at the AlGaN/GaN interface. When the 3DEG is depleted the depleted donors form a thin positively charged depletion region which electrostatically resemble the positive piezoelectric charge at the AlGaN/GaN interface. On the other hand, when electrons are present, in the 3DEG the Fermi-Level within the GaN layers will come close to the GaN conduction band as it happens for the 2DEG in the GaN layer.

The main difference between the simulated and real structure is thus expected to be in the lack of the AlGaN layer beneath the field-plate (FP) contact which will thus change the voltage at which the FP depletes the electron channel.

As reported in [16], the drain voltage V_{FP} at which the channel pinches off under the FP is given by $V_{FP} = q^*ns/C_{FP}$ where q*ns is the charge density of the channel and C_{FP} is the channel to FP capacitance per unit area. C_{FP} is calculated by the in-series addition of capacitance of each layer. Calculating the V_{FP} values for the simulated and real device structures approximately 18V and 20V are obtained when neglecting or including the AlGaN layer, respectively. The difference is within 10% but, probably more significant, both values are well below the 100V drain voltage applied during the off time interval ensuring that the FP action on the device channel is properly emulated also in the simplified structure adopted for numerical simulations.

We can thus conclude that for a qualitative analysis where the trap inducing the observed R_{ON} variation is located in the buffer layers the substitution of the AlGaN/GaN interface with a thin n-doped GaN layer should not affect significantly the final goal of providing a qualitative representation of the experimental results.

V. CONCLUSION

A detailed analysis of the R_{ON} increase experienced by normally-off GaN HEMTs operated in pulse-mode conditions has been presented. A clear correlation between the experimental data and the numerical simulation in the device operative conditions explains in detail the degradation phenomena. It was demonstrated that the R_{ON} drift can be related to two different reasons: the hole-emission process from carbon-related traps during the off-state condition and the lacks of a holes source within the semiconductor structure. In particular, this last one suppress the hole capture process that should take place during the on-time interval of the switching period.

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