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High Conversion-Gain Pinned-Photodiode Pump-Gate Pixels in 180-nm CMOS Process

SONG CHEN (Student Member, IEEE), JIAJU MA (Student Member, IEEE), DONALD B. HONDONGWA (Student Member, IEEE), AND ERIC R. FOSSUM (Fellow, IEEE)

Thayer School of Engineering at Dartmouth, Hanover, NH 03755-8000, USA

CORRESPONDING AUTHOR: S. CHEN (e-mail: song.chen.th@dartmouth.edu)

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ABSTRACT This paper presents the design and characterization of high conversion-gain pixels in a 180-nm CMOS image sensor process. By reducing overlapping capacitance between a floating diffusion and transfer gate, output-referred pixel conversion gain as high as 118uV/e- and read noise as low as 1.8e- rms are experimentally achieved without significant lag. A dark current of 38 pA/cm^2 is measured at 60 °C. Comparison between the proposed devices and a baseline pixel regarding device structure and characterization results is also presented.

INDEX TERMS CMOS image sensor, high conversion gain, pump gate, low light imaging, pinned photodiode.

I. INTRODUCTION

Image sensors capable of high-performance low-light imaging are demanded in many industrial, scientific and medical applications. Due to limited signal level under low-light conditions, ultra-low read noise (e.g., deep sub-electron read noise) is desired to maintain high signal-to-noise ratio. The main approaches to this are either to increase the signal prior to the introduction of readout circuit noise and/or reduce the noise. To reduce the circuit's 1/f noise and RTS noise contributions, buried-channel transistors [1] and cooling [2], have been explored, and Correlated Multiple Sampling (CMS) [3], [4] to provide better noise rejection has been successfully demonstrated. Single-Photon Avalanche Diodes (SPAD) [5] that increase signal gain by avalanche multiplication in a high electric field region are commonly used in photon-counting applications. In-pixel amplifier gain has also been investigated [6]. When pixel fill-factor, readout speed, manufacturability and practicality are considered, each of these approaches has its limitations.

Our approach is to increase pixel conversion gain (μV/e-) to boost the signal before noise is introduced, effectively reducing input-referred read noise. This approach has been used in our Quanta Image Sensor (QIS) research [7] and is primarily achieved by reducing the capacitance of the floating-diffusion (FD) node. As pointed out in [8], the overlapping capacitance between FD and transfer gate (TG) is a significant portion of FD capacitance. Recently, several groups have worked on reducing this capacitance [8]–[14]. A vertical transfer pump-gate with distal FD was described in [8]–[10] that transfers the carriers over a virtual-phase [15] barrier to the FD. That concept was inspired by a pinned-photodiode pump-gate (PPD-PG) device without a distal FD (but with distal storage node) that was described by Aptina in [16] for global-shutter pixels, although in the Aptina device, the pump-gate was intended to be cycled several times to fully transfer charge from the PPD to the storage node. In the work of Seo *et al.*, the PPD p+ pinning layer implantation is extended to the edge of FD in [11] and [12] to place a fully-depleted-diode structure between TG and FD. A self-aligned source/drain (S/D) offset structure is proposed in [13] and [14] by omitting LDD implantation and channel stop under FD.

A challenge faced by high conversion gain (CG) pixels, including those of this work, is to achieve high dynamic range. This is because a given output voltage corresponds to fewer signal electrons, with concomitant lower SNR. At saturation, this results in lower dynamic range. Digital integration [17] has been proposed to sum multiple readouts to extend the dynamic range of high CG pixels and can

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TABLE 1. High CG pixels from various references.

Ref #	Conversion Gain (uV/e-)	Read Noise (e- rms)	Pixel Size (um)	Process Node (nm)
[10]	250/413	0.38/0.29	1.4x1.4	65
[12]	220	0.27	11.2x5.6	110
[14]	243	0.46	5.5x5.5	180
Our work	118	1.8	3.6x3.6	180

be used with our devices if needed. A lesser challenge relates to pixel fill-factor. To reduce capacitance between pixel elements, high CG pixels have lower fill factor in front-side illuminated devices. Backside illuminated devices are less constrained.

The high conversion gain PPD-PG pixels proposed in this paper are different from our prior small-pitch backside-illuminated vertical-transfer pump-gate pixels for the QIS. The PPD-PG pixel enables application with larger pixel, front-side illuminated (FSI) devices. Compared to [16], the focus is on high conversion gain and a single transfer. Only minor adjustment (or no adjustment) is needed in the fabrication process. The pixels also have higher full-well capacity compared to QIS jots.

In this paper, a 3.6μm pitch PPD-PG pixel is implemented in a 180nm FSI CIS process. Testing results show that the pixel-output-referred conversion gain is successfully boosted over 55% from 76μV/e- to as high as 118μV/e- enabling average pixel read noise as low as 1.8e- rms. Table 1 summarizes the high CG pixels reported in various references. Further improvement in read noise can be achieved by incorporating the techniques described in [14]. Higher CG may be obtained from the reduction of FD junction capacitance by canceling the channel stop implantation under FD thereby decreasing the p-type doping concentration. Use of a buried-channel source follower and floating capacitor load readout can also improve read noise. These techniques are compatible with our PPD-PG pixels and would be useful in the development of a next-generation device.

II. DEVICE CONCEPT AND DESIGN

A. DEVICE CONCEPT

Figure 1(a) shows a schematic of the PPD-PG pixel. There are two main parts in the structure which differentiate the PPD-PG pixel from a traditional 4T pixel: (1) The FD region is distal - a gap exists between the right edge of TG and FD; (2) a lightly doped p-type region, called the virtual-phase potential barrier (VB) bridges the channel under TG to FD. The part of VB under TG is labeled as VB-I, and the part of VB between TG and FD is labeled as VB-II. Similar techniques were proposed in [15] and [16], but the virtual barrier in those devices is designed to be strong enough to hold charge under TG when TG goes high. In the PPD-PG device, it is expected that most of charge goes to FD.

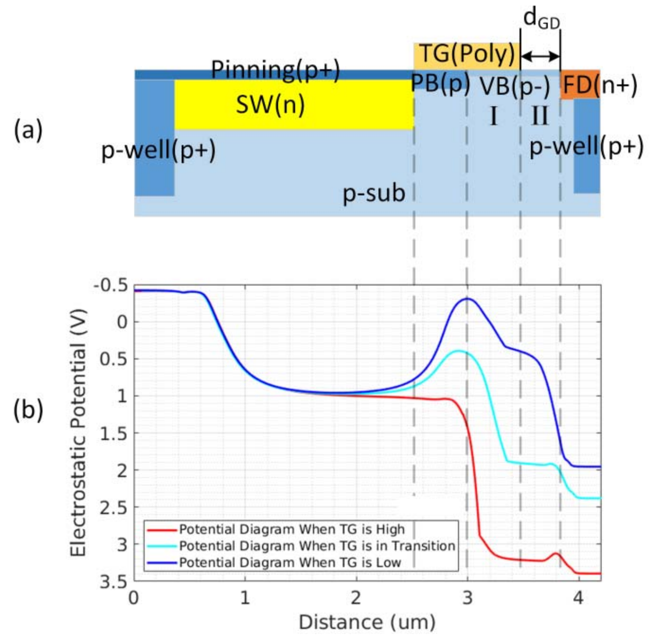


FIGURE 1. (a) Schematic cross section of the proposed PPD-PG pixel. (b) Potential diagram and charge transfer path when TG is high, low and in transition.

Figure 1(b) shows corresponding potential diagrams in one TG pulse extracted from TCAD 2D simulation using X-FAB 180nm CIS process conditions. When TG is high, the channel under TG opens and all carriers in the pinned-photodiode (PPD) are transferred out towards the FD node. Some of the carriers are left in the channel because of the small potential barrier in the gap between TG and FD. However, as TG transitions from high to low, the rest of carriers are "pumped" to FD.

B. REDUCE OVERLAPPING CAPACITANCE

Similar to the BSIM3v3 model for MOSFET [18], parasitic capacitance between TG and FD, C_{GD}, can be characterized by the sum of three components: (1) non-LDD region overlapping capacitance C_{ov}, (2) LDD region overlap capacitance C_{ov_LDD} and (3) fringing field capacitance C_F.

The capacitance C_{GD} was extracted for different gap size d_{GD} (measured as the distance from the right edge of TG to the left edge of FD mask, as shown in Fig. 1(a)) from TCAD 2D simulation to show how the capacitance between TG and FD changes as FD is moved away from TG. Simulation results are plotted in Fig. 2 as a set of solid curves. A second set of curves (dashed) show the relationship without LDD implantation. The spread between corresponding curves in the two sets approximates the value of C_{ov_LDD}. Note that device width (in the direction looking into the cross section) is assumed to be 0.42μm in TCAD 2D simulation. The sidewall spacers are also simulated. LDD implantation is included unless otherwise specified.

Two observations should be noticed in Fig. 2. First, the value of C_{GD} drops significantly as we move FD away

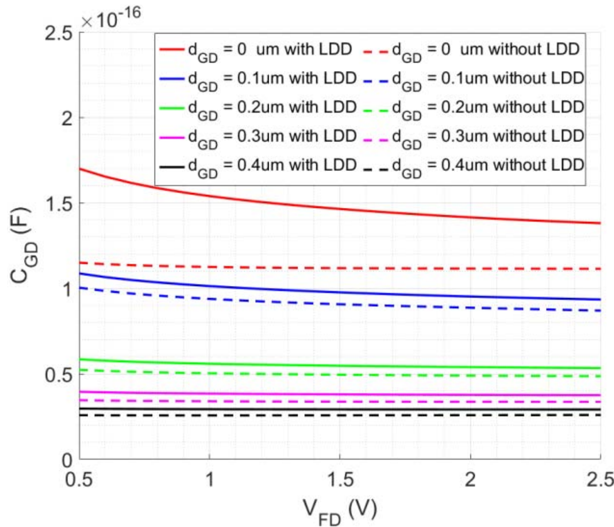


FIGURE 2. Parasitic capacitance between TG and FD, C_{GD} vs. voltage on FD node V_{FD} for different gap size d_{GD}.

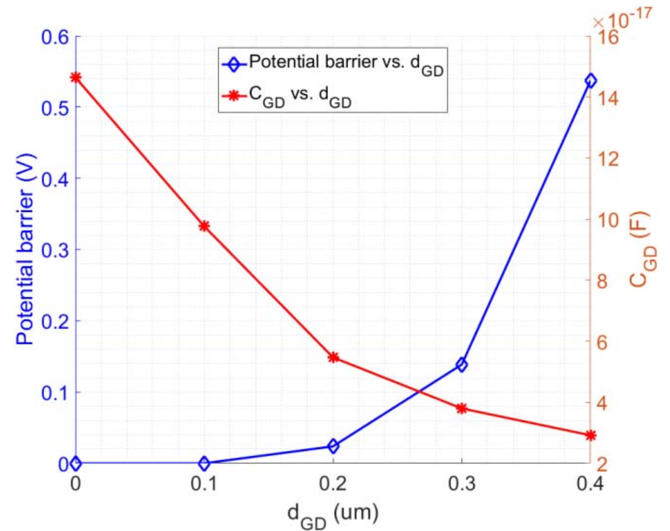


FIGURE 3. (1) Potential barrier in VB-II vs. different gap size d_{GD} when TG is high (2) C_{GD} vs. different gap size d_{GD} when TG is low and V_{FD} =1.5V.

from TG by 0.2 μm. Second, in a normal pixel, i.e., when $d_{GD} = 0$ μm, the value of C_{GD} in the curve without LDD is lower than the one with LDD. One concludes that C_{ov} and C_{ov_LDD} are major components in C_{GD} and the overlapping capacitance approaches zero as the overlap between two plates of capacitor gets smaller. This discussion gives important guidance for PPD-PG pixel design: a gap size above 0.2 μm is needed to significantly reduce overlapping capacitance.

C. THE EFFECT OF POTENTIAL BARRIER IN VB-II

The region VB-I is right under TG, so its potential is directly modulated by TG. VB-II, the gap resulting from moving FD away from TG, is mostly modulated by the lateral electrical field from FD and TG. Full and efficient charge transfer can only happen if (1) no potential barrier exists in VB-II when TG is low and (2) only a small barrier exists in VB-II when TG is high.

Because of how FD is made, the doping concentration in VB-II is lower than VB-I. To prevent the implantation of the p-well under FD from affecting the doping concentration in VB-II, the left edge of the p-well was moved slightly to the right. When TG is low ($V_{TG} = 0\ V$) and FD is at a higher voltage ($V_{FD} > 0.5V$) after charge transfer, VB-II will be fully depleted and the potential will monotonically increase from VB-I to VB-II. As shown in the simulated potential diagram in Figure 1(b), condition (1) is satisfied.

The relationship between potential barrier in VB-II when TG is high and the size of gap d_{GD} between TG and FD in TCAD simulations was also explored. As shown in Figure 3, when d_{GD} goes above 0.30μm, the potential barrier is high while reduction in C_{GD} is not significant.

A potential hazard in this pump-gate operation is that charge in VB may backflow to SW when TG goes low. A baseline 4T pixel has similar problem regarding charge in the channel under TG. As a result, a potential barrier between SW and VB is needed when the channel is closing to prevent this from happening. The p-type region PB under TG is serving this purpose. PB also exists in baseline 4T pixel but we increased its doping concentration to make the barrier slightly stronger as the pump operation is relatively slower than normal charge transfer.

III. DESIGN VARIATIONS

The gap size d_{GD} is chosen as 0.30μm mainly based on previous discussion on overlapping capacitance reduction and potential barrier in Sec. II. Also, the possible C_{GD} variation caused by misalignment is only around 0.025fF for d_{GD} within the range of 0.30μm±0.10μm. Since the VB region is critical to pump-gate pixel's performance, including conversion gain and lag, design variations in layout for this region were used in the test chips. For comparison, baseline 4T pixels developed by collaboration between our group and X-FAB, are also measured and reported in this paper.

Figures 4 (a) and (b) show layout schematics of the two proposed pump-gate pixel designs. The main difference between these two is the way the width of VB region along *YY'* is defined. In figure 4(a), boundaries are defined by shallow trench isolation (STI) while in figure 4(b) boundaries are defined by heavily doped p-well. The difference is more clearly shown in cross section view along *YY'* for two different layouts in figure 5. To account for the feature enlargement due to lateral straggle of the heavy implantation for p-well, the VB region in figure 5(b), which has a width of 0.50μm, is designed to be wider than the VB region in figure 5(a), which has a width of 0.41μm. Figure 4(c) shows the layout of the baseline pixel. All pixels have a pitch of 3.60μm.

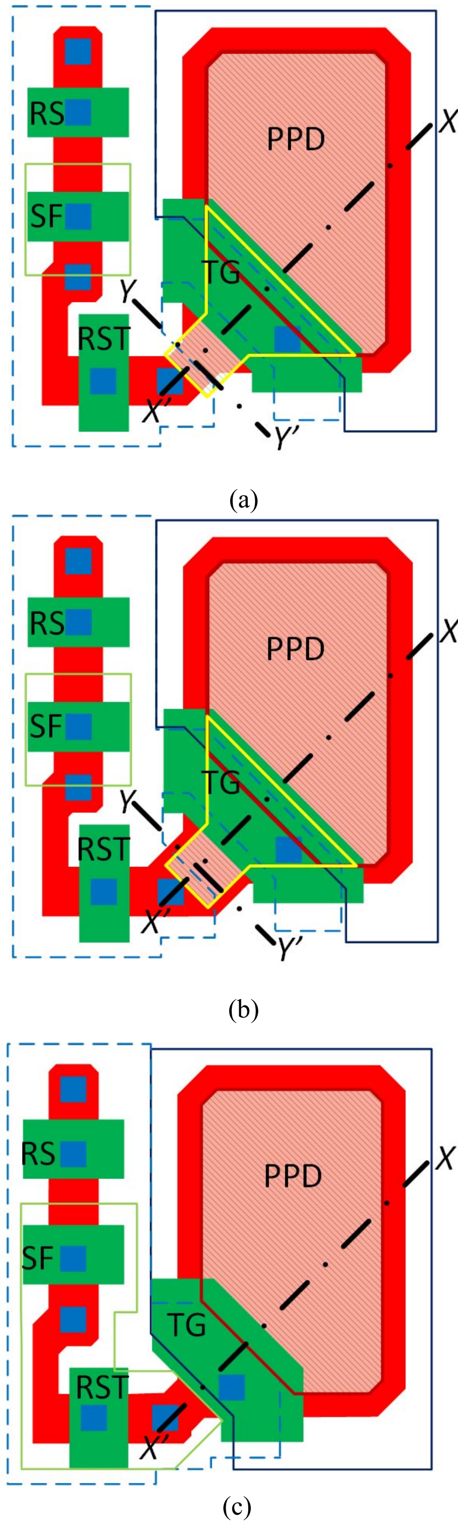


FIGURE 4. Layout schematic of tested pixels (a) PPD-PG with narrow VB region. (b) PPD-PG with wide VB region. (c) Baseline pixel.

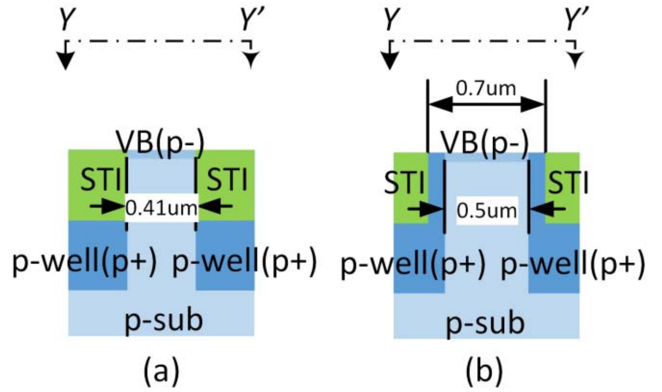


FIGURE 5. Schematic cross-section view of tested PPD-PG pixels along *YY'* (a) PPD-PG pixel with p-type and narrow VB. (b) PPD-PG pixel with p-type and wide VB.

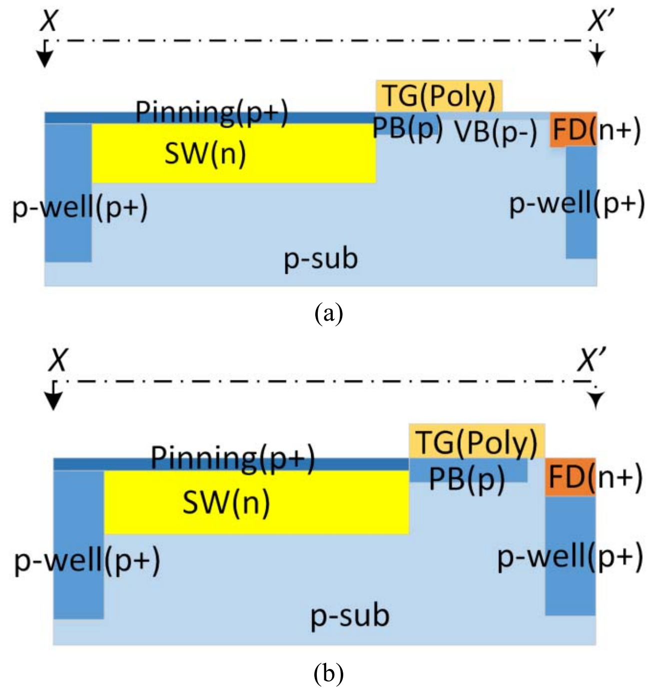


FIGURE 6. Schematic cross-section view of tested pixels along *XX'* (a) PPD-PG pixel. (b) Baseline pixel.

Figure 6 shows illustrations of the schematic cross-section views of pump-gate and baseline pixels. TCAD simulations are based on actual 4T pixel fabrication processes.

Three different types of pixels were designed as summarized in Table 2.

IV. CONVERSION GAIN AND CONVERSION GAIN VARIATION

The photon transfer curve (PTC) method is used to extract conversion gain of the pixels. For each type of pump-gate pixels, 2000 frames of data are collected from a 150(row) x 50(column) pixel array at each light level and 4000 frames of data are collected for baseline pixels as the array size is smaller, i.e., 150x25. Figure 7 shows PTC curves from measurement. Mean slope of PTC curve is used to calculate the pixel output-referred conversion gain (CG). A small non-linearity is observed in the PTC curves in the low signal region, suggesting lower CG at low signals. This is counter to an expectation of lower capacitance of FD at higher voltages. The cause of the non-linearity on the PTC curves is not

TABLE 2. Design variations of all tested 6 pixels.

Pixel type	Structure	Layout	Schematic cross-section view	VB region property	
PPD-PG pixel (PG implant, narrow VB)	PG pixel	Fig. 4(a)	Fig. 6(a)	p-type	Narrow
PPD-PG pixel (PG implant, wide VB)	PG pixel	Fig. 4(b)	Fig. 6(a)	p-type	Wide
Baseline pixel	Baseline pixel	Fig. 4(c)	Fig. 6(b) modified	-	-

known at this time, but non-linearity in the readout chain is one possibility since the linearity of the PTC curves improves as we improve the linearity of the readout chain by biasing. This small non-linearity does not impact the conclusions of this work but should be investigated in the development of a next-generation device.

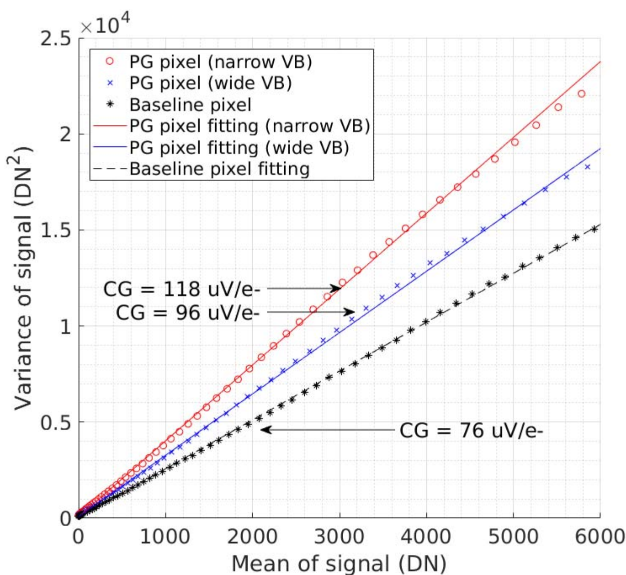


FIGURE 7. Photon transfer curves of tested pixels.

One concern about high CG pixels is CG variation. To characterize CG variation, the central 140(row) x 40(column) pixels out of the 150x50 array for each type of pump-gate pixel were measured at around 500e- signal level using the PTC method and 100,000 samples are taken for each pixel at each light level. The same measurement is performed on baseline pixels but with a smaller array size, i.e., 140x20. Gain variation in each column-parallel readout channel can cause systematic column-wise CG variation in measurement. Double Delta Sampling (DDS) and calibration are used to suppress this effect. The distributions of CG for each type of pixel array are also shown in a histogram in figure 8. The mean value and standard deviation of each histogram are summarized in table 3.

CG variation of the proposed pixels are higher than baseline pixels. It is suspected that this is due, in part, to the floating diffusion not being self-aligned to the transfer gate, resulting in higher variations in the floating diffusion area. More investigation would be necessary to pinpoint the exact cause of this variation.

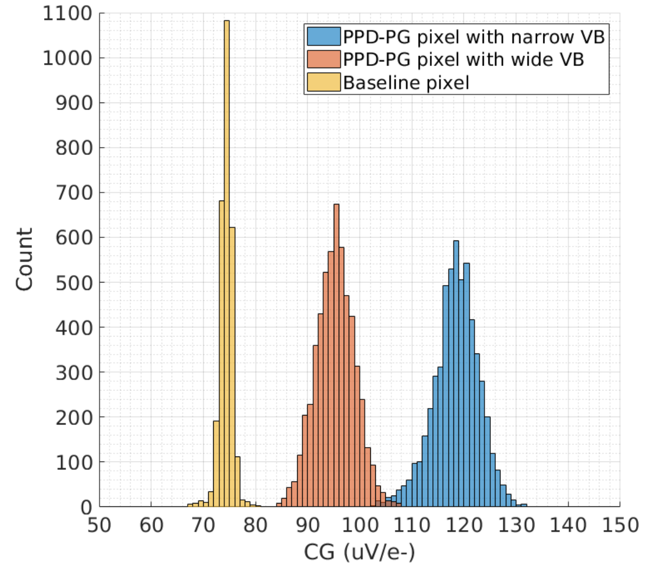


FIGURE 8. Histogram showing CG distribution of each type of pixel array.

TABLE 3. Statistical characteristics of cg for pump-gate pixels.

Pixel type	CG mean value (uV/e-)	CG standard deviation (uV/e-)	CG standard deviation/mean value percentage
PPD-PG pixel (PG implant, narrow VB)	118	4.4	3.7%
PPD-PG pixel (PG-implant, wide VB)	95	3.7	3.9%
Baseline pixel	74	1.3	1.7%

V. READOUT NOISE

The direct benefit of the high conversion gain of the pump-gate pixels is improving the input-referred readout noise performance. Measured results are summarized in table 4. Please note that all the results are shown in median value. The CG of pump-gate pixels with narrow VB is about 55% higher than the CG of baseline pixels and the measured input-referred noise is 37% lower. Figure 9 shows the probability vs. pixel read noise for each type of pixel. The input-referred pixel read noise of each pixel in figure 9 is calculated by dividing read noise in voltage by the CG of that pixel. All horizontal axes are aligned and on the same scale and it is seen that pump-gate pixels have lower read noise. According to [19], long tails in histograms might be attributed to low-frequency-noise sources such as random-telegraph-signal (RTS) noise, and an empirical model can be applied.

TABLE 4. Input-referred readout noise of all tested pixels (at median value).

Pixel type	Readout noise contributed by pixel (e- rms)	Readout noise contributed by circuits after pixel (e- rms)	Total readout noise (e- rms)
PPD-PG pixel (PG implant, narrow VB)	1.81	1.77	2.55
PPD-PG pixel (PG-implant, wide VB)	2.00	2.21	2.99
Baseline pixel	2.89	3.09	4.23

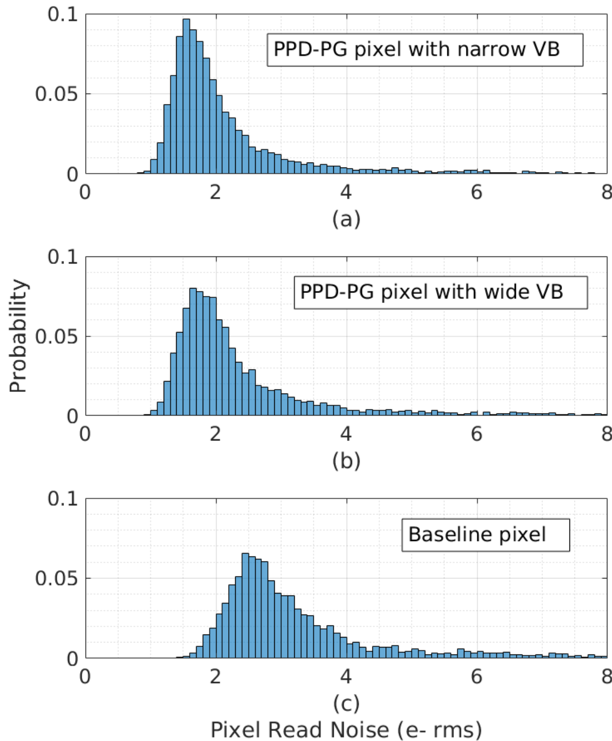


FIGURE 9. Histograms showing distribution of pixel read noise based on measured pixel arrays. (a) PPD-PG pixel with narrow VB. (b) PPD-PG pixel with wide VB. (c) baseline pixel.

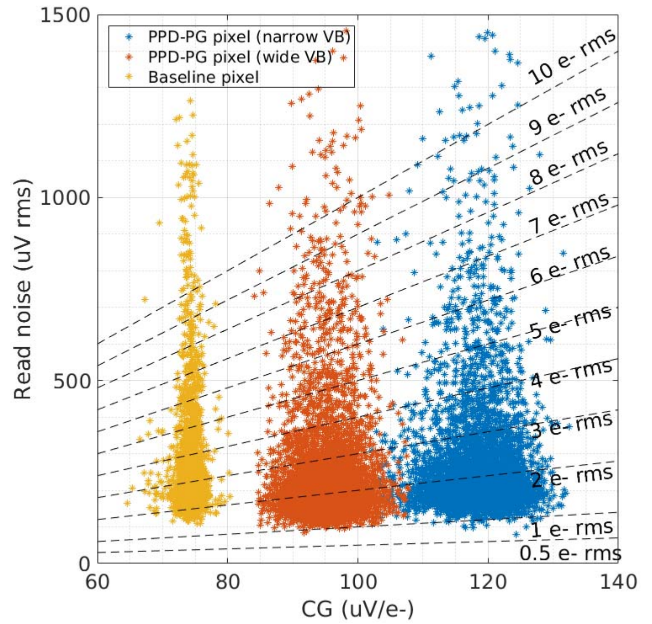


FIGURE 10. Scatter plot of measured pixel read noise vs. CG for PG pixel with narrow VB, PG pixel with wide VB and baseline pixel.

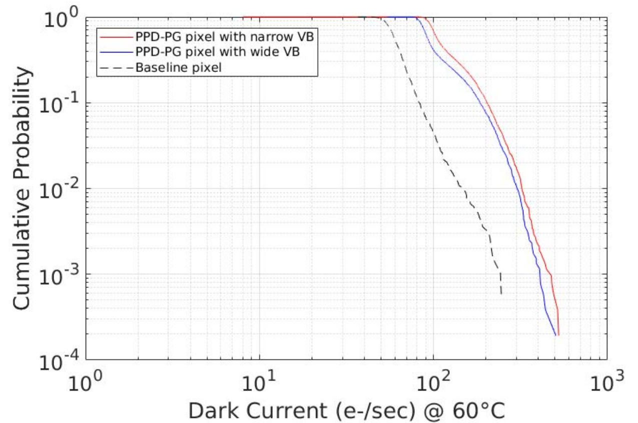


FIGURE 11. Cumulative probability of the pixel dark current value at 60 °C.

Figure 10 shows a scatter plot of measured read noise in uV rms vs. CG in μV/e- for each type of pixels. Note that the number of pixels measured for the PG pixels are twice that of baseline pixels because of different array sizes. Compared to baseline pixels, the PG pixels are found to have higher read noise variation which is likely caused by slightly smaller SF gate size and floating diffusion area variation.

VI. DARK CURRENT

Besides finely tuning the fabrication process, another common technique to suppress dark current in 4T pixel is a careful design of the channel under TG. A monotonically increasing potential profile in the channel from PPD side to FD side when TG is low helps dump dark current generated under TG to FD node instead of storage well of PPD [20]. As shown in cross section view of tested pixels in figure 6, the PB region plays an important role in creating this monotonically increasing potential profile. In order to add the VB region in pump-gate pixels while maintaining the same transfer gate length, the PB region in pump-gate pixels has to be smaller than in baseline pixels. This difference in PB region also leads to a slightly lower threshold voltage of TG in pump-gate pixels which affects their dark current performance. Therefore, pump-gate pixels show relatively higher dark current than baseline pixels. The design of pump-gate pixels can be improved by shortening the VB region which could be adopted in future designs.

Dark current of all types of pixels are measured at 60°C. Baseline pixels show the best dark current performance which is 25.9 e-/sec (32.1 pA/cm^2). PPD-PG pixels also demonstrate comparable dark current levels. Dark current for PPD-PG pixels with narrow VB is 31.2 e-/sec

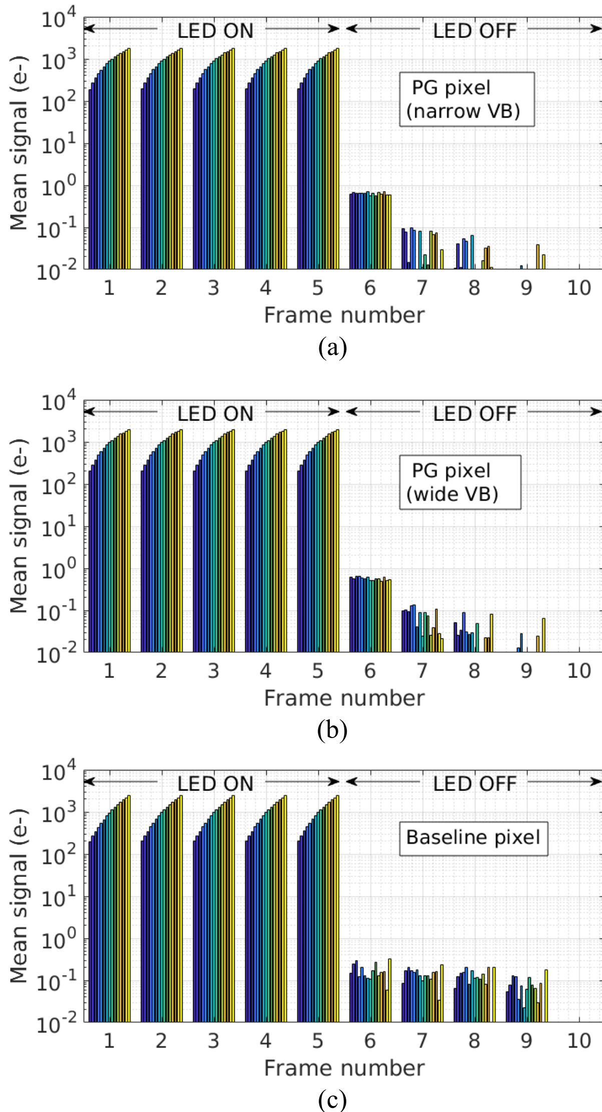


FIGURE 12. Lag measurement for each type of pixel for 5 illuminated frames followed by 5 dark frames. Each frame set represents 15 different signal levels ranging from 100e- to 2500 e-. TG high is 3.3V; TG low is 0V; TG turns on 1us for each transfer. (a) PPD-PG pixel with narrow VB. (b) PPD-PG pixel with wide VB. (c) baseline pixel.

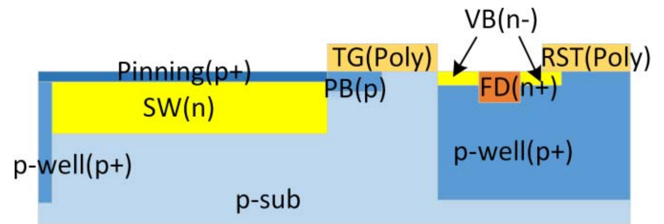


FIGURE 13. Schematic cross section view of proposed pixels including PPD, TG and RST.

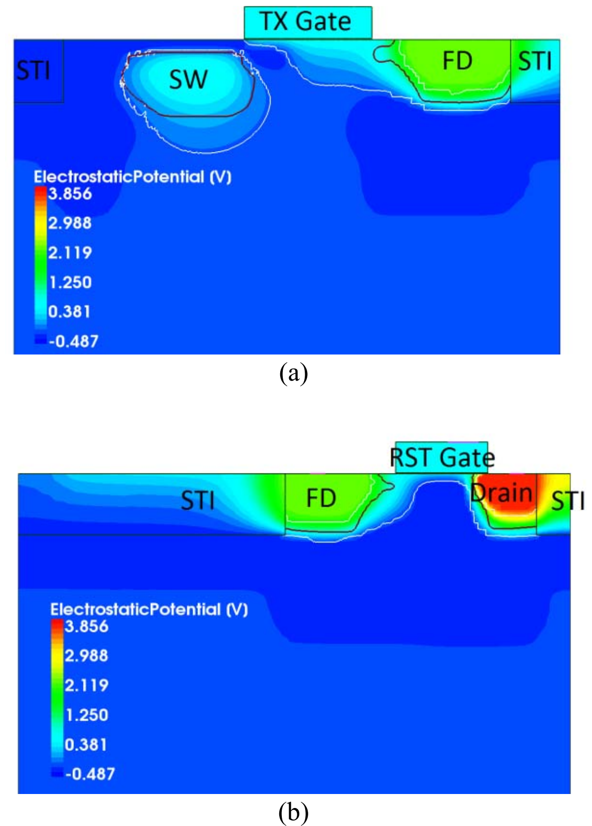


FIGURE 14. Schematic cross-section view of the proposed pixel's electrostatic potential profile from (a) PPD to FD, (b) FD to drain of reset transistor.

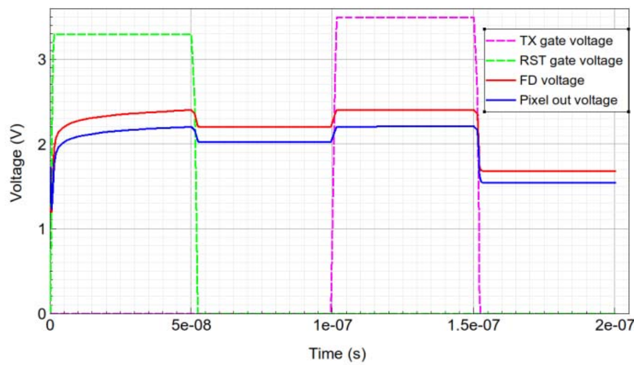
(38.4 pA/cm^2); dark current for wide VB is 32.3 e-/sec (39.9 pA/cm^2).

Cumulative probability of pixel dark current value at 60°C is also depicted in figure 11. The number of pixels measured for each type of pump-gate pixel is 5600 (140x40 array). The number of pixels measured for baseline pixels is 2800 (140x20 array).

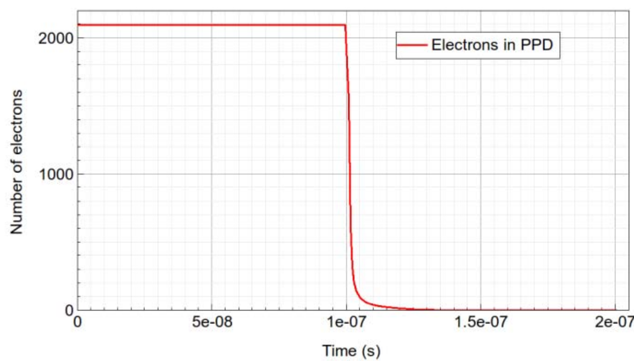
VII. LAG

As discussed above, charge transfer from the storage well in the PPD to the FD node in pump-gate pixels is completed in two steps. Each step has the potential to cause image lag. In the first step, TG is high and charge is transferred from SW to the part of VB region under TG. If a potential barrier in PB exists, it would result in lag. A higher TG on voltage would help to eliminate this lag. A longer TG turn-on period is also helpful in this situation. In the second step, TG is low and charge is pumped to FD node. If a potential barrier exists in VB-II between TG and FD, there would be some charge left in VB to cause lag. A lower TG off voltage (may go negative) would help to eliminate lag in this step.

To perform a fair comparison, all measurements for image lag are done with TG high at 3.3V, TG low at 0V and TG turn-on period equaling 1µs for each transfer. Except the first TG pulse, each TG pulse marks the end of integration for current frame and the starting of integration for next frame. 15 different input signal levels are measured for each type of pixel. The mean value of input signal is controlled within 200e- to 2000e- range. The results are shown in figure 12.



(a)



(b)

FIGURE 15. Transient simulation results of the proposed pixel from TCAD 3D device simulation (a) Voltages (b) Electrons in PPD storage well.

Both pump-gate pixels and baseline pixels show image lag less than 1 electron. Also, the amounts of charge content observed in Frame #6 are almost independent of input signals levels in figure 12. Thus, the image lag is unlikely caused by slow charge transfer. Instead, a small potential barrier should account for the charges left behind.

VIII. PROPOSED FUTURE IMPROVEMENT

The fabricated pump-gate pixels can be improved in the future in two aspects: (1) Making them more compatible with the standard CIS process by using existing mask and implantation steps; (2) Enhancing CG further by applying a similar principle to reduce overlapping capacitance between FD and reset gate. A schematic cross section view of modified pixel design is shown in figure 13. The dedicated VB implantation is removed. Instead, p-well implantation for buried channel nMOS is used. The reset gate is moved away from FD around 0.25um.

TCAD 3D device simulation shows that the regions between FD and TX gate, and FD and reset gate are fully depleted. The white lines in figure 14 represent the boundaries of depletion regions. Thus, the overlapping capacitances between FD and TX, FD and reset gate are both reduced significantly comparing to normal pixel.

FD can be easily reset to above 2V even with a normal 3.3V high level on reset gate which is an advantage over the design in [12]. Figure 15 shows transient simulation results from TCAD. The conversion gain of proposed pixel calculated from simulation results is around 250uV/e- on FD and 231uV/e- at the pixel output (source of row select transistor).

TABLE 5. Characterization results of all tested pixels.

Pixel type	PPD-PG pixel (narrow VB)	PPD-PG pixel (wide VB)	Baseline pixel
Pitch Size (um)	3.6	3.6	3.6
SF Size (um)	0.42x0.42	0.42x0.42	0.42x0.5
Col. Bias Current (uA)	1.5	1.5	1.5
CG (uV/e-)	118	96	76
CG Variation	3.7%	3.9%	1.7%
Total Read Noise at median (e- rms)	2.55	2.99	4.23
Dark current (pA/cm^2) @60°C	38.4	39.9	32.1
Lag (e-)	<1	<1	<1
Full Well Capacity (e-)	5800	5800	6500

IX. CONCLUSION

In this paper, the design of pump-gate pixels with boosted conversion gain up to 118 uV/e- was discussed. With only minor adjustment in standard CIS process, the overlapping capacitance between FD and TG, including LDD region and non-LDD region, is significantly reduced. Two layout design variations (narrow VB and wide VB) for pump-gate pixels are explored. Both types of pump-gate pixels demonstrate higher conversion gain and lower input-referred noise than baseline pixels. Good dark current performance is observed for all tested pixels. Characterization results of all types of pixels are summarized in table 5. Possible improvements in the PPD-PG pixels were discussed and simulated using TCAD. Additional noise improvement may be possible with source-follower optimization such as by using buried-channel transistors instead of surface-channel transistors.

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SONG CHEN (S'12) received the B.E. degree in electrical engineering from Zhejiang University, China, in 2012. He is currently pursuing the Ph.D. degree with the Thayer School of Engineering at Dartmouth. His research interests include time-resolved CMOS image sensors and high-speed low-noise readout circuit design.

JIAJU MA (S'12) received the B.S. degree in physics from Nankai University, China, in 2012. He is currently pursuing the Ph.D. degree with the Thayer School of Engineering at Dartmouth. He is exploring low-noise CMOS image sensor pixel devices for quanta image sensor and other photon-counting imaging applications.

DONALD B. HONDONGWA (S'12) received the B.A. degree in physics from Vassar College, Poughkeepsie, NY, USA, in 2011 and the B.E. degree from the Thayer School of Engineering at Dartmouth, Hanover, NH, USA, in 2012, where he is currently pursuing the Ph.D. degree focusing on advanced imaging technologies, CMOS image sensor design, photon counting, and imaging applications.

ERIC R. FOSSUM (S'80-M'84-SM'91-F'98) is a Professor with the Thayer School of Engineering, Dartmouth. He is the primary inventor of the CMOS image sensor used in billions of camera phones and other applications and is a 2017 Queen Elizabeth Prize Laureate. He was inducted into the National Inventors Hall of Fame and is a member of the National Academy of Engineering. He is a co-founder and Past President of the International Image Sensor Society. He is currently exploring the quanta image sensor.