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Simulation Study of Vertically Stacked Lateral Si Nanowires Transistors for 5-nm CMOS Applications

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ABSTRACT In this paper, we present a simulation study of vertically stacked lateral nanowires transistors (NWTs), which may have applications at 5-nm CMOS technology. Our simulation approach is based on a collection of simulation techniques to capture the complexity in such ultra-scaled devices. Initially, we used drift-diffusion methodology with activated Poisson–Schrodinger quantum corrections to accurately capture the quantum confinement in the cross-section of the device. Ensemble Monte Carlo simulations are used to accurately evaluate the drive current capturing the complexity of the carrier transport in the NWTs. We compared the current flow in single, double, and triple vertically stacked lateral NWTs with and without contact resistance. The results presented here suggest a consistent link between channel strain and device performance. Furthermore, we propose a device structure for the 5-nm CMOS technology node that meets the required industry scaling projection. We also consider the interplay between various sources of statistical variability and reliability in this paper.

INDEX TERMS Nanowire transistor, TCAD, Monte Carlo, vertically stacked.

I. INTRODUCTION

In recent years, the Fin field effect transistor (FinFET) has been introduced as a technology solution designed to tackle the challenges facing the semiconductor industry, such as high leakage current, short-channel effects, and performance degradation in extremely scaled planar MOSFETs [1], [2]. Currently, the 7 nm FinFETs are under intensive development [3]. To continue to maintain the scaling of the technology the FinFET size must be reduced significantly [4]. However, scaling down the fin width of the FinFET increases the process variability and the device's statistical variability [5]. For example, in order to improve the drive current the fin must be taller and narrower, making it very hard to control the channel shape and geometry. Therefore, further scaling of the FinFET transistors will be extremely challenging.

A possible alternative device architecture that could replace Si FinFET, before looking to alternative channel materials, is the nanowire transistor (NWT) [6]. The excellent electrostatic integrity offered by gate-all-around NWTs makes them one of the most prominent candidates for replacing FinFET for the next generation technology node [7].

To maintain the performance boost, the industry is considering a 15% increase of the existing saturation current (I_{sat}) required for 7 nm and 5 nm technology nodes in comparison to the previous generation transistor. As shown in Table 1 and Fig. 1 (right-hand-side), considering three technology nodes after 14 nm FinFET, the target value of the I_{sat} for the 5nm transistor is close to 1.6 mA/μm.

The possibility of creating a transistor with two lateral nanowires channels as a single device to tackle the challenge

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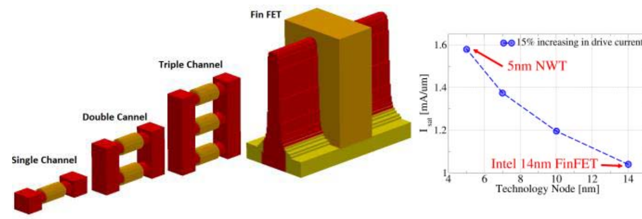

FIGURE 1. 3D schematic view of the Intel 14nm FinFET and Single, Double, Triple 5nm Si nanowire transistors (NTWs) and material information for the two channel Si NWT and the scaling target from 14nm technology to 5nm technology (left).

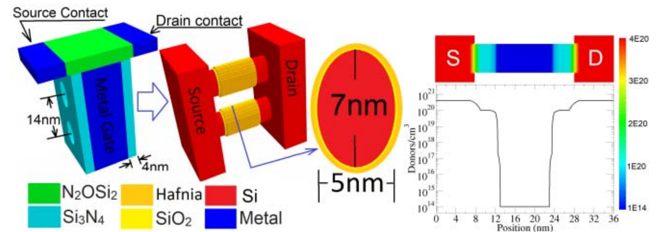

FIGURE 2. (left) 3D schematic view a Si nanowire transistor (NTW) and material information for the two channel Si NWT. (right) The doping profile of the Si NWT.

TABLE 1. Technology node and related saturation current and pitch.

Node	14nm	10nm	7nm	5nm
Lay-out pitch (nm)	42	29	21	14
I_{sat} (x15%) mA/um	1.04	1.196	1.375	1.58

of performance degradation shown in a single NWT has been reported in [8]–[10]. The 7nm FinFETs chip must have taller fins to boost the drive current. On the other hand, the vertically stacked lateral Si NWT will have less than average height of FinFETs at 7nm technology node and beyond with smaller chip footprint.

The electron transport properties in Si NWTs could be engineered precisely to reach the industrial target of improving the saturation current by 15% for each generation. The increase in performance can be achieved by the following approaches: introducing strain in the channel, engineering the device structures such as cross-sectional geometries and channel orientations, and using devices with multi-lateral channels. Additionally, the trade-off between performance and leakage currents can be achieved by engineering the device structures.

The research to date has focused on the simulation of NWTs as a mono (single) channel. Insufficient attention has been paid to the simulation of NWTs with multi-lateral channels with a 5-nm node. Therefore, in this work we seek to fill this gap by presenting simulations of NWTs with multiple channel lengths and number of lateral channels. For the results to be realistic, our simulations consider the impact of quantum confinement, non-equilibrium transport, and contact resistance for such ultra-scaled NWTs. We also performed statistical variability SV simulations to evaluate the impact of numerous sources of variability on the NWT performance.

We also seek to answer the following important question: Is it possible to reach the industrial target for a 5nm technology node using a single channel silicon (NWT)? If not, how many lateral channels are needed in one device for this target to be achieved?

The paper is organised as follows: Section II is the device description. Section III describes the simulation methodology. The device calibration methodology is described in Section IV. In Sections V and VI we discuss the results, before drawing the conclusions in Section VII.

II. DEVICE DESCRIPTION

In our previous works [11]–[14], we established a correlation between cross-sectional geometry and electrostatic properties, and performance in ultra-scaled NWTs. Our results showed that NWTs with elliptical cross-section have the best device performance when compared to a cross-section of the square and circular NWTs. Following on our previous work, in this paper we study Si n-channel gate all around NWTs with an elliptical cross-section of 7nm x 5nm. All simulated devices have 0.4nm SiO_2 interfacial and 0.8nm HfO_2 (High-k) layer. The doping concentration in the channel is - $10^{14}/cm^3$, in extensions - $10^{20}/cm^3$, and in source/drain - $4x10^{20}/cm^3$, as shown in Fig. 2. A simulation of four different gate lengths of 10nm, 12nm, 16nm, and 20nm is considered in this work. Furthermore, devices with single, double, and triple channel configurations were simulated. In all devices, the source/drain contacts are on top of the device. The general device structure is illustrated in Fig. 2.

III. METHODOLOGY

The simulation process was performed using Ensemble Monte Carlo (EMC) simulations [15] with Poisson-Schrödinger (PS) quantum corrections as a reference point. Monte Carlo is a direct method for solving the Boltzmann transport equation (BTE), accounting for the stochastic nature of electron transport and important electron scattering events, such as intra-valley and inter-valley electron-phonon scatterings, ionised impurity scattering, and surface roughness scattering.

We use an analytical band structure model including ellipsoidal non-parabolic valleys, derived from a full-bandstructure calculated using the k·p method. The simulation is carried out self-consistently by tracking the trajectory of hundreds of thousands of particles moving in a field distribution, calculated by solving Poisson's equation in 3D, and updated regularly (every 0.5fs). The converged charge and potential profiles from the PS solution are used as initial conditions for the 3D-EMC. The QM correction is applied throughout the simulation period to maintain self-consistent but time-varying electrostatic potential and field distributions. 3D EMC simulations provide accurate physical treatment of the non-equilibrium transport [16] in ultra-scaled channel transistors and provide an accurate prediction of the ON-state transistor performance.

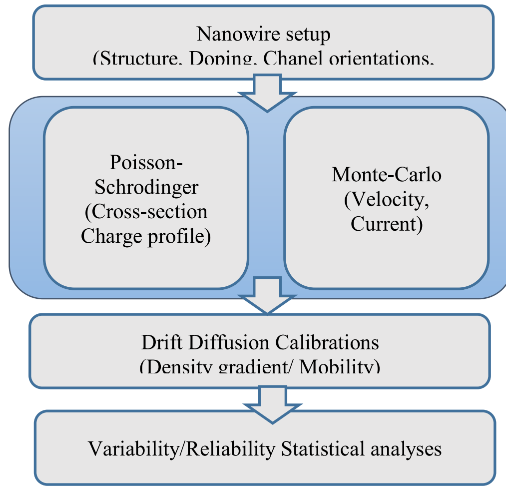

FIGURE 3. Simplify simulation tool flow chart.

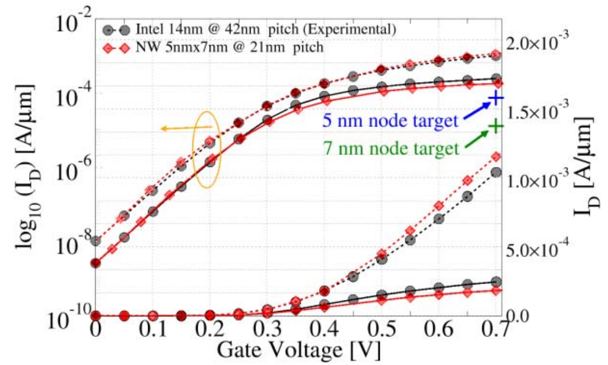

FIGURE 4. I_D-V_G curve compares the experimental performance of Intel 14nm FinFET with the 5nm silicon Nanowire (MC simulations). Dashed lines correspond to high drain voltage $V_D = 0.7V$, while the solid lines are for low drain voltage $V_D = 0.05V$. The gate length of NWT is 12 nm.

Once a satisfactory result is obtained, the DD model is calibrated to this reference data obtained from EMC. This ensures that the DD model reflects and captures all the properties and parameters obtained from MC/PS simulations. This calibrated DD model is then used to perform a comprehensive simulation of statistical variability and reliability and the interaction between them. For each channel length considered in the simulation, an ensemble of 1000 devices was simulated. A high-level flowchart of the simulation process is presented in Fig. 3. In summary, the quantum corrections obtained from PS simulation were imported to the EMC model to accurately capture the charge transport.

IV. DEVICE CALIBRATION

The aim of the drift diffusion calibration is to determine a set of simulation parameters in DD that minimises the difference between device simulation results and target simulation results obtained from other more accurate simulation models, such as EMC [15]. A set of recommended calibration parameters is identified for this purpose, including: the gate work function, density gradient confinement effective mass, and mobility models with their respective parameter values.

The calibration strategy for I_D-V_G curve consists of the following three stages: 1) the sub-threshold region, 2) the low field dependence, and 3) the high field dependence. The calibration stages are ordered such that the effect of calibration of earlier stage parameters is independent of those of later stages, and they will be used in the following stages.

In our simulation, the density gradient effective masses have already been calibrated against Poisson-Schrödinger. At all stages of the calibration the threshold voltage (V_T) can be realigned by adjusting the work function. In DD calibration, up to three mobility models can be selected for use in a given simulation: 1) Low-field mobility (that considers ionised impurity scattering); Arora mobility model [17], Masetti mobility model [18], and Philips mobility model [19]. 2) Perpendicular field-dependent mobility (that considers surface roughness scattering); Yamaguchi [20], Lombardi [21], and thin-layer mobility model [22]. 3) Lateral field-dependent mobility (for velocity saturation); Caughey-Thomas velocity saturation model [23].

The following three carrier mobility models have been used in this work: Masetti, Lombardi, and Caughey-Thomas Models. At low V_D, the NWT I_D-V_G characteristics are determined by the low-field mobility for a gate voltage in the vicinity of V_T. Then the device calibration process is continued using the complete I_D-V_G curve at low drain bias. During the first calibration iteration, a perpendicular electric field model was enabled and the lateral electric field model disabled. In the final stage of the calibration process, the complete I_D-V_G behaviour at high applied V_D is calibrated. The parameters adjusted in the first stage are considered in the second and final iteration stages.

V. RESULTS AND DISCUSSION

Based on the methodology described in the previous section, we simulated the key transistor's characteristics, such as the current-voltage (I_D-V_G) characteristics. Fig. 4 compares the I_D-V_G characteristics of 14 nm FinFET transistor with a single Si-NWT simulated in this work. Those results are then compared to the target drive current (1.58 mA/µm) for the 5 nm CMOS, which we evaluate in the introduction of this work. Both curves are aligned to give the same leakage current. From the results presented in Fig. 4, it is clear that I_{ast} for a single nanowire transistor is higher in comparison to 14nm FinFET. This result is consistent at both high and low drain biases. The SS is ~62.55 [mV/dec], DIBL is ~9.04 [mV/V] More importantly, Fig. 4 reveals that even though the single NWT has a better drive current, the value of the I_{sat} is significantly lower in comparison to our target value of 1.58 mA/µm at high (0.7V) drain bias. Please note that all current in Fig. 4 are normalized per layout width (layout pitch) which are presented in Table 1.

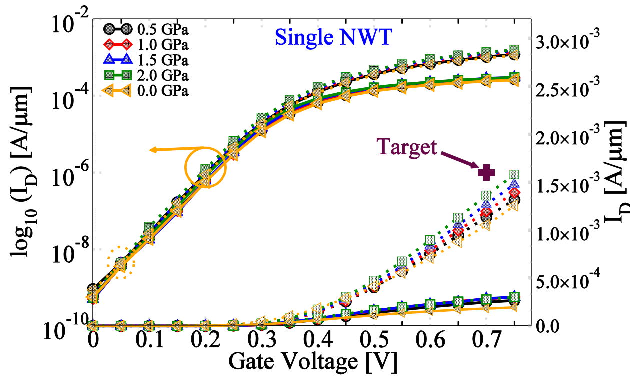

FIGURE 5. I_D-V_G curve compares results for four single 5nm NWTs each with different strain value (MC simulations). Dashed lines correspond to high drain voltage $V_D = 0.7$V, while the solid lines are for low drain voltage $V_D = 0.05$V. The gate length is 12 nm.

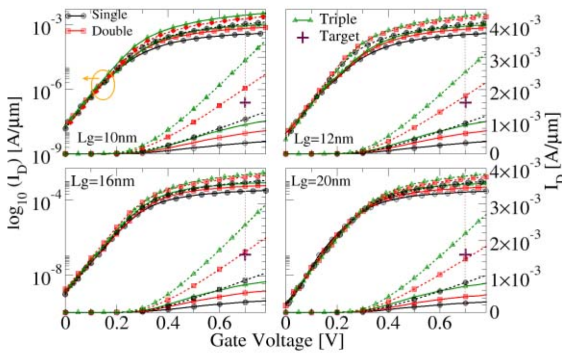

FIGURE 6. I_D-V_G curves based on calibrated DD methods of a single, double, and triple channel Si NWT at four different gate lengths at low (0.05V) and high (0.7V) drain bias. Dashed lines represent 0.7V drain bias and the solid line is for 0.05V drain bias. The contact resistance is not considered in this simulation.

A possible option to improve the I_{sat} current is to introduce strain in the channel. Simulation of the I_D-V_G characteristics of four single NWTs each with different strain value is presented in Fig. 5. From the same figure, it can be concluded that introducing channel strain indeed improves the I_{sat} magnitude by (5%-30%), however the target drive current cannot be reached even at 2.0 GPa strain.

Another option to improve I_{sat} is to introduce multiple channels in a single transistor. Introducing multiple lateral channels is experimentally challenging, but possible. In Fig. 6, we compare the devices with four different gate lengths in single, double, or triple channel. Careful analysis of this data leads to the following conclusions. Firstly, for all single channel devices the target of the drive current cannot be achieved. Hence, a single channel NWT could not fulfil the scaling requirement for the 5nm CMOS technology. However, the drive current depends on the gate length, which is the second main point observed in Fig. 6. For example, for the device with $L_G = 12$nm the drive current can be higher than the target value if we consider two channel devices (neglecting S/D contact resistance). However, this is not the case for the devices with 20 nm gate length.

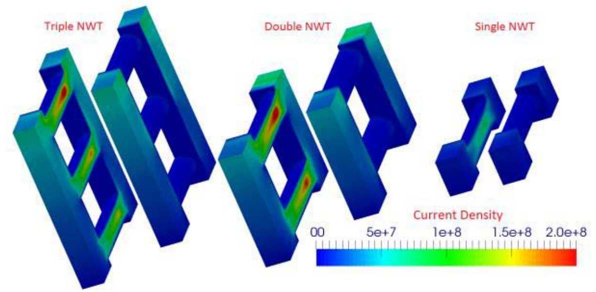

FIGURE 7. 3D view of the current density for NWTs with single, double, and triple channels with $L_G = 12$nm based on calibrated DD methods.

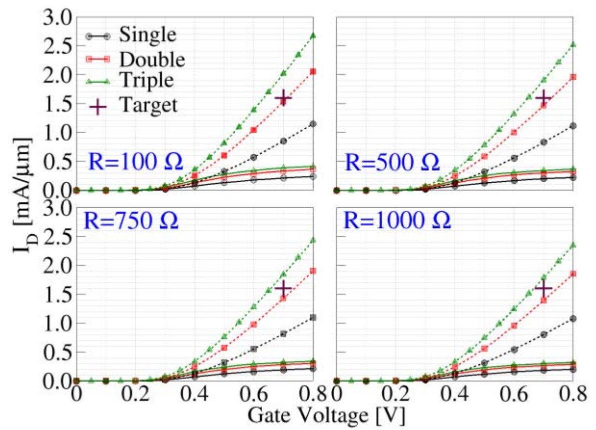

FIGURE 8. I_D-V_G characteristics for single, double and triple channel Si NWT at $L_G = 12$ nm considering four contact resistance values (R) based on calibrated DD methods without channel strain.

Therefore, we can conclude that a nanowire transistor with two lateral channels could achieve the required target performance, but only for a specific gate length and without considering contact resistance.

Fig. 6 shows clearly that all nanowires with three lateral channels have significantly higher values of the I_{sat} current in comparison to the target value at 5nm technology. Hence, using three stacked lateral channels in a single device could fulfil the scaling performance target for 5 nm CMOS.

Fig. 7 shows the 3D current density profile for the transistor with one, two, and three channels. From the figure, it is clear that the current density varies in each lateral channel. For example, in the triple NWTs, although the channels have the same cross-sectional area, the top channel, which is the closest to the metal, has more current density than middle and lower channels. Indicative of this is the magnitude of the size of the red region close to the drain. The intensity of this red region decreases when moving to the second and third channel. A similar picture is observed for the device with two channels. The current density in the top channel is higher than the current density in the bottom one. Hence, it can be concluded that the current density in each lateral channel decreases when increasing the distance between the contact and the channel.

In the simulations presented in Fig. 5, Fig. 6, and Fig. 7, the source/drain contact resistance (R) is not considered.

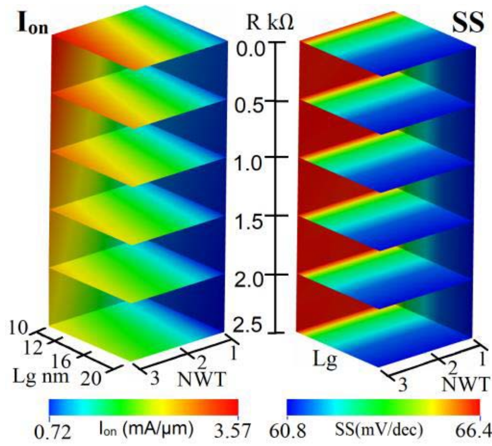

FIGURE 9. Design of experiment for stacked NWT and the effects of contact resistance values (R), gate length, and the number of stacked NWT on I_{sat}, and SS.

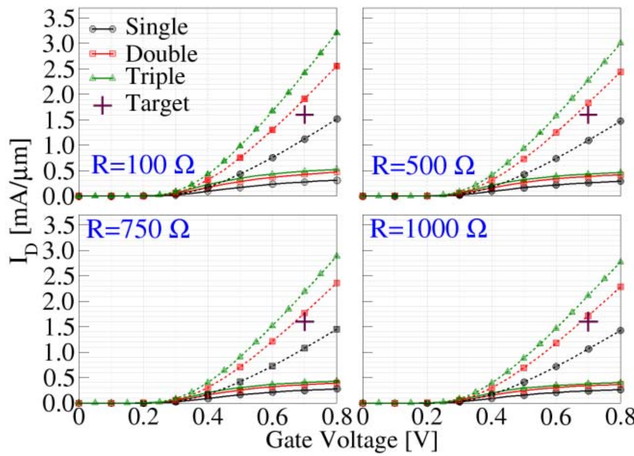

FIGURE 10. I_D-V_G characteristics for strained Si NWT with single, double, and triple channel Si NWT at L_G = 12 nm considering four contact resistance values (R) based on calibrated DD methods. All NWTs channels are strained by 2GPa.

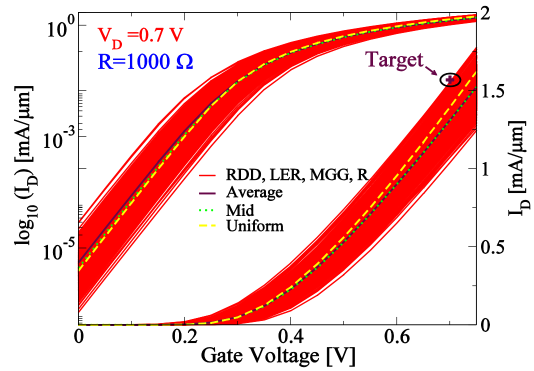

FIGURE 11. Linear transfer characteristics for the ensemble with RDD, LER, and MGG for double channel Si NWT at L_G = 12 nm considering four contact resistance values (R) based on calibrated DD methods.

For an even more realistic picture of the device performance, in Fig. 8 and Fig. 10 we consider four different values of R. In this case the resistance is introduced as lump resistance in the simulation (100 Ω, 500 Ω, 750Ω, and 1K Ω). The contact resistance applied to both contacts (source/drain) in such case the potential on the source and drain contacts will be uniformly modified to account for the voltage drop across the lumped resistance.

In Fig. 8 we present simulation results considering four different values of the contact resistance for devices without strain. As expected, the results presented in Fig. 8 show that the $_t$ current decreases when increasing the contact resistance, for instance at 1KΩ, I_{sat} is around 0.82, 1.49, 1.92 [mA/μm] for single, double, triple NWTs respectively at high (0.7V) drain bias. More importantly, for devices with two channels our simulation analysis shows a lower value of the I_{sat} current than the target value. Hence, the addition of contact resistance in the simulation illustrates that transistors with two channels cannot reach the required scaling criteria for 5nm CMOS applications. On the contrary, all transistors with triple channels show higher values in comparison with the target. Therefore, our simulations show that only three channel Si NWT has the potential to reach or offer better performance than the expected scaling target. Fig 9 presents a design of experiment for single, double and triple NWTs the gate lengths for each device are in range (10nm to 20nm), while the resistance range is from 500Ω to 2500Ω. It is clear that the number of lateral NWTs have no significant effect on the SS.

However, Fig. 10 presents the same devices in fig 8 but with applied 2GPa channel strain. In this case, our results show that for all values of R the double channel transistor surpasses the target value. Hence, the two-channel transistor may be sufficient to reach the industrial target.

Moreover, it is apparent from Fig. 5 that the strain can raise the drain current by 30% at 2.0 GPa for single NWT. However, as Fig. 10 shows, there is a significant degradation in the drive current in the vertically stacked NWT with two and three laterals channels. This is due to the voltage drop through current path across series resistance at S/D contacts and in highly doped S/D regions. For instance, the current drops by 24.6% and 26.5% for double NWT and triple NWT, respectively at 1KΩ.

VI. STATISTICAL VARIABILITY

Statistical variability (SV) is becoming important in nanoscale transistors [24]. Random Discrete Dopants (RDD), Line Edge Roughness (LER), and Metal Gate Granularity (MGG) remain the main sources of SV due to the inherited processes in doping and gate patterning. The simulation of different sources of SV using GARAND is described in more detail elsewhere [25]–[28].

In this section, we present results regarding the SV of the vertically stacked lateral NWT. The current-voltage transfer characteristic of an ensemble of 1000 atomistic devices with the main sources of SV (RDD, LER, and MGG) is shown in Fig. 11. Comparing the uniform device (yellow line) with

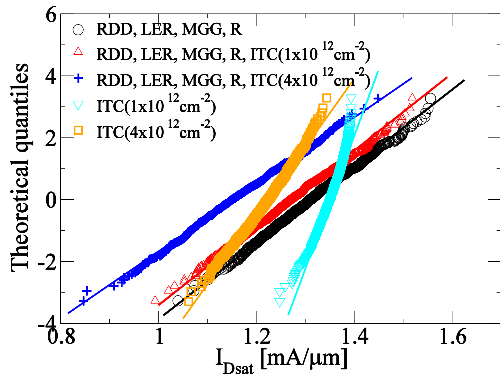

FIGURE 12. Normal probability QQ-plot of drain saturation distributions due to individual VS effect of (RDD, LER, MGG, and R), and in their combination with $1x10^{12}$ cm^{-1} and with $4x10^{12}$ cm^{-1} ITC.

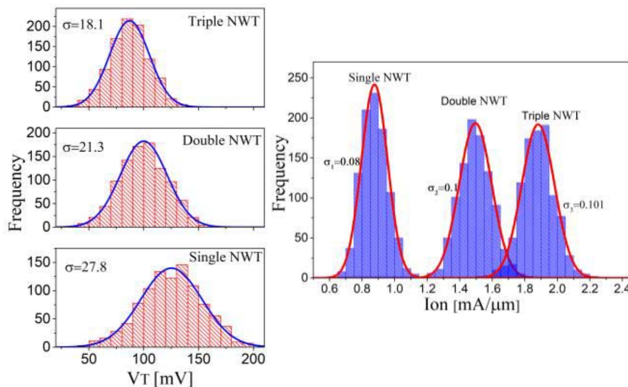

FIGURE 13. Threshold voltage V_T distributions and saturation current Ion distribution subject to combined SV (RDD, WER, and MGG) of single, double, and triple NWTs.

an average transistor (purple), the average I_{sat} is 15% less than the uniformly doped device.

Fig. 11 shows the drain current (at high drain bias I_{sat}) distribution for 1000 devices in five different scenarios. In all cases, R=1000 Ω. Firstly, there are three sources of SV and contact resistance without trap in the oxide. This is the data with black cycles on Fig. 11. The results with red and blue symbols correspond to considering 1000 devices with sources of variability with added interface trapped charges (ITC) with two levels of degradation $n=1x10^{12}$ and $n=4x10^{12}$ correspondingly. Finally, we examined two sets of 1000 devices with no sources of variability but considering the two levels of trap concentration mentioned above, and the impact of these two levels of ITC on the performance (I_{sat}) of 1000 device.

From the data presented in Fig. 12, the following conclusions can be drawn. Firstly, all devices which include sources of SV have a broader distribution of the drive current in comparison to the 'smooth' transistors. Moreover, for all devices which include SV, features have a distribution of I_{sat} values that follow the Gaussian line (solid line in the Fig. 12).

TABLE 2. Mean and standard deviations values of V_T and I_{ON} subject to combined SV (RDD, WER, and MGG) of single, double, and triple NWTs.

NWT		VT [mV]		I_{on} [mA/µm]	
		Mean	σV_T	Mean	σI_{on}
Single		125.2	27.87	0.876	0.080
Double		99.97	21.35	1.496	0.100
Triple		87.05	18.12	1.898	0.101

For the devices where we consider only traps in the oxide and no variability sources, the distribution is very similar in both cases with much narrower distribution in comparison to the previous three cases. Fig. 13 compares threshold voltage (V_T) distributions and saturation current (I_{on}) distribution of single, double, and tribble NWT (1000 device of each structure) subject to combined SV (RDD, WER, and MGG). The VT standard deviation of triple lateral stacked NWTs has a lower standard deviation (o') than the double stacked NWTs while the value of o'V_T for a single NWT shows the highest o' compared with double and triple NWTs. VT has been extracted at the same value of the OFF-current (I_{off}) for all simulated devices. What is interesting in this data is that the variation of o'V_T is decreasing with increasing the number of the lateral channels in the stack. The improvement in o'V_T in vertically stacked NWT can be explained by the fact that in the multiple stacked lateral channels NWTs, like triple channel NTWs for example, a considerable amount of the variability in lateral channels are cancelling each other. Further analysis of data revealed that σI_{on} of single NWT is less than σI_{on} of double NWTs by 0.02 while σI_{on} of double NWTs is close to σI_{on} of triple stacked NWTs as shown in fig. 13 and table 2.

VII. CONCLUSION

In this work, we simulated ultra-scaled NWTs with two methods: DD+PS and EMC. Based on those methods we established a link between channels strain and device performance. We also compared the current flow in single, double, and triple vertically stacked horizontal NWTs. Our results show that using multiple channel nanowire transistors could improve the device performance, and especially the drive current, significantly. More importantly, our simulations show that a single nanowire transistor even with strained Si channel will not be able to provide the required drive current in comparison to the industrial target at 5nm node. However, devices with two and three vertically stacked channels have the potential to reach the industrial target.

In addition, we presented the interplay between device performance and various sources of SV, which was compared to different levels of trapped charges. Our results suggest that the BTI degradation has a negative impact on important figures of merit in multi-channel NWTs.

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