Received 10 August 2017; revised 5 September 2017; accepted 6 September 2017. Date of publication 11 September 2017; date of current version 24 October 2017. The review of this paper was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2017.2751065

Demonstration of GaN Static Induction Transistor (SIT) Using Self-Aligned Process

WENWEN LI[1], DONG JI[1], RYO TANAKA[2], SAPTARSHI MANDAL[1] (Student Member, IEEE), MATTHEW LAURENT[1], AND SRABANTI CHOWDHURY[1] (Senior Member, IEEE)

1 Department of Electrical and Computer Engineering, University of California, Davis, CA 95616, USA
2 Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106-9560, USA

CORRESPONDING AUTHOR: W. LI (e-mail: wweli@ucdavis.edu)

This work was supported in part by DARPA-YFA program under Grant D15AP00992 and in part by ARPA-E SWITCHES program.

ABSTRACT The rapid development of RF power electronics requires amplifier operating at high frequency with high output power. GaN-based HEMTs as RF devices have made continuous progress in the last two decades showing great potential for working up to G band range. However, vertical structure is preferred to obtain higher output power. In this paper, we have designed and fabricated GaN static induction transistor using the self-aligned technology, which was accomplished mainly by using a SiO_2 lift-off step in buffered oxide etch (BOE). By optimizing the time in ultrasonic bath and in BOE, the SiO_2 and the metal on top were removed completely which resulted in the gate metal only on the sidewalls. Both dry and wet etch techniques were investigated to reduce the gate leakage on the etched surface. The low power dry etch combined with the tetramethylammonium hydroxide wet etch can effectively reduce the etch damages, decrease the gate leakage and enhance the gate control over the channel.

INDEX TERMS Gallium nitride, static induction transistors, high power, self-aligned, etch.

I. INTRODUCTION

The development of high power amplifiers is driven by the growing demand of advanced wireless communication, satellite broadcasting, marine and space-based radar systems. Gallium nitride's (GaN's) high breakdown electric field, high electron mobility and high electron saturation velocity allow improved performance in the RF range. AlGaN/GaN HEMTs using very high mobility 2DEG channel have been investigated extensively in the last two decades. They demonstrated very promising features suitable for RF applications [1], [2]. Highly scaled T-Gate technology offers HEMTs very high f_T and f_{max} which shows the capability of working from L to G band range [3]–[6]. High RF power is another important criterion for power amplifiers which enables higher data rates and longer range for communication applications. To obtain higher power, many transistor unit cells must be combined in parallel to increase the current, which results in a large surface area. Vertical geometry is preferred to increase the power since only two electrodes are needed on the surface, thus eliminating source air-bridging, the unit cell size can be much smaller compared to lateral structure. Moreover, the electron trapping near the gate and high gate leakage caused by high electric fields on the surface of HEMTs lead to lower output power and efficiency [7], [8]. Proper field plating with high quality dielectric (low D_{it}) layers are employed to reduce dispersion in lateral HEMTs [9]–[11]. In vertical structures, the high electric fields are below the surface of the semiconductor, which maintain the output current during the high frequency operation [12]. In recent years, the availability of thick and high quality GaN free-standing substrates is attracting more research efforts [13]–[16].

The concept of Static induction transistor (SIT) was introduced by Nishizawa and in 1975, experimental SITs were fabricated and the drain current of this device was shown to follow the predicted space-charge injection mode [17]. A typical recessed gate SIT structure with bottom and sidewall contacts was shown in Fig. 1. SIT is a class of short-channel Field Effect Transistors. The current is flowing vertically between the source and the drain and is controlled by electrostatic potential barrier induced by the two opposite gates on the sidewalls. Thus, SIT shows a triode-like unsaturated output characteristics. SiC SITs

2168-6734 © 2017 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

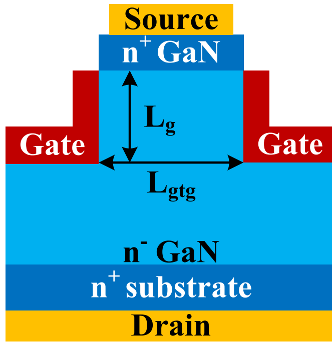


FIGURE 1. Cross-sectional view of GaN recessed gate SIT with bottom and sidewall gate Schottky contacts.

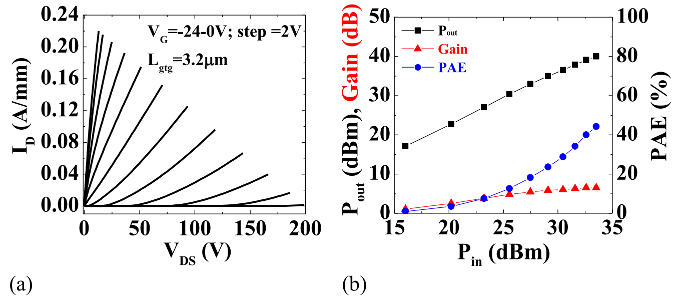


FIGURE 2. Simulated (a) DC output characteristics and (b) RF power performance of the SIT for Lg = 2μm and Lgtg = 3.2μm with drift layer thickness of 3μm.

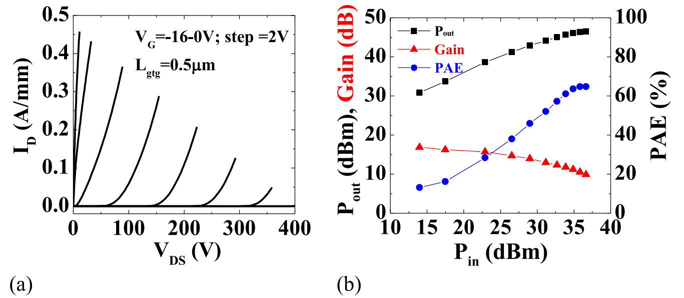


FIGURE 3. Simulated (a) DC output characteristics and (b) RF power performance of the SIT for Lg = 0.7μm and Lgtg = 0.5μm with drift layer thickness of 3μm.

have shown the potential for high power and high frequency applications [18]–[20]. With higher electron mobility and higher saturation velocity than SiC, GaN SITs have the potential to operate at higher frequency with higher output power [21]. In this work, we successfully designed and fabricated the GaN SIT using self-aligned process.

II. DEVICE SIMULATION AND FABRICATION

A device-circuit-integrated model was built in Silvaco's Mixed Mode platform to accurately evaluate the device performance in a power amplifier based on physics modeling. The details of the model was reported recently by Ji *et al.* [22]. A 2D device simulation was performed in Silvaco ATLAS using drift-diffusion model. Impact ionization was not taken into consideration in the modeling due lack of unanimously accepted parameters. Instead, we set a leakage current criteria as 1μA/mm and defined the breakdown voltage when the leakage current reaches 1μA/mm. The simulated device has the gate length (L_g) of 2μm, gate to gate distance (L_{gtg}) of 3.2μm and drift layer thickness of 3μm, which had the same dimensions as our fabricated device. It is critical to note that a typical triode-like output characteristics is offered in a SIT (see Fig. 2 (a)). Next, we have built the circuit for class B amplifier based on the 2D device simulator. Both small signal and large signal performance were simulated. The simulated device shows an f_T of 5.6GHz. 10W/mm of output power density was achieved at V_{DS} = 180V at 2GHz. By further shrinking the feature size to L_g = 0.7μm and L_{gtg} = 0.5μm, with 3μm of drift layer thickness, the simulated device demonstrated f_T of 16GHz and output power density of 44.7W/mm at V_{DS} = 300V, showing great potential for high power RF application (Fig. 3).

Our first-generation devices were grown by metalorganic chemical vapor deposition (MOCVD) on sapphire substrates. The epitaxial growth began with 1μm n^+ layer followed by 5μm drift layer with the doping of $5\times10^{15}/cm^3$. Next, 400nm of n^+ layer was grown on top to form the source ohmic contact. The process flow to realize a SIT is shown in Fig. 4. First, an inductively coupled plasma (ICP) etch was used to remove the n^+ layer everywhere except the region to form the source contact in the final device. 1.3μm of plasma-enhanced chemical vapor deposition (PECVD) SiO_2 was then deposited followed by 150nm Ni layer which acted as a hard mask to pattern the SiO_2. The SiO_2 was etched using fluorine-based reactive ion etching (RIE) at 200W power. After completely removing the Ni film using Ni etchant, 2μm GaN was etched using a combination of ICP dry etch and tetramethylammonium hydroxide (TMAH) wet etch to achieve smooth and vertical sidewalls. Ni/Au/Ni (30nm/400nm/20nm) were then deposited as the gate metal using E-beam evaporation in planetary rotation system. We used a SiO_2 lift-off technique in buffered oxide etch (BOE) to remove the SiO_2 and gate metal on top of the pillar and leave the gate metal just on the sidewalls, which will realize this self-aligned process. The details of the lift-off process are discussed under Section III. Source contact was formed on top of the n^+ region. Finally, a large drain contact (~30mm^2) was defined on the drift region away from the device-containing area, which can be regarded as an ohmic contact.

III. SELF-ALIGNED PROCESS

The critical step to achieve this self-aligned process is the SiO_2 lift-off technique in BOE (Fig. 5). Short loop experiments were carried out to optimize this process. Three methods were tried. The first method involved a simple dip of the sample in BOE for 40min. As shown in Fig. 6 (a), most of the metal on top of the mesa was removed; however, some residual metal was still on the edge of the pillar, which

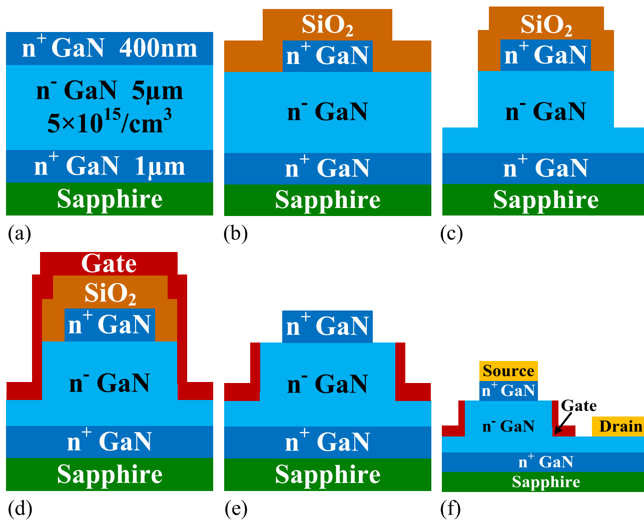


FIGURE 4. Process flow for GaN SIT (a) As-grown structure. (b) 1.3μm PECVD SiO_2 deposition after n^+ layer etch. (c) Deep GaN etch using SiO_2 as the hard mask. (d) Gate metal deposition using Ni/Au/Ni. (e) SiO_2 lift-off process in BOE. (f) Complete SIT structure with source contact on top and big drain contact on the drift region.

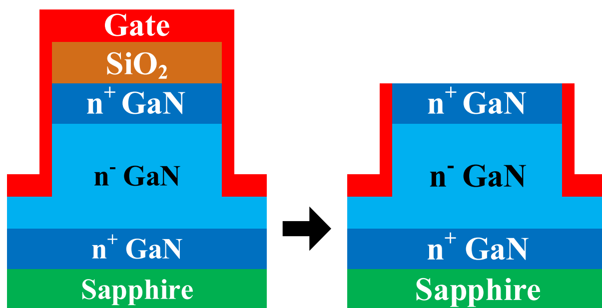


FIGURE 5. Schematic short-loop self-aligned process flow using SiO_2 lift-off in BOE.

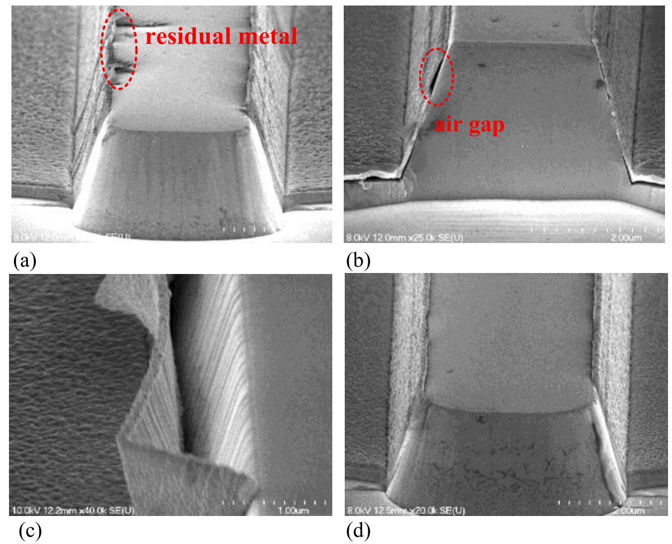


FIGURE 6. SEM images using different methods for SiO_2 lift-off: (a) Dipped in BOE for 40min. (b) Ultrasonic bath in BOE for 30min. (c) Pipette assisted method. (d) Combination of 25min dip and 5min ultrasonic bath in BOE.

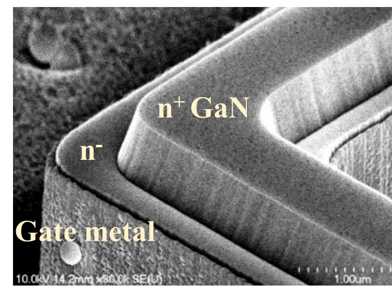


FIGURE 7. SEM image after the SiO_2 lift-off process of the full device.

caused shorts between the source and the gate in the transistor. The second method relied on the usage of ultrasonic vibrations during the lift-off. Fig. 6 (b) shows the SEM image after 30min of ultrasonic bath. The metal was completely removed and no residual metal was observed on the mesa. However, air gaps were found on the sidewalls between the metal and GaN, which would compromise the gate modulation of the channel in the full device. The third method utilized a mechanical method of carefully pipetting the solvent to flow on the wafer surface. The force generated by the solvent lifted off the SiO_2 and the metal. The metal was removed completely and the edges of the mesa were clean. However, it was observed that the lift-off process was sensitive to the direction of solvent flow. Pipetting the solvent parallel to the channel region resulted in complete removal of metal on the mesa without removing any metal on the sidewalls; however, when pipetted perpendicular to the channel region, it showed tendencies to peel off the metal from the sidewalls as shown in Fig. 6 (c). An optimized method, which is a highlight of this paper, was therefore developed to accomplish the lift-off process. A combination of 25min dip to take away the majority of the metal with 5min ultrasonic bath to remove the residual metal offered the most promising and reproducible result. The edges of the metal were very clean and precise with no air gaps appearing between the metal and the sidewalls (Fig. 6 (d)). We employed this optimized lift-off process in the fabrication of the full transistor. After the lift-off process, as shown in Fig. 7, the gate metal deposited on the sidewalls was evidently separated from the n^+ region.

IV. ETCH TECHNIQUES TO IMPROVE DEVICE PERFORMANCE

Since the channel of the SIT is defined by the deep GaN etch, a smooth and low damage etch is required to achieve low gate leakage and better pinch-off. The trench was first formed by ICP-based dry etching with a Cl_2/BCl_3 gas combination at 400W of ICP power and 70W of bias power. The ICP etch was optimized to result in a fairly smooth but slant sidewall with an angle of 15° to the direction orthogonal to the surface as shown in Fig. 8 (b). Wet etch using TMAH solution was used after the dry etch to further remove the roughness of the sidewalls. TMAH solution is widely used

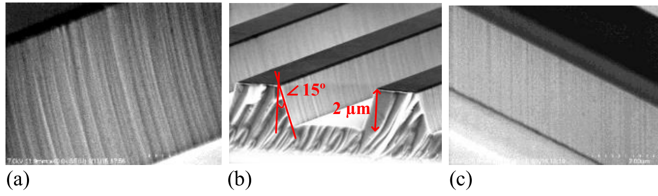


FIGURE 8. SEM image of the sidewall profile (a) after the ICP dry etch, (b) angle of etch, (c) after the TMAH post-treatment.

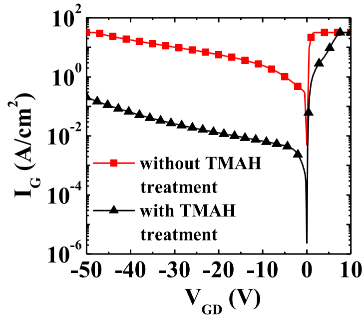


FIGURE 9. Influence of TMAH post-treatment on I-V characteristics of the Schottky diodes fabricated on the etched surfaces.

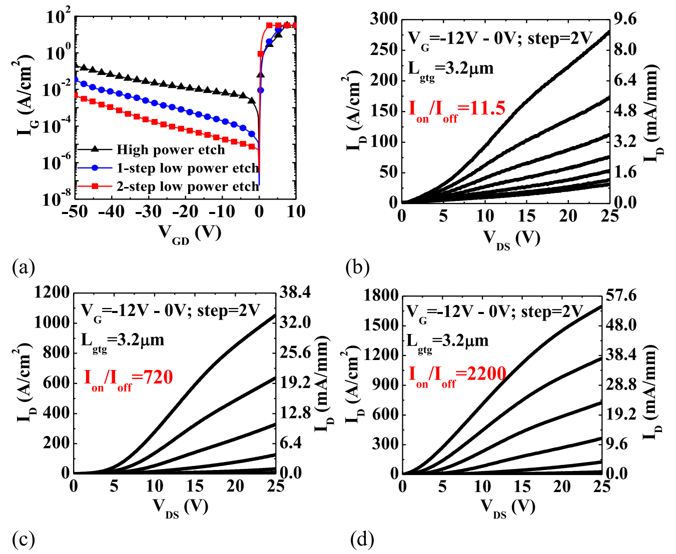


FIGURE 10. Influence of different etch power on the behavior of the devices. (a) I-V characteristics of the Schottky diodes fabricated on the etched surfaces. Output I-V characteristics of SIT using (b) high power ICP etch, (c) one-step low power etch, and (d) two-step low power etch.

as an anisotropic etchant for GaN. TMAH etches m-plane at a significantly slower rate compared to other semi-polar planes of the wurzite GaN crystal [23]. The wet etching was performed at 85°C for 1h in TMAH with the concentration of 25%. The SEM pictures Fig. 8 (c) showed a remarkable improvement in the sidewall profile after the TMAH treatment. Another important role of TMAH was to remove the plasma-induced damages on the etched surfaces. Fig. 9 shows the I-V characteristics of the Schottky diodes (200μm diameter) fabricated on the etched planar surfaces with and without the TMAH post-treatment. With the TMAH treatment, the reverse leakage current was reduced by more than two orders of magnitude.

An important factor to achieve low damage etch is the combination of low ICP power and low bias power at which the sample is etched. Three samples were subjected to different powers to study the effect on leakage. Sample A was the 400/70W high power (etch rate∼200nm/min) etched sample. Sample B was etched at 100W ICP power and 30W bias power (etch rate∼60nm/min) to define a 2μm deep etch in a single step. Sample C was subjected to a two-step etch: 100W ICP power and 30W bias power was used for etching the first 1.8μm and 100W ICP power and 20W bias power (etch rate∼15nm/min) was used to etch the rest 200nm. After the dry etch, all three samples went through an identical TMAH treatment. Schottky diodes were fabricated on the etched surfaces. The leakage current in sample C was nearly two orders of magnitude lower than in sample A (Fig. 10 (a)) due to lower plasma induced damages on the surface.

Transistors were fabricated using the three-different etching power to define the gate area. The output characteristics are shown in Fig. 10. I_D-V_{DS} characteristics of the SIT using two-step low power etch showed almost 6 times higher output current than using the high power etch and the I_{on} to I_{off} ratio (at $V_{DS} = 25V$) is 200 times higher. The increase of the output current is considered as a result of an increase in the mobility in the vicinity of the sidewall region, due to a reduction in etch-related damages. Plasma etch will create a damaged layer with significant thickness from the surface [24] and the mobility in that damaged area is much lower. At higher power, the penetration of the damaged region is increased. As the electrons are flowing in the entire region between the two gates, with higher etch power, lower output current was generated. This demonstrates that low-damage etch process is critical for channel definition, and yields significant advantages for transistor operation in both on- and off-states.

V. CONCLUSION

We have successfully fabricated self-aligned GaN-based SITs. This self-aligned process was achieved using SiO_2 lift-off procedure in BOE. The role of TMAH etch on the sidewalls was investigated as a function of gate to drain leakage. The positive impact of low power etch was established through 2-terminal and 3-terminal device characteristics. Clearly with lower etch power, both on- and off-state behaviors were improved resulting in a drop of the leakage current by nearly 2 orders of magnitude and output current increasing by 6 times.

ACKNOWLEDGEMENT

The authors would like to acknowledge Dr. Anant Agarwal for helpful discussion. They would also like to acknowledge the Center for Solid State Electronics Research at Arizona State University for their support.

REFERENCES

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008, doi: 10.1109/JPROC.2007.911060.

[2] D. W. Runton, B. Trabert, J. B. Shealy, and R. Vetury, "History of GaN: High-power RF Gallium Nitride (GaN) from infancy to manufacturable process and beyond," *IEEE Microw. Mag.*, vol. 4, no. 3, pp. 82–93, May 2013, doi: 10.1109/MMM.2013.2240853.

[3] M. Higashiwaki, T. Mimura, and T. Matsui, "30-nm-gate AlGaN/GaN heterostructure field-effect transistors with a current-gain cutoff frequency of 181 GHz," *Jpn. J. Appl. Phys.*, vol. 45, nos. 42–45, pp. L1111–L1113, Oct. 2006, doi: 10.1143/JJAP.45.L1111.

[4] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT with 300-GHz f_{max}," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 195–197, Mar. 2010, doi: 10.1109/LED.2009.2038935.

[5] S. Huang *et al.*, "High-f_{MAX} high Johnson's figure-of-merit 0.2-μm gate AlGaN/GaN HEMTs on silicon substrate with AlN/SiN_x passivation," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 315–317, Mar. 2014, doi: 10.1109/LED.2013.2296354.

[6] A. Margomenos *et al.*, "GaN technology for E, W and G-band applications," in *Proc. Compound Semicond. Integr. Circuit Symp. (CSICs)*, La Jolla, CA, USA, Oct. 2014, pp. 1–4, doi: 10.1109/CSICS.2014.6978559.

[7] A. Tarakji *et al.*, "Mechanism of radio-frequency current collapse in GaN-AlGaN field-effect transistors," *Appl. Phys. Lett.*, vol. 78, no. 15, pp. 2169–2171, Apr. 2001, doi: 10.1063/1.1363694.

[8] C. Roff *et al.*, "Analysis of DC–RF dispersion in AlGaN/GaN HFETs using RF waveform engineering," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 13–19, Jan. 2009, doi: 10.1109/TED.2008.2008674.

[9] Y. Ando *et al.*, "10-W/mm AlGaN-GaN HFET with a field modulating plate," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 289–291, May 2003, doi: 10.1109/LED.2003.812532.

[10] S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. J. Chen, "Effective passivation of AlGaN/GaN HEMTs by ALD-grown AlN thin film," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 516–518, Apr. 2012, doi: 10.1109/LED.2012.2185921.

[11] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, "Current collapse suppression by gate field-plate in AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1379–1381, Nov. 2013, doi: 10.1109/LED.2013.2280712.

[12] S. Mandal *et al.*, "Dispersion free 450-V p GaN-Gated CAVETs with Mg-ion implanted blocking layer," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 933–936, Jul. 2017, doi: 10.1109/LED.2017.2709940.

[13] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, "CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 41–43, Jan. 2012, doi: 10.1109/LED.2011.2173456.

[14] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Appl. Phys. Exp.*, vol. 7, no. 2, 2014, Art. no. 021002, doi: 10.7567/APEX.7.021002.

[15] D. Ji and S. Chowdhury, "Design of 1.2 kV power switches with low R_{on} using GaN-based vertical JFET," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2571–2578, Aug. 2015, doi: 10.1109/TED.2015.2446954.

[16] W. Li and S. Chowdhury, "Design and fabrication of a 1.2 kV GaN-based MOS vertical transistor for single chip normally off operation," *Phys. Status Solidi A*, vol. 213, no. 10, pp. 2714–2720, Oct. 2016, doi: 10.1002/pssa.201532575.

[17] J. Nishizawa, T. Terasaki, and J. Shibata, "Field-Effect transistor versus analog transistor (static induction transistor)," *IEEE Trans. Electron Devices*, vol. ED-22, no. 4, pp. 185–197, Apr. 1975, doi: 10.1109/T-ED.1975.18103.

[18] R. R. Siergiej *et al.*, "High power 4H-SiC static induction transistors," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 1995, pp. 353–356, doi: 10.1109/IEDM.1995.499213.

[19] R. C. Clarke, A. K. Agarwal, R. R. Siergiej, C. D. Brandt, and A. W. Morse, "The mixed mode 4H-SiC SIT as an S-band microwave power transistor," in *Proc. IEEE Device Res. Conf.*, Santa Barbara, CA, USA, Jun. 1996, pp. 62–63, doi: 10.1109/DRC.1996.546316.

[20] Y. M. Sung, J. B. Casady, J. B. Dufrene, and A. K. Agarwalet, "A review of SiC static induction transistor development for high-frequency power amplifiers," *Solid State Electron.*, vol. 46, no. 5, pp. 605–613, May 2002, doi: 10.1016/s0038-1101(01)00312-4.

[21] G. E. Bunea, S. T. Dunham, and T. D. Moustakas, "Modeling of a GaN based Static induction transistor," *MRS Internet J. Nitride Semicond.*, vol. 4S1, no. G6.41, Feb. 1999, doi: 10.1557/PROC-537-G6.41.

[22] D. Ji, Y. Yue, J. Gao, and S. Chowdhury, "Dynamic modeling and power loss analysis of high-frequency power switches based on GaN CAVET," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4011–4017, Oct. 2016, doi: 10.1109/TED.2016.2601559.

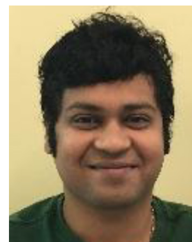
[23] M. Kodama *et al.*, "GaN-based trench gate metal oxide semiconductor field-effect transistor fabricated with novel wet etching," *Appl. Phys. Exp.*, vol. 1, no. 2, pp. 1–3, Feb. 2008, doi: 10.1143/APEX.1.021104.

[24] W. Nakamura, Y. Tokuda, H. Ueda, and T. Kachi, "Inductively coupled plasma-induced defects in n-type GaN studied from Schottky diode characteristics," *Phys. B. Condens. Matter*, vols. 376–377, pp. 516–519, Apr. 2006, doi: 10.1016/j.physb.2005.12.131.

WENWEN LI received the B.S. degree in integrated circuits design and integration systems and the M.S. degree in microelectronics and solid state electronics from Xidian University, Xi'an, China, in 2010 and 2013, respectively. She is currently pursuing the Ph.D. degree with the Electrical and Computer Engineering Department, University of California, Davis, CA, USA, working with Prof. S. Chowdhury.

DONG JI received the B.S. degree in optical information of science and technology from Beijing Jiaotong University, Beijing, China, in 2013 and the M.S. degree in electrical engineering from Arizona State University, Tempe, USA, in 2014. He is currently pursuing the Ph.D. degree with the Electrical and Computer Engineering Department, University of California, Davis, CA, USA, working with Prof. S. Chowdhury.

RYO TANAKA received the B.Tech. degree in physical science and engineering and the M.S. degree in crystalline materials science from Nagoya University, Aichi, Japan, in 2007 and 2009, respectively. Since 2009, he has been with Fuji Electric Company, Ltd., Tokyo, Japan. From 2014 to 2016, he was a Visiting Research Scholar with the University of California, Santa Barbara.



SAPTARSHI MANDAL (S'13) received the B.S. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, and the M.S. degree in electrical engineering from the University of Toledo, OH, USA, in 2013. He is currently pursuing the Ph.D. degree in electrical engineering with the University of California, Davis, CA, USA. His current research interests include design, fabrication, and characterization of gallium nitride vertical devices for high power and RF electronics.

MATTHEW LAURENT received the B.S. degree in applied physics from Rensselaer Polytechnic Institute in 2009 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 2011 and 2016, respectively. He is currently a Post-Doctoral Scholar with the University of California, Davis. His current research interests include MOCVD growth and electrical characterization of group III-N semiconductor materials and heterojunctions, and their application to high-power electronic devices.

SRABANTI CHOWDHURY (S'08–M'11–SM'17) received the B.Tech. degree in radiophysics and electronics from the University of Calcutta, India, in 2003 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 2008 and 2010, respectively. She was with Transphorm Inc., as a Technical Staff Member from 2010 to 2013. In 2013, she joined the faculty of ECEE Department, Arizona State University, Tempe, AZ, USA, as an Assistant Professor.

She is currently an Associate Professor with the ECE Department, University of California, Davis, CA, USA.