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A Simple Model for the Thermal Noise of Saturated MOSFETs at All Inversion Levels

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ABSTRACT We propose a single formula for the channel thermal noise of saturated long-channel MOSFETs operating in weak, moderate, and strong inversion. Our approach is based on a novel interpolation of well-known analytical formulas known to be valid in weak and strong inversion, and the result is both accurate and simple enough to be useful for hand calculations. We expect the formula to be particularly useful for designing energy-efficient analog circuits biased in moderate inversion. We have validated it using noise measurements of nMOS and pMOS transistors in a 0.5-μm CMOS process.

INDEX TERMS Thermal noise, MOSFETs, moderate inversion.

I. INTRODUCTION

This paper proposes a simple model for the channel thermal noise of saturated long-channel MOSFETs that is suitable for analog circuit design and valid at all inversion levels. We begin by considering a common charge-based model for the power spectrum density (PSD) of thermal noise present in MOSFET drain current, which is given by

$$\overline{\Delta I_{ds}^2} = \frac{2q\,|Q_{tot}|}{\tau_d} = \frac{4kT\mu_{eff}\,|Q_{tot}|}{L^2}, \tag{1}$$

where $\tau_d = L^2/2D$ is the mean diffusion time of carriers through the channel, Q_{tot} is the total channel charge, μ_{eff} is the effective carrier mobility, and the second expression was derived by assuming the Einstein relationship $(D/\mu_{eff}) = (kT/q)$ [1]–[3]. This formula was first proposed back in 1966, and remains the basis for channel thermal noise modeling in industry-standard compact MOSFET models such as BSIM4 and Enz-Krummenacher-Vittoz (EKV). However, it has been modified to account for additional noise mechanisms found within deeply-scaled devices.[1]

While eqn. (1) is valid in all regions of transistor operation, there is no simple analytical expression relating Q_{tot} to the terminal voltages or drain current in the moderate inversion region, i.e., when V_{GS} is approximately equal to the threshold voltage of the device [4], [5]. As a result, the formula is not suitable for hand calculations while designing circuits that operate in this region. This is unfortunate, since moderate inversion provides the optimum trade-off between gain, linearity, bandwidth, noise, and DC mismatch for many low-power applications [6]–[8].

Several analytical MOSFET thermal noise models valid in all regions of operation have been proposed to address this issue [9]–[15] (also see [16] for a recent review). While suitable for implementation in circuit simulators, these models are too complex for hand calculations. However, the modeling challenge can be simplified by realizing that analog designs generally i) bias MOSFETs in saturation, i.e., ensure that V_{DS} is greater than the saturation voltage V_{DSAT}; and ii) use relatively long channel lengths to minimize short-channel effects such as increased output conductance g_{ds}. A simple analytical formula for predicting the noise of saturated long-channel devices at all inversion levels would therefore be very useful for analog circuit design, and is the focus of this paper.

1. Details are available at bsim.berkeley.edu and ekv.epfl.ch, respectively.

II. NOISE MODELING

A. PROPOSED MODEL

It is useful to recall that the physical basis of eqn. (1) is the assumption that the drift velocity of charge carriers within the channel is much smaller than their thermal velocity. Under these conditions, the diffusive random processes that cause shot noise are largely unaffected by electric fields within the channel. As a result, drift currents add no variability to the charge transport and are effectively noiseless. Consider a saturated MOSFET with an average drain current I_{DSAT}. In the subthreshold region all charge transport occurs due to diffusion, so the current noise PSD is given by the well-known shot noise result $2qI_{DSAT}$. On the other hand, in the above threshold region most charge transport occurs due to drift, so the noise PSD is significantly lower than $2qI_{DSAT}$. In fact, it can be found from eqn. (1) by using the well-known result $|Q_{tot}| = (2/3)WLC_{ox}(V_{GS} - V_{TS})$, where V_{TS} is the threshold voltage assuming a source-referenced model. Neither of these simple formulas is valid in the moderate inversion region, but progress can be made by interpolating between them. For example, the following interpolation formula [3, eq. (7.43)] has been proposed as a simple way to model thermal noise in moderate inversion:

$$\overline{\Delta I_{ds}^2} = \frac{2qI_{DSAT}}{\left(1 + \frac{3x}{4}\right)}, \tag{2}$$

where $x \equiv \kappa_s(V_{GS} - V_{TS})/(2\phi_t)$ is the normalized gate overdrive voltage, κ_s is the subthreshold slope constant, and $\phi_t = kT/q$ is the thermal voltage. Interestingly, the quantity $A \equiv 3x/4$ in the denominator is equal to the ratio of the diffusion and drift transit times through the channel; these are given by $L^2/2D$ and $L^2/[(3/4)\kappa_s\mu_{eff}(V_{GS} - V_{TS})]$, respectively [3]. Hence A is a measure of how much stronger noiseless drift currents are compared to noisy diffusion currents. It can also be viewed as the loop gain of electrostatic negative feedback (charge smoothing) on carrier density fluctuations within the channel [2], [3]; a similar effect occurs in vacuum tubes [17], [18]. The result is to reduce the noise PSD by a factor of $1/(1+A)$ compared to the full shot noise value of $2qI_{DSAT}$. However, eqn. (2) is only valid for $x > 0$, i.e., does not correctly asymptote to $2qI_{DSAT}$ in the subthreshold region where current flow is known to be purely diffusive and electrostatic feedback non-existent. Moreover, it has not been experimentally verified.

In order to extend the range of validity of eqn. (2), we refer to the well-known EKV MOSFET model, which is notable in using unified formulas that cover the entire operating range of the device [19], [20]. In particular, we consider a source-referenced version of the EKV model for convenience. This model [3, eq. (4.48)] uses the following interpolation formula to estimate the large signal I_{DS}-V_{DS} curve over the entire operating range:

$$I_{DS} = I_0\left(\underbrace{\left[\ln\left(1 + e^{x}\right)\right]^2}_{i_f} - \underbrace{\left[\ln\left(1 + e^{x-y}\right)\right]^2}_{i_r}\right), \tag{3}$$

where $I_0 \equiv (2\mu C_{ox}\phi_t^2/\kappa_s) \times (W/L)$ is known as the specific current and $y \equiv V_{DS}/(2\phi_t)$ is the normalized drain-source voltage. The two terms inside the parentheses are the forward and reverse channel currents (i_f and i_r, respectively). The drain current saturates when $i_r \to 0$, resulting in $I_{DSAT} = I_0 i_f$. As a result, $I_{DSAT} \approx I_0 e^{2x}$ in subthreshold ($x \ll 0$) and $\approx I_0 x^2$ above threshold ($x \gg 0$).

We combine features of eqns. (2) and (3) to propose the following novel interpolation formula for the PSD of drain current noise in saturation:

$$\overline{\Delta I_{ds}^2} = \frac{2qI_{DSAT}}{1 + \ln\left(1 + \exp\left(\frac{3x}{4}\right)\right)}. \tag{4}$$

It is easy to see that this equation has the right limiting behavior and is thus potentially valid over the device's entire operating range. In weak inversion ($x \ll 0$) the exponential term in the denominator goes to zero, so $\overline{\Delta I_{ds}^2} = 2qI_{DSAT}$, i.e., full shot noise. In strong inversion ($x \gg 0$) the exponential term is $\gg 1$, so $\ln(1 + \exp(3x/4)) \approx 3x/4$, resulting in the well-known formula $\overline{\Delta I_{ds}^2} = 4kT\gamma g_{ds0}$ where $\gamma = 2/3$, $g_{ds0} = g_{msat}/\kappa_s = I_{DSAT}/V_L$, and $V_L = (V_{GS} - V_{TS})/2$. Also g_{ds0} is the channel conductance at zero bias ($V_{DS} = 0$), g_{msat} is the transconductance in saturation, and $V_L = I_{DSAT}/g_{msat}$ is the effective linear range of the device.

It is interesting to note that since the denominator of eqn. (4) has the form $1 + \ln(1 + \exp(3x/4))$, it can also be viewed as the result of electrostatic negative feedback with a loop gain of $A \equiv \ln(1 + \exp(3x/4))$. Moreover, the equation only uses measurable large-signal voltages and parameters, making it suitable for circuit design.

B. COMPARISON TO THE EKV MODEL

It is interesting to compare the proposed formula with the EKV model. The drain current noise expression used in the original EKV paper can be written as [19]:

$$\overline{\Delta I_{ds}^2} = \frac{2qI_{DSAT}}{\sqrt{i_f + \frac{1}{2}\sqrt{i_f} + 1}}\left[\frac{\left(1 + \eta^2\right) + \frac{4}{3}i_f\left(\frac{1+\eta+\eta^2}{1+\eta}\right)}{\left(1 + i_f\right)}\right], \tag{5}$$

where $\eta \equiv \sqrt{i_r/i_f}$ is a measure of saturation, and decreases from 1 to 0 as we go from the linear to the saturation region. It is easy to verify that this formula has the right limiting behavior in both weak and strong inversion. Here we focus on the saturation region ($\eta \to 0$) for any inversion level, for which eqn. (5) simplifies to

$$\overline{\Delta I_{ds}^2} = \frac{2qI_{DSAT}}{\sqrt{i_f + \frac{1}{2}\sqrt{i_f} + 1}}\left(\frac{1 + \frac{4}{3}i_f}{1 + i_f}\right). \tag{6}$$

Eqns. (4) and (6) have the same asymptotic limits in weak inversion (where $i_f \to 0$) and strong inversion (where $i_f \to x^2$), but differ significantly when x is close to 0, i.e., in moderate inversion. In fact, the difference between the two equations has its largest value of 41.5% at a normalized overdrive voltage of $x = 1.26$. This difference can be significantly reduced by using $V_{TS'} \equiv V_{TS} + 2\phi_t$ in eqn. (4). Specifically, this small modification, which accounts for the slightly different definitions of threshold voltage in weak and strong inversion [21], reduces the maximum difference between the two equations to 20.8% at $x = 0.84$, i.e., by approximately a factor of 2. The resulting noise levels (normalized to $2qI_{DSAT}$) predicted by both models versus x are shown in Fig. 1. The two differ significantly when $|x| < 5$, i.e., in moderate inversion.

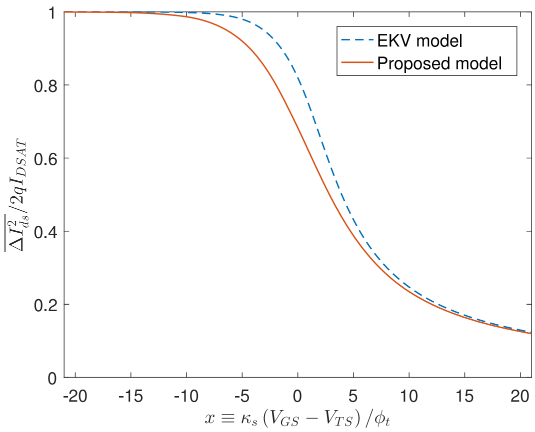

FIGURE 1. Normalized drain current noise in saturation predicted by i) the EKV model, and ii) the proposed model.

C. POSSIBLE EXTENSIONS

The proposed model assumes that drift velocities are small, such that i) the carrier mobility is equal to its low-field value, and ii) drift currents are noiseless. This is not valid for short-channel MOSFETs operating above threshold: the high lateral and vertical electric fields present in these devices lead to velocity saturation, vertical mobility reduction, carrier heating, and channel-length modulation [3]. As a result, the carrier temperature and effective mobility vary as a function of position in the channel, and the measured thermal noise exceeds that predicted by eqns. (1) and (4). The proposed formula can be *qualitatively* generalized to account for such excess thermal noise mechanisms. Specifically, the 3/4 term in the denominator of eqn. (4) can be replaced by $1/(2\gamma)$, where $\gamma > 2/3$ is the effective noise factor of the device. However, no simple formula for predicting the actual value of γ is known (the ones used by BSIM4 and EKV are quite complex), and deriving one is beyond the scope of this paper.

III. EXPERIMENTAL SETUP

One NMOS and one PMOS transistor were fabricated in the OnSemi 0.5μm CMOS process in order to experimentally verify eqn. (4). Large values of channel length L and channel area WL were used to avoid short channel effects and minimize $1/f$ noise, respectively. Specifically, the dimensions were 2496μm/24μm and 4416μm/12μm, respectively.

A. CIRCUIT DESIGN

The circuit used for noise measurements is shown in Fig. 2. It consists of the packaged IC, DC biasing circuits, a resistive load R_{DC}, and a custom low-noise preamplifier. The device under test (DUT) is measured in a common-source configuration: a manually adjustable bias circuit is used to set V_{GS}, the source and well terminals are connected either to ground (NMOS) or V_{DD} (PMOS) such that $V_{BS} = 0$ (no body effect), and R_{DC} is connected between the drain terminal and either V_{DD} (NMOS) or ground (PMOS). The potentiometer in the gate bias circuit is bypassed either to ground (NMOS) or V_{DD} (PMOS) with a large capacitor (11μF), resulting in a low-pass corner frequency of $\approx$ 15Hz. This scheme ensures that noise from V_{GS} is negligible at frequencies of interest. A set of 8 DIP switches is used to adjust the value of R_{DC} over a broad range (approximately 2.4kΩ to 500kΩ). A set of jumpers (S2-S5) allows a single preamplifier to be used to measure noise either from the DUT and load (in common-source configuration), or only the load.

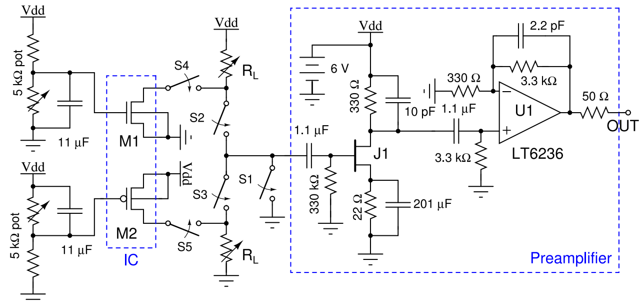

FIGURE 2. Schematic of the setup used for experimental noise measurements.

The preamplifier was designed to have very low input-referred voltage and current noise. It has two gain stages: the first uses an ultra-low-noise JFET (BF862, NXP), while the second uses a high-speed low-noise op-amp (LT6236, Linear). The measured overall voltage gain is $G \approx 70$ from 100Hz to several MHz. The measured input-referred voltage noise PSD is almost constant for frequencies from 2kHz to several MHz and has an average value of $\overline{e_n^2} = 0.87\text{nV/Hz}^{1/2}$; this is in excellent agreement with simulations. Moreover, the JFET has very low gate current of $\sim$ 3pA at room temperature, so the input-referred current noise is negligible ($\sim$ 1fA/Hz$^{1/2}$). The entire circuit was implemented on a two-layer circuit board, assembled inside an aluminum box to minimize external pickup, and run off batteries (2 sets of 4 AA cells, nominally $\pm$6V) to ensure that power supply noise was negligible [22].

The noise at the preamplifier output was measured with a spectrum analyzer (Agilent 4395A). The measured trace was averaged either 32 or 64 times to ensure low displayed average noise level (DANL). The flat "thermal" region of the spectrum (typically 2-20kHz) was then selected for further processing. The high end of this region is defined by low-pass filtering by capacitance at the drain terminal of the DUT, while the low end is defined by the $1/f$ noise from the DUT.

B. DATA PROCESSING

The measured output noise PSD was processed as follows. In saturation, the output conductance g_{ds} of the DUT is much smaller than R_L and can be ignored. The total output noise PSD in the thermally-dominated region is then given by

$$\overline{\Delta V_{out}^2} = \left[\overline{\Delta I_{ds}^2} R_L^2 + 4kTR_L + \overline{e_n^2}\right] |G|^2 , \qquad (7)$$

where $R_L = R_{DC}||(330\text{k}\Omega)$ is the AC load resistance and $\overline{e_n^2}$ and G are the preamplifier's input-referred voltage noise and voltage gain, respectively. The three terms in eqn. (7) correspond to DUT noise, load noise, and preamplifier noise, respectively. The ratio of the first and second terms is $\approx I_{DS}R_{DC}/V_L$, so the DUT noise will dominate as long as the DC voltage drop across the load resistance is much larger then the effective linear range of the device, i.e., $\phi_t/\kappa_s \approx$ 35mV in subthreshold or $(V_{GS} - V_{TS})/2$ above threshold. We ensured this condition by using the DIP switches to adjust the value ofR_{DC} for each value of V_{GS}. The resulting value of load noise was estimated by measuring the output noise of the preamplifier with the DUT disconnected. Similarly, the preamplifier's own noise was estimated by measuring its output with the input shorted to ground through switch S1. The low input-referred noise of the preamplifier ensures that it's noise is always much smaller than that of the DUT. Both the second and third terms are thus small compared to the DUT noise and can be subtracted from the total output noise without affecting the overall accuracy of the measurement. The result is then divided by the measured value of R_L and averaged over all frequencies in the thermal region to yield $\overline{\Delta I_{ds}^2}$.

We also used the same experimental setup to measure DUT noise in the unsaturated (linear) region. In this case one can no longer ignore the effects of g_{ds}. The resulting output noise PSD is given by

$$\overline{\Delta V_{out}^2} = \left[\left(\overline{\Delta I_{ds}^2} + \frac{4kT}{R_L}\right)\left(R_L || \frac{1}{g_{ds}}\right)^2 + \overline{e_n^2}\right] |G|^2 . \qquad (8)$$

The value of g_{ds} can be estimated from a DC I_{DS}-V_{DS} sweep of the device, and $\overline{\Delta I_{ds}^2}$ is then extracted from eqn. (8) using the same procedure described earlier.

C. TEMPERATURE DEPENDENCE

It is important to study the behavior of the proposed noise model versus temperature, since important device parameters such as threshold voltage and carrier mobility are strong functions of temperature. We made measurements inside a Peltier-cooled oven (Memmert IPP30) with a temperature accuracy of $\pm 0.1°$C to validate our model. Note that the preamplifier's input-referred current noise increases strongly with temperature. Fortunately, it remains negligible over our temperature range of interest (5-65°C), and thus does not have to be included in the analysis.

However, the experimental setup for temperature-dependent measurements is complicated by battery voltage droop, which results in a noticeable decrease of V_{GS} with time while the test setup is inside the oven. We eliminated this effect by using a low-dropout linear voltage regulator (LDO) to stabilize the DUT and preamplifier power supply

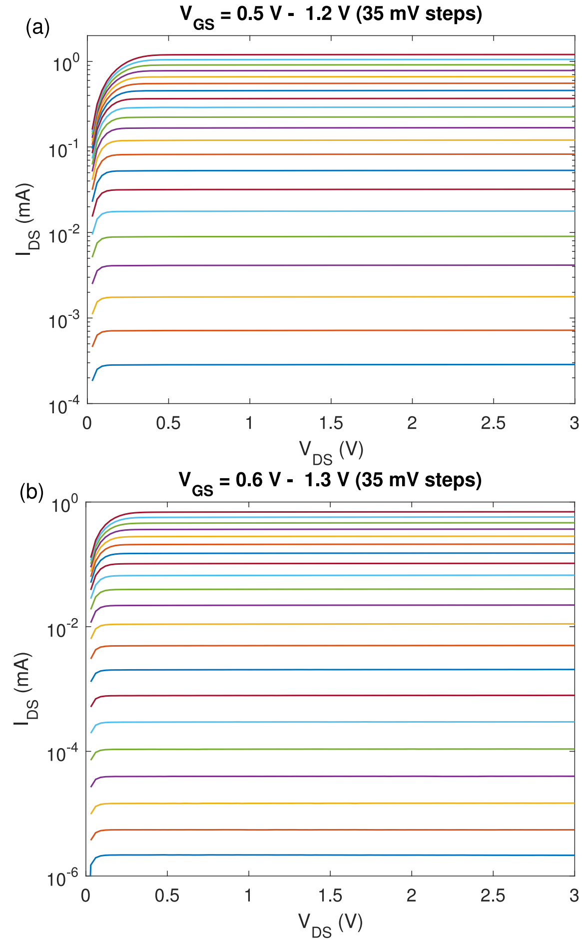

FIGURE 3. **Measured DC drain current as a function of V_{DS} and V_{GS} for (a) NMOS and (b) PMOS transistors at 20°C.**

voltage. The resulting in-band noise introduced by the LDO was eliminated by adding a second-order passive LC low-pass filter (cutoff frequency = 150Hz) to filter the regulated output voltage.

IV. RESULTS AND DISCUSSION

A. ROOM-TEMPERATURE MEASUREMENTS

Initial measurements were made at room temperature (20°C). The DC drain current I_{DS} of each device was measured as a function of V_{DS} and V_{GS} using a benchtop source measure unit (Keithley 2450). The results are shown in Fig. 3. They are in good agreement with long-channel MOSFET behavior. In particular, i) $V_{DSAT} \approx 4\phi_t$ in subthreshold and $\kappa_s (V_{GS} - V_{TS}) = x \times 2\phi_t$ above threshold; and ii) the output conductance $g_{ds} = \partial I_{DS}/\partial V_{DS}$ is negligible when $V_{DS} > V_{DSAT}$, i.e., in saturation.

The measured drain current at $V_{DS} = 3$V (see Fig. 3) was used to define the saturated current I_{DSAT} for each device. This quantity was plotted as a function of V_{GS} and fit to i) the exponential function $I_s \exp(\kappa_s V_{GS}/\phi_t)$ in subthreshold, and ii) the square law function $K(W/L)(V_{GS} - V_{TS})^2$ above threshold, as shown in Fig. 4. The best-fitting values of κ_s and V_{TS} are also shown on each plot.

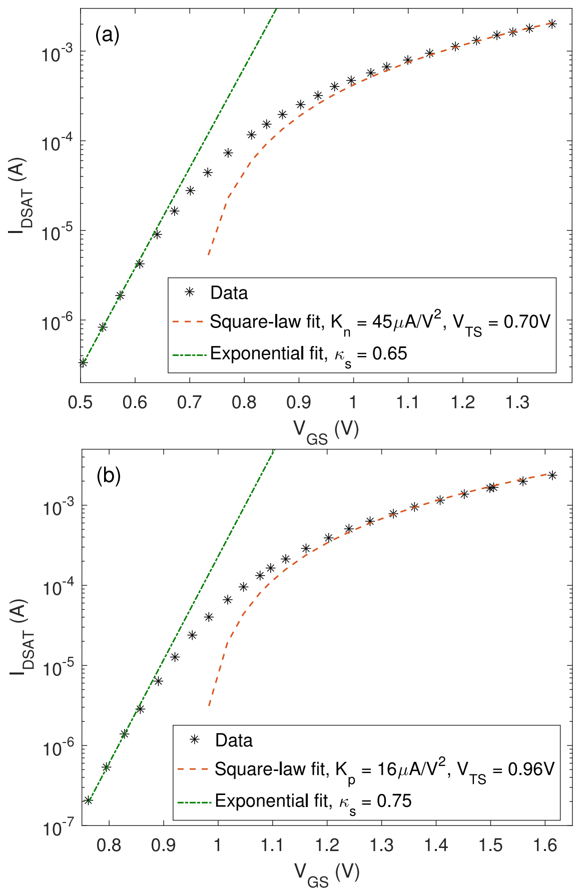

FIGURE 4. **Measured DC drain current in saturation (at $V_{DS} = 3V$) as a function of V_{GS} for (a) NMOS and (b) PMOS transistors at 20°C. Fits to i) an exponential function in subthreshold, and ii) a square-law function above threshold, are also shown.**

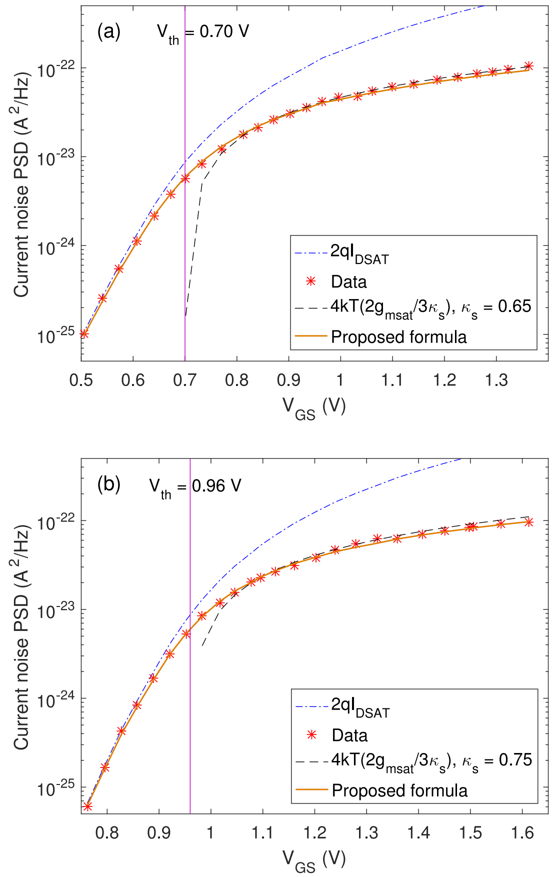

FIGURE 5. **Measured PSD of drain current noise in saturation as a function of V_{GS} for (a) NMOS and (b) PMOS transistors at 20°C. The measured V_{DS} varies between 1.1V and 6.1V for the NMOS, for which the maximum value of $V_{DSAT} = 0.43V$. Similarly, it varies between 1.8V and 6.0V for the PMOS, for which the maximum value of $V_{DSAT} = 0.49V$. Hence both devices are always saturated. Noise levels predicted by the proposed model (using $V_{TS'} \equiv V_{TS} + 2\phi_t$) are also shown.**

The measured values of $\overline{\Delta I_{ds}^2}$ in the saturation region for both devices are shown in Fig. 5 as a function of V_{GS}. The data covers all three regions of operation, namely weak, moderate, and strong inversion. The existing formulas for thermal noise in weak and strong inversion fit the data over their respective ranges of applicability, while the proposed formula, i.e., eqn. (4), fits well over the entire range. Specifically, the (mean, rms) fitting errors are (2.3%, 4.7%) and (1.5%, 4.0%) for the NMOS and PMOS, respectively. Moreover, these fitting errors are much smaller than the differences between eqns. (4) and (6) in moderate inversion (see Fig. 1). Hence the proposed model is more accurate than the EKV model in this region.

The linear region is not the focus of this paper, but we did measure noise from the PMOS as a function of V_{DS} for two V_{GS} values in moderate inversion. The results are shown in Fig. 6. This plot illustrates the high quality of our noise measurements. The increase in $\overline{\Delta I_{ds}^2}$ as $V_{DS} \to 0$ is intermediate between its theoretical values in weak and strong inversion (2 and 3/2, respectively). Moreover, it approaches 3/2 as V_{GS} increases, as expected.

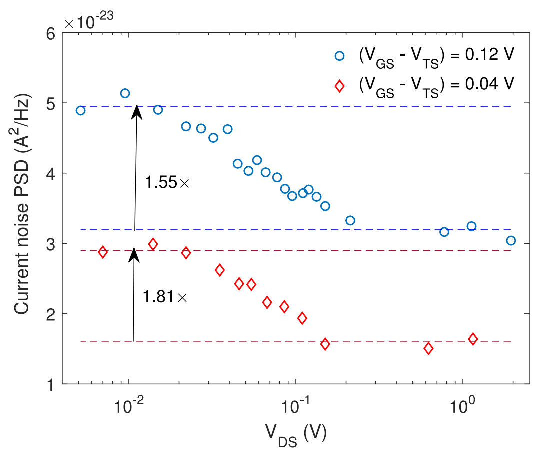

FIGURE 6. **Measured PSD of drain current noise of the PMOS as a function of V_{DS} for two different V_{GS} values in moderate inversion at 20°C.**

B. VARIABLE-TEMPERATURE MEASUREMENTS

Initially, a benchtop source measure unit (Keithley 2450) was used to measure the DC I_{DS}-V_{GS} curve of each device

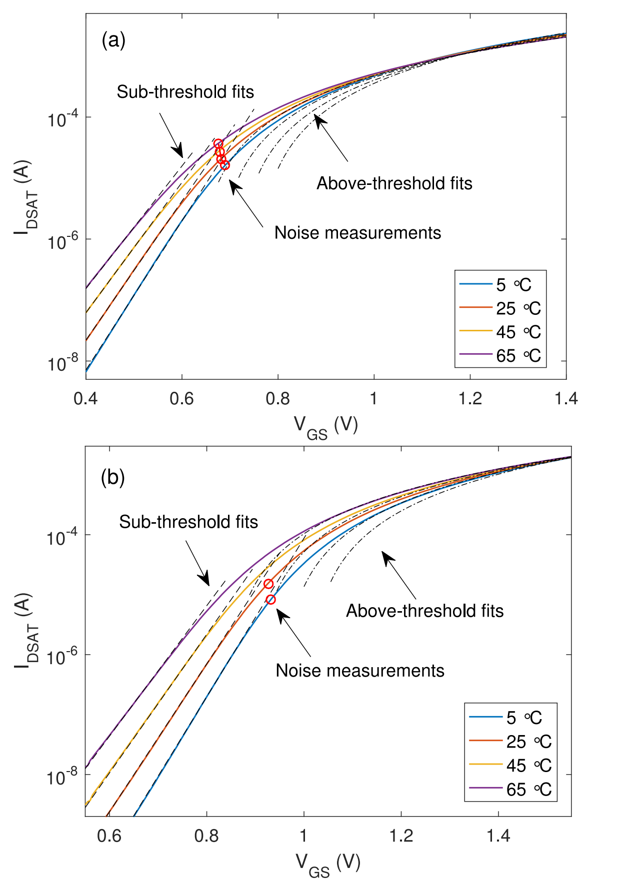

FIGURE 7. **Measured DC drain current in saturation (at $V_{DS} = 2$V) as a function of V_{GS} for (a) NMOS and (b) PMOS transistors at various temperatures. Fits to i) an exponential function in subthreshold, and ii) a square-law function above threshold, are shown. Circles represent the DC bias points at which noise was measured.**

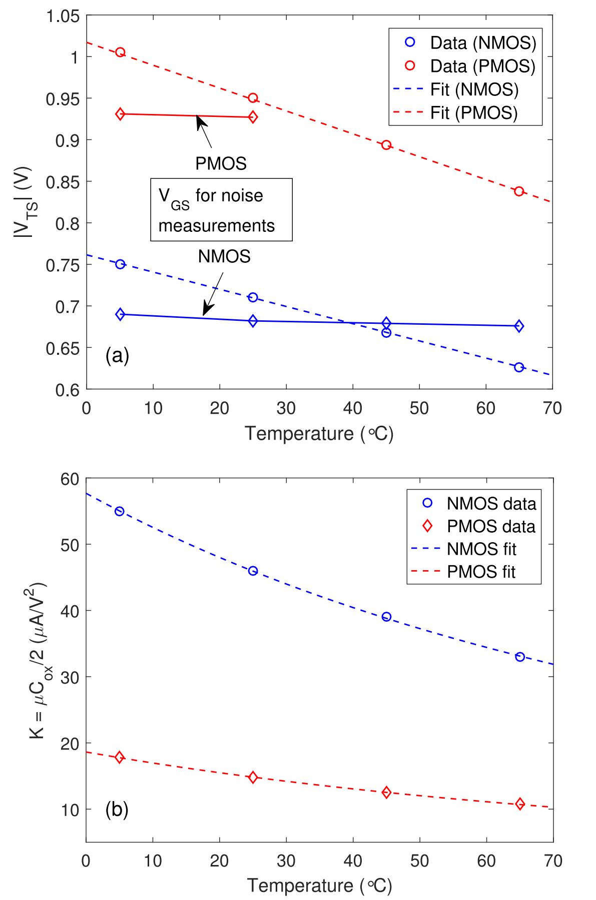

FIGURE 8. **Measured (a) threshold voltage V_{TS} and (b) drive strength $K = \mu C_{ox}/2$ of NMOS and PMOS transistors in saturation (at $V_{DS} = 2$V) as a function of temperature. In each case, fits to eqn. (9) are shown. In (a), the V_{GS} values at which noise was measured are also shown. The value of κ was temperature independent, and equal to 0.675 and 0.73 for the NMOS and PMOS, respectively.**

in saturation at temperatures between 5°C and 65°C. Each curve was then fitted to an exponential in subthreshold, and a square-law above threshold, as shown in Fig. 7.

The best-fitting values of threshold voltage V_{TS} and drive strength $K = \mu C_{ox}/2$ of the NMOS and PMOS transistors versus temperature are shown in Fig. 8. Both V_{TS} and K decrease with temperature in a similar way for the two devices. The figure also shows that these changes are well-described by the following expressions, which are similar to those used in both the BSIM4 and EKV models:

$$V_{TS}(T) = V_{TS}(T_{nom}) - TCV\,(T - T_{nom}),$$
$$\mu(T) = \mu(T_{nom})\left(\frac{T}{T_{nom}}\right)^{BEX}. \quad (9)$$

Here TCV and BEX are constants, while T_{nom} is the nominal temperature. Note that eqn. (9) results in a linear temperature dependence for V_{TS} and a polynomial one for μ (and thus K). Table 1 summarizes the measured model parameters for both devices.

For each device, a bias point in moderate inversion was then selected for performing temperature-dependent noise measurements. This choice was motivated by the fact that the proposed model provides a novel closed-form expression for drain current noise in this region. The measured bias points are shown in Figs. 7 and 8. The value of V_{GS} is almost constant with temperature, as expected, although it does decrease slightly because of the finite temperature coefficient of the LDO. Hence the gate overdrive voltage $x \equiv \kappa_s(V_{GS} - V_{TS})/(2\phi_t)$ increases with temperature. As a result, we expect the current noise PSD $\overline{\Delta I_{ds}^2}$ to diverge from the shot noise limit as temperature increases.

The measured values of $\overline{\Delta I_{ds}^2}$ in the saturation region for both devices are shown in Fig. 9 as a function of temperature. They are in very good agreement with the proposed model, with (mean, rms) fitting errors of (1.1%, 5.0%) and (1.4%, 1.7%) for the NMOS and PMOS, respectively. These values are similar to those for the room temperature measurements.

TABLE 1. **Summary of measured device parameters.**

Parameter	Value (NMOS)	Value (PMOS)
T_{nom} (°C)	20	20
$V_{TS}(T_{nom})$ (V)	0.70	0.96
TCV (mV/°C)	2.07	2.75
$K(T_{nom})$ (μA/V^2)	45.0	16.0
BEX	-2.6	-2.6
κ_s	0.65	0.75

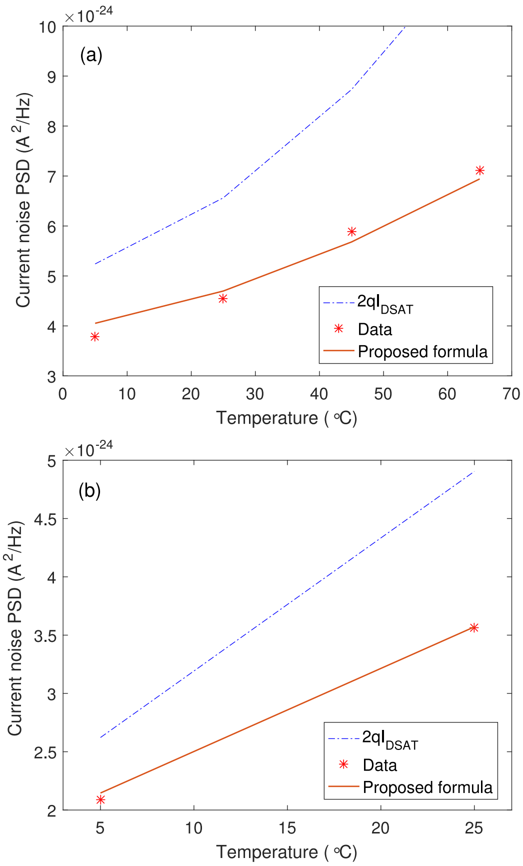

FIGURE 9. Measured PSD of drain current noise in saturation as a function of temperature for (a) NMOS and (b) PMOS transistors. The measured V_{DS} varied between 1.5V and 3.2V for the NMOS, for which the maximum value of $V_{DSAT} = 0.10$V. Similarly, it varied between 3.2V and 3.8V for the PMOS, for which the maximum value of $V_{DSAT} = 0.10$V. Hence both devices were always saturated. Noise levels predicted by the proposed model (using $V_{TS'} \equiv V_{TS} + 2\phi_t$) are also shown. Temperature-related component failures on the test board prevented us from making measurements beyond 25°C with the PMOS device.

V. CONCLUSION

We have proposed and verified an analytical model for the channel thermal noise of saturated long-channel MOSFETs in weak, moderate, and strong inversion. The model is simple enough to be useful for hand calculations, while also being in very good agreement with experimental data over a wide range of inversion levels and temperatures. It is based on treating charge smoothing within the MOSFET channel as an electrostatic negative feedback loop with bias-dependent loop gain A; the effect of feedback is to reduce the current noise PSD by a factor of $1/(1 + A)$ compared to full shot noise. The success of this feedback-based approach suggests that it may be beneficial in other scenarios. In particular, we plan to extend it in order to model MOSFET noise in i) the linear region; and ii) short-channel devices.

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