High Mobility In$_{0.53}$Ga$_{0.47}$As MOSFETs With Steep Sub-Threshold Slope Achieved by Remote Reduction of Native III-V Oxides With Metal Electrodes

S. YOSHIDA[1,2,3], H. C. LIN[2], A. VAIS[2], A. ALIAN[2], J. FRANCO[2], S. EL KAZZI[2], Y. MOLS[2], Y. MIYANAMI[1], M. NAKAZAWA[1], N. COLLAERT[2], H. WATANABE[3], AND A. THEAN[4]

1 Sony Semiconductor Solutions Corporation, Kanagawa 243-0014, Japan
2 IMEC, 3001 Leuven, Belgium
3 Osaka University, Osaka 565-0871, Japan
4 National University of Singapore, Singapore

CORRESPONDING AUTHOR: S. YOSHIDA (e-mail: shinichi.b.yoshida@sony.com)

ABSTRACT We have validated that the electrical performances of the In$_{0.53}$Ga$_{0.47}$As MOSFETs such as sub-threshold slope (SS) and electron mobility were dependent on interfacial reactions in the metal/high-k/InGaAs gate stacks which could be controlled remotely by choice of the metal electrodes. We demonstrated In$_{0.53}$Ga$_{0.47}$As MOSFETs with high mobility (peak mobility ~1300 cm^2/Vs) and superior SS performance (SS 76.4 mV/dec) at the scaled CET region owing to the remote reduction of the native III–V oxide by the TiN electrodes.

INDEX TERMS High-k gate dielectrics, indium gallium arsenide, MOSFETs, semiconductor-insulator interfaces.

I. INTRODUCTION

To overcome the physical limitations of metal–oxide–semiconductor field-effect transistors (MOSFETs) based on silicon channel materials, III-V semiconductors have been widely investigated as alternative channel materials [1]. InGaAs channel n-MOSFETs are widely considered one of the most promising candidates among the III–V materials because of their high electron-injection velocity [2]–[4]. To realize low-power, high-performance InGaAs MOSFETs, the issue of high-k/InGaAs gate stacks, which is a major challenge for InGaAs MOSFETs, needs to be addressed [5], [6]. It has already been reported that the poor properties of high-k/InGaAs interfaces negate the superior electron carrier transport properties of InGaAs materials due to carrier scattering [7]. Various passivation techniques have been used to reduce the high interface trap density (D$_{it}$) of high-k/InGaAs gate stacks, such as the so-called self-cleaning effect of the trimethylaluminum (TMA) precursor of Al$_2$O$_3$ grown by atomic layer deposition (ALD) [8] and sulfur

passivation by (NH$_4$)$_2$S solution [9]. However, previous studies have mainly focused on the high-k dielectrics or surface treatments of the InGaAs. The impact of metal electrodes on the performance of InGaAs MOSFETs has not yet been fully investigated. Recently, we systematically studied the effect of the metal electrodes on the interfacial reactions in high-k/InGaAs gate stacks. We revealed that the interfacial reactions could be controlled remotely by choice of the metal electrodes [10]. Metal electrodes with negative Gibbs free energies (e.g., Pd) compared with that of the III-V atoms resulted in oxidation of the InGaAs surface during the post annealing. Conversely, metal electrodes with positive Gibbs free energies (e.g., TiN) compared with that of the III-V atoms reduced the native III–V oxides between the high-k dielectrics and InGaAs. From our studies of InGaAs MOS-capacitors with different metal electrodes, we found that metal electrodes that can reduce the native III-V oxides are most suitable for creating a high-k/InGaAs interface with low D$_{it}$. In this work, we applied the interfacial

control method, using metal electrodes with $In_{0.53}Ga_{0.47}As$ MOSFETs and investigated the electrical performance of the devices, including characteristics such as the sub-threshold slope (SS) and electron mobility of MOSFETs with different metal electrodes.
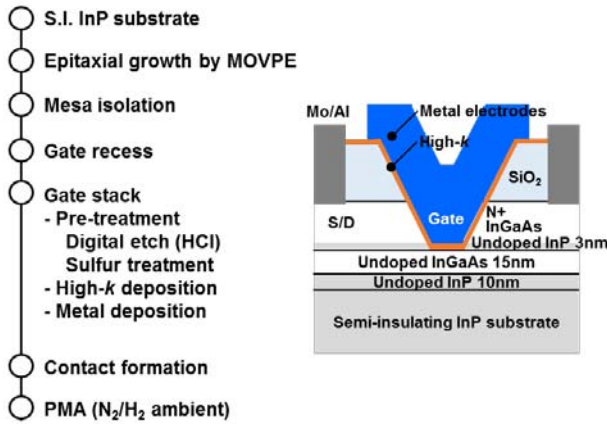

FIGURE 1. Process flow of InGaAs MOSFETs in this experiment.

II. EXPERIMENTS

Fig. 1 shows the process of $In_{0.53}Ga_{0.47}As$ MOSFET fabrication used in this experiment. We grew epitaxial layers composed of N^+ InGaAs (Si doping concentration, 1×10^{19} /cm^3)/undoped InP/undoped $In_{0.53}Ga_{0.47}As$ (15 nm thick)/undoped InP on InP substrates by metal organic vapor phase epitaxy (MOVPE). After a mesa isolation step, a gate recess process was applied to expose the undoped $In_{0.53}Ga_{0.47}As$ layer to create the surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs. Wet-chemical based digital etching using HCl and H_2O_2 followed by the sulfur treatment [$(NH_4)_2S$ 10%, 3 min] was performed to suppress the effects of interface traps. Then, the high-k dielectrics [(HfO_2/Al_2O_3 bi-layers) or (HfO_2 single layer)] were deposited by ALD. The precursors were TMA and H_2O for Al_2O_3, and $HfCl_4$ and H_2O for HfO_2. We evaluated four different metal electrode structures as shown in Table 1. On the basis of our previous results, the native III-V oxides, which remained between the high-k dielectrics and InGaAs layers, become reduced by TiN for HfO_2/Al_2O_3 bi-layers or a HfO_2 single layer. Conversely, the surface of InGaAs was oxidized by the Pd metal electrodes, resulting in the formation of III-V oxides at the high-k/InGaAs interface. The thickness of the grown III-V oxides can be controlled by the thickness of the Pd layer. We used a metal electrode structure with TiN 70 nm/Pd 10 nm to form ultrathin III-V oxide layers while suppressing an increase of the capacitance equivalent thickness (CET). We also selected Mo as a metal electrode, which does not cause any interfacial reactions at the high-k/InGaAs interface due to its comparable Gibbs free energies to the III-V atoms (In, Ga, As). Metal electrodes were patterned by a lift-off process and post metal annealing (PMA) was applied to all the samples in forming-gas

ambient at 400 °C or 450 °C. The temperature and time of the PMA was varied to identify the optimal annealing condition for the high-k/InGaAs interfaces. Capacitance–voltage (C_g-V_g) and I_D-V_G characteristics were obtained to evaluate the CET, electron mobility and the electrical performance of the $In_{0.53}Ga_{0.47}As$ MOSFETs.

TABLE 1. Gate stack structures of MOSFETS and interfacial reactions.

Metal electrodes	High-k dielectrics	Interfacial reactions induced by metal electrodes
TiN 80 nm	HfO_2	Reduction of the native III-V oxide
TiN 70 nm / Pd 10 nm	HfO_2	Oxidation of InGaAs surface
Mo 80 nm	HfO_2 / Al_2O_3	None reaction at the high-k/InGaAs interface
TiN 80 nm	HfO_2 / Al_2O_3	Reduction of the native III-V oxide

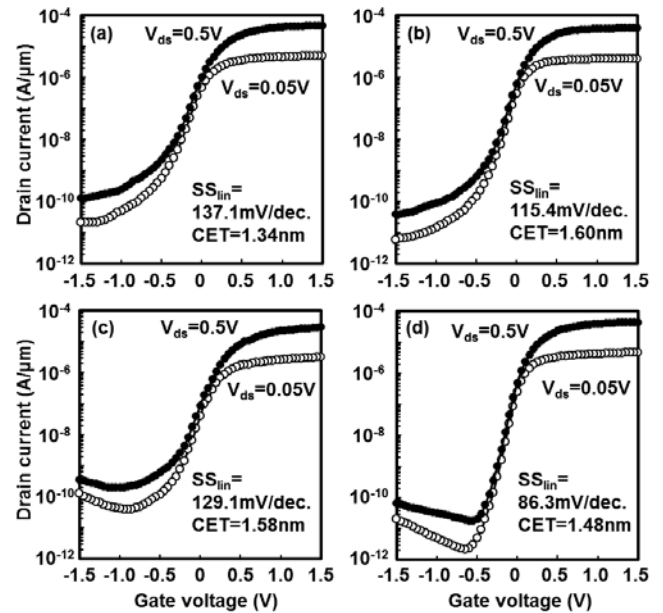TiN and Mo were deposited by sputter deposition. Pd was deposited by thermal evaporation.

FIGURE 2. I_D-V_G characteristics at V_{ds} = 0.5 V and 0.05 V with different metal electrodes and high-k stacks, (a) TiN/HfO_2 4nm, (b)TiN/Pd/HfO_2 4nm, (c) Mo/HfO_2 2nm/Al_2O_3 2nm, (d) TiN/HfO_2 2nm/Al_2O_3 2nm.

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the I_D-V_G characteristics (W/L = 100 μm/10 μm) at V_{ds} = 0.5 V and 0.05 V with four different metal/high-k stacks. Comparing the SS value for the TiN/HfO_2 gate stack to that for the TiN/Pd/HfO_2 stack, we confirmed that the value of SS was improved by adding Pd, owing to the formation of III-V oxides with fewer interface traps, despite an associated increase of the CET. The SS value of the Mo/HfO_2/Al_2O_3 stack was relatively worse, however, the TiN/HfO_2/Al_2O_3 stack showed the steepest SS of 86.3mV/dec. among all the MOSFETs. These results indicate that the native III-V oxides remained even after the

TMA self-cleaning effect of ALD-Al$_2$O$_3$ in the case of the Mo electrodes. Furthermore, the PMA with TiN considerably reduced the amount of native III-V oxides, which improved the properties of the high-*k*/InGaAs interface [10]. We also evaluated major I$_{off}$ contributors of the devices with the TiN/HfO$_2$ stack (worst SS) and the TiN/HfO$_2$/Al$_2$O$_3$ stack (best SS) as shown in Fig. 3. The leakage current of the device with the TiN/HfO$_2$ stack is mainly from the source to the drain. On the other hand, the source current (I$_S$) of the device with the TiN/HfO$_2$/Al$_2$O$_3$ stack reduced thanks to the superior interfacial properties as compared to that of the device with the TiN/HfO$_2$ stack. The gate leakage current (I$_G$) is also dominant at high negative bias for the TiN/HfO$_2$/Al$_2$O$_3$ stack.
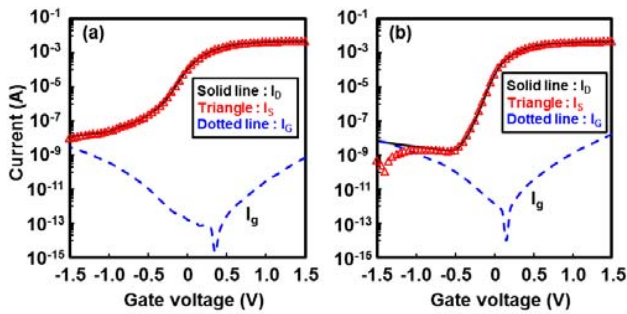

FIGURE 3. I$_D$, I$_S$ and I$_G$ as function of V$_G$ at V$_{ds}$= 0.5 V with different metal electrodes and high-*k* stacks, (a) TiN/HfO$_2$ 4nm, (b) TiN/HfO$_2$ 2nm/Al$_2$O$_3$ 2nm.

The SS values of all the samples are plotted as a function of the D$_{it}$ values at mid-gap which were evaluated by a conductance method using MOS-capacitors in our previous studies as shown in Fig. 4 (a) [10]. Moreover, the relationship between D$_{it}$ estimated from SS and D$_{it}$ of MOS-capacitors is also shown in Fig. 4 (b). It was clear that the SS values extracted from the MOSFETs strongly correlated with the D$_{it}$ values. Therefore, we could explain that the differences in the SS values observed among the samples were determined by the quality of the high-*k*/InGaAs interface.
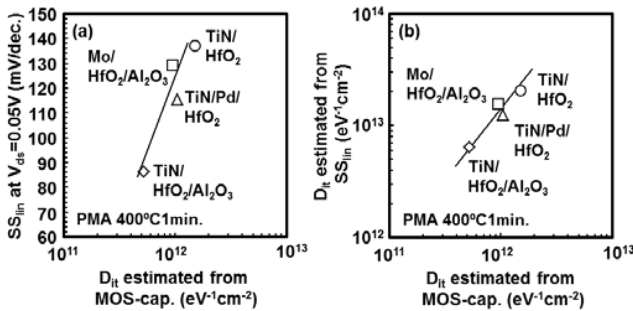

FIGURE 4. (a) SS values of InGaAs MOSFETs with different gate stacks as function of the D$_{it}$ values at mid-gap, (b) D$_{it}$ values estimated from SS of InGaAs MOSFETs with different gate stacks as function of the D$_{it}$ values at mid-gap estimated from MOS-capacitors.

We confirmed that the reduction of the native III-V oxides induced by PMA with TiN resulted in good interface quality and the improvement of SS values. Thus, it is important to carefully control the PMA conditions such as annealing temperature and time because the thermal budget of annealing is the driving force that can regulate the remote reaction initiated by the metal electrodes. Moreover, it is known that the annealing temperatures than 500 °C degrade the interface quality due to diffusion of III-V atoms from the III-V surface into the high-*k* dielectrics [11]. Thus, there is a window of optimal PMA conditions for processing the devices to achieve a native-oxide-free interface without any diffusion of III-V atoms. Fig. 5 (a) shows the SS values as a function of thermal budget for different metal/high-*k* stacks. For HfO$_2$ or HfO$_2$/Al$_2$O$_3$, the SS values gradually improved with longer annealing time up to 20 min at 400 °C as the reduction of the native III-V oxides by TiN proceeded. However, the SS values worsened from the PMA at 450 °C, which could be attributed to diffusion of III-V atoms into the high-*k* dielectrics. It should also be noted that the degradation of the SS values with PMA at high temperature for HfO$_2$ was quite severe compared with that of the HfO$_2$/Al$_2$O$_3$ stacked structure. This can be explained by the diffusion-blocking properties of Al$_2$O$_3$ over HfO$_2$ [12]. As the results, we could achieve superior SS performance (SS 76.4mV/dec.) with the remote reduction effect of the native III-V oxide by TiN through careful choice of the PMA conditions as shown in Fig. 5 (b).
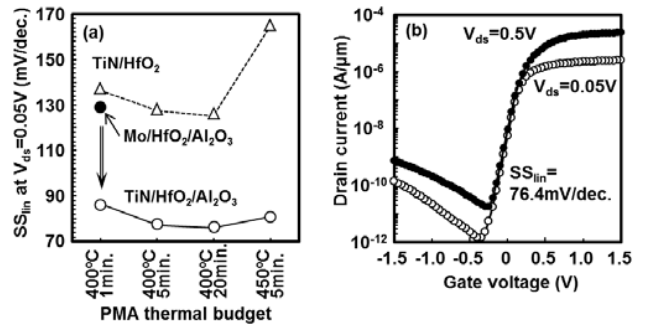

FIGURE 5. (a) Impact of the thermal budget of PMA on SS values, (b) I$_D$-V$_G$ characteristics (W/L = 100 μm/20 μm) at V$_{ds}$= 0.5 V and 0.05 V with TiN/HfO$_2$ 2nm/Al$_2$O$_3$ 2nm after 400 °C 20min PMA.

Fig. 6 shows C$_g$-V$_g$ curves of In$_{0.53}$Ga$_{0.47}$As MOSFETs with either TiN/HfO$_2$ 2 nm/Al$_2$O$_3$ 2 nm or TiN/HfO$_2$ 2 nm/Al$_2$O$_3$ 1 nm gate stacks after the optimal PMA condition (400 °C 20min). And the electron mobility as a function of carrier density (N$_s$) of In$_{0.53}$Ga$_{0.47}$As MOSFETs with that gate stacks is shown in Fig. 7. We extracted the electron mobility by split C-V method using the C$_g$-V$_g$ curves at 100 kHz to minimize the effect of oxide traps which was more significant at low frequency measurements, resulting in frequency dispersion as shown in Fig. 6 (b). The extracted CET was 1.48 nm for the TiN/HfO$_2$ 2 nm/Al$_2$O$_3$ 2 nm and
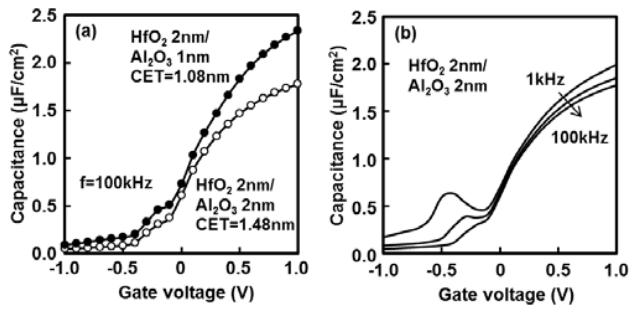
FIGURE 6. (a) C$_g$-V$_g$ curves at 100 kHz of TiN/HfO$_2$/Al$_2$O$_3$ gate stacks with different Al$_2$O$_3$ thickness, (b) C$_g$-V$_g$ curves from 1 kHz to 100 kHz of TiN/HfO$_2$ 2nm/Al$_2$O$_3$ 2nm gate stacks.
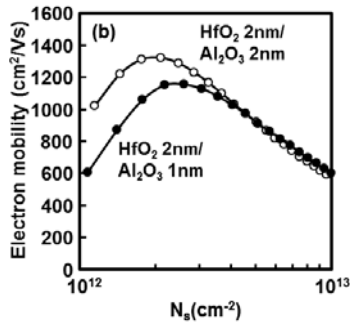

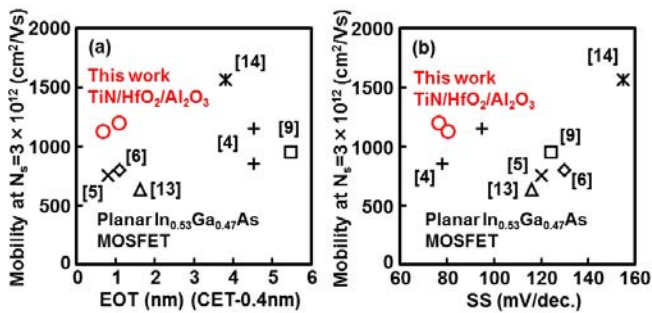**FIGURE 7.** Electron mobility as a function of carrier density (N$_s$) extracted by split C-V method.

FIGURE 8. Benchmark of the electron mobility at N$_s$ = 3×10^{12} (cm^2/Vs) as a function of (a) EOT and (b) SS values.

1.08 nm for the TiN/HfO$_2$ 2 nm/Al$_2$O$_3$ 1 nm, respectively. The MOSFETs with TiN/HfO$_2$ 2 nm/Al$_2$O$_3$ 2 nm showed a high electron mobility of 1,300 cm^2/Vs at the scaled CET region. We could also confirm that the peak mobility was degraded by scaling down the CET. This result could be attributed to carrier scattering effects becoming prominent due to the degradation of the interface trap density at the extremely scaled CET region. Finally, the combined high mobility, low SS and low equivalent oxide thickness (EOT) values are benchmarked against literature in Fig. 8 [13], [14]. Even with a sub-1 nm EOT, the In$_{0.53}$Ga$_{0.47}$As MOSFETs in this work exhibited high mobility accompanied with a lower SS.

IV. CONCLUSION

In conclusion, we investigated the impact of metal electrodes on the interfacial properties of metal/high-*k*/InGaAs gate stacks. We revealed that the electrical performance of the In$_{0.53}$Ga$_{0.47}$As MOSFETs could be modified by interfacial reactions in the high-*k*/InGaAs gate stacks, which could be remotely controlled by choice of the metal electrodes. Moreover, we validated that the In$_{0.53}$Ga$_{0.47}$As MOSFETs with TiN/HfO$_2$/Al$_2$O$_3$ gate stacks exhibited high mobility (Peak mobility ~1,300cm^2/Vs) and superior SS performance (SS 76.4mV/dec.) at the scaled CET region thanks to the remote reduction effect of the native III-V oxide by TiN.

REFERENCES

[1] S. Oktyabrsky and P. D. Ye, *Fundamentals of III–V Semiconductor MOSFETs*. Heidelberg, Germany: Springer, 2010.

[2] M. Radosavljevic et al., "Advanced high-K gate dielectric for high-performance short-channel In$_{0.7}$Ga$_{0.3}$As quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, Baltimore, MD, USA, Dec. 2009, pp. 319–322.

[3] S. Takagi et al., "MOS interface and channel engineering for high-mobility Ge/III-V CMOS," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2012, pp. 505–508.

[4] A. Alian et al., "Impact of the channel thickness on the performance of ultrathin InGaAs channel MOSFET devices," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2013, pp. 437–440.

[5] N. Goel et al., "Addressing the gate stack challenge for high mobility InxGa1-xAs channels for NFETs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2008, pp. 363–366.

[6] D. H. Zadeh et al., "Low D$_{it}$ high-k/In$_{0.53}$Ga$_{0.47}$As gate stack, with CET down to 0.73 nm and thermally stable silicide contact by suppression of interfacial reaction," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2013, pp. 36–39.

[7] S. Oktyabrsky et al., "Electron scattering in buried InGaAs MOSFET channel with HfO$_2$ gate oxide," in *Proc. MRS*, vol. 1155. 2009.

[8] C. L. Hinkle et al., "GaAs interfacial self-cleaning by atomic layer deposition," *Appl. Phys. Lett.*, vol. 92, no. 7, 2008, Art. no. 071901.

[9] Y. Urabe et al., "Correlation between channel mobility improvements and negative Vth shifts in III–V MISFETs: Dipole fluctuation as new scattering mechanism," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2010, pp. 142–145.

[10] S. Yoshida et al., "Systematic study of interfacial reactions induced by metal electrodes in high-k/InGaAs gate stacks," *Appl. Phys. Lett.*, vol. 109, no. 17, 2016, Art. no. 172101.

[11] H.-D. Trinh et al., "Effect of postdeposition annealing temperatures on electrical characteristics of molecular-beam-deposited HfO$_2$ on n-InAs/InGaAs metal–oxide–semiconductor capacitors," *Appl. Phys. Exp.*, vol. 5, no. 2, 2012, Art. no. 021104.

[12] H. Dong et al., "Indium diffusion through high-k dielectrics in high-k/InP stacks," *Appl. Phys. Lett.*, vol. 103, no. 6, 2013, Art. no. 061601.

[13] J. Huang et al., "InGaAs MOSFET performance and reliability improvement by simultaneous reduction of oxide and interface charge in ALD (La)AlOx/ZrO2 gate stack," in *IEDM Tech. Dig.*, Baltimore, MD, USA, Dec. 2009, pp. 335–338.

[14] H.-C. Chin, X. Liu, X. Gong, and Y.-C. Yeo, "Silane and ammonia surface passivation technology for high-mobility In$_{0.53}$Ga$_{0.47}$As MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 973–979, May 2010.

S. YOSHIDA, photograph and biography not available at the time of publication.

H. C. LIN, photograph and biography not available at the time of publication.

A. VAIS, photograph and biography not available at the time of publication.

A. ALIAN, photograph and biography not available at the time of publication.

J. FRANCO, photograph and biography not available at the time of publication.

S. EL KAZZI, photograph and biography not available at the time of publication.

Y. MOLS, photograph and biography not available at the time of publication.

Y. MIYANAMI, photograph and biography not available at the time of publication.

M. NAKAZAWA, photograph and biography not available at the time of publication.

N. COLLAERT, photograph and biography not available at the time of publication.

H. WATANABE, photograph and biography not available at the time of publication.

A. THEAN, photograph and biography not available at the time of publication.