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First Demonstration of a Two-Tier Pixelated Avalanche Sensor for Charged Particle Detection

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ABSTRACT This paper presents the first experimental demonstration of a pixelated two-layer Geiger-mode avalanche sensor designed for the direct detection of charged particles. In the proposed device, each pixel is formed by two vertically aligned avalanche detectors, exploiting the coincidence between two simultaneous avalanche events to discriminate between the detection of particles and dark counts. A 48 $\times$ 16 pixel array has been designed and fabricated in a 150-nm CMOS process and vertically integrated through bump bonding. The pixel, that includes passive quenching, comparator, and digital electronic circuits for coincidence processing and signal storage, has a size of 50 μm $\times$ 75 μm and a maximum fill factor of 51.6%. The operation of the particle sensor has been validated with the measurement of dark count rate distribution at different coincidence resolution times. An average dark count rate per pixel as low as 93 mHz, corresponding to 24 Hz/mm^2, was obtained at room temperature. A first sensor validation using a ^{90}Sr β source is presented.

INDEX TERMS Avalanche pixel sensor, particle detector, SPAD, CMOS, bump bonding.

I. INTRODUCTION

In the last decade, CMOS technologies have proved to be excellent platforms for the realization of integrated optical sensors as well as for pixelated charged particle sensors [1]–[4]. While pinned photodiodes have become the detectors of choice in image sensors, the ultimate performance in terms of sensitivity and timing resolution for the detection of ultrafast optical signals can be obtained using Geiger-mode avalanche diodes, a.k.a. Single Photon Avalanche Diodes (SPADs) [5]. Pixelated CMOS optical sensors based on SPADs have been demonstrated in several application domains: among others it is worth mentioning optical ranging, Fluorescence Lifetime Imaging , Positron Emission Tomography and Raman Spectroscopy [6]–[11].

A preliminary study for the integration of a Geiger-mode avalanche particle detector in CMOS has also been presented [12]–[14]. Since in Geiger mode it is impossible to discriminate particle-generated signals from dark events, the use of two Geiger-mode avalanche diodes in coincidence has been proposed [15], but a pixel array based on this concept has never been presented so far. An experimental validation of the idea was carried out using two silicon photomultipliers (SiPM) in coincidence, demonstrating a detection efficiency larger than the SiPM

geometrical Fill Factor, but without providing spatial information [16], [17].

In charged particle tracking and counting applications, the detectors of choice can be either hybrid or monolithic depending on the required resolution and radiation damage tolerance. In the case of hybrid detectors, bump bonding is typically used to connect the sensor array to a readout electronic chip. This approach offers the flexibility of customizing sensors and electronics independently, at the expense of a larger parasitic input capacitance. Since the input noise of the readout electronics is increased by large input capacitances, a large charge discrimination threshold needs to be set in hybrid detectors, thus limiting the minimum detectable charge. The large threshold affects the minimum detector thickness, that is around 100μm in the hybrid pixels currently under development for tracking in high-energy physics applications [18], [19]. In State-of-the-Art monolithic detectors, the active area is typically limited to a few 10s of μm and full substrate depletion is not achieved. However, they exhibit a good signal-to-noise ratio thanks to their low parasitic capacitance, and their charge collection time can be as low as a few tens of ns [20]. For ultrafast timing applications, a class of detectors with low-gain avalanche amplification is emerging, providing a timing resolution as low as a few 10s of ps [21]. For this class of detectors, however, a fine pixelation has still to be demonstrated. If compared to existing solutions, the proposed Geiger-mode avalanche pixel is potentially interesting for combining fine pixelation, low material budget, low power consumption and timing resolutions that in principle can be lower than 100ps thanks to Geiger-mode operation.

To fully exploit the potential of the coincidence detection concept, low-noise avalanche detectors need to be co-integrated with deep submicron readout circuits, and two detector layers should be vertically integrated. Several examples of 3D-integrated SPAD arrays for optical sensing have been recently presented [22]–[24], supporting the technological feasibility of the proposed approach.

In this work, we present a two-layer sensor based on avalanche detectors in coincidence fabricated in a commercial 150nm CMOS process and integrated using a standard bump bonding technology. The architecture of the sensor is described in Section II. A selection of results from the experimental validation of the sensor is shown in Section III, while possible improvements of the proposed sensor in view of the potential applications are discussed in Section IV.

II. SENSOR DESIGN

The coincidence pixel is composed of 2 levels of detectors and electronics, with a vertical interconnection used to deliver the digitized signal from the top to the bottom layer (Fig. 1).

The Geiger-mode detectors used in this work, fabricated in a commercial 150nm CMOS process (6 metal, 1 poly), have been previously developed for optical sensing applications [25], [26]. The detector junction, implemented as p+ or pwell in a deep nwell, is isolated from the p-type substrate. Therefore, the thickness of the active volume is very narrow, in the order of 1μm [26]. The detectors have been covered with a metal shield to avoid optical cross-talk between different layers, but a few pixels have been left unshielded to enable optical tests.

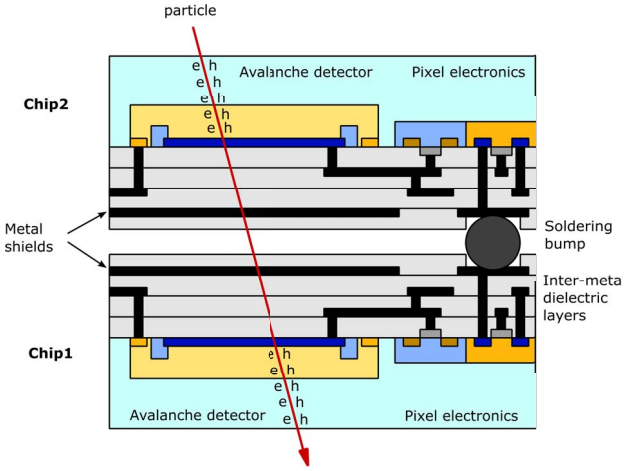

FIGURE 1. Cross section of a two-layer CMOS pixel based on avalanche detectors in coincidence.

A simplified schematic diagram of the pixel is presented in Fig. 2. The detector front-end is the same in both layers, and includes a quenching transistor, a comparator and a programmable monostable for pulse shortening. The coincidence resolution time depends on the monostable pulse width, that can be set to three different nominal values of 750ps, 1.5ns or 10ns. A configuration register is used to independently enable or disable the pixels with an arbitrary pattern. The bottom half-pixel also includes a coincidence detector and digital electronic circuits for data storage (1bit/pixel) and readout.

The pixel array, having a total size of 16 $\times$ 48 pixels, is partitioned in subarrays with 4 different detector sizes. Each pixel has a size of 50 μm x 75 μm, with a maximum geometrical fill factor of 51.6%. The peripheral electronic circuits offer the flexibility for mapping dark count rate (DCR), timing resolution and crosstalk probability between different pixels in the same layer [27].

A micrograph of the bottom chip is shown in Fig. 3(a), while 3(b) shows a concept view of the complete sensor, where the two tiers have been vertically integrated using a flip chip process with SnAg solder bumps. In the final assembly, the bottom chip is connected to the package through standard wire bonds, while power, analog and digital signals are supplied from the bottom to the top chip through bump bonding pads.

III. EXPERIMENTAL RESULTS

A few samples of top and bottom chips were wire-bonded for testing before proceeding to vertical integration. Electrical tests showed the correct functionality of both avalanche detectors and electronics in the two chips.

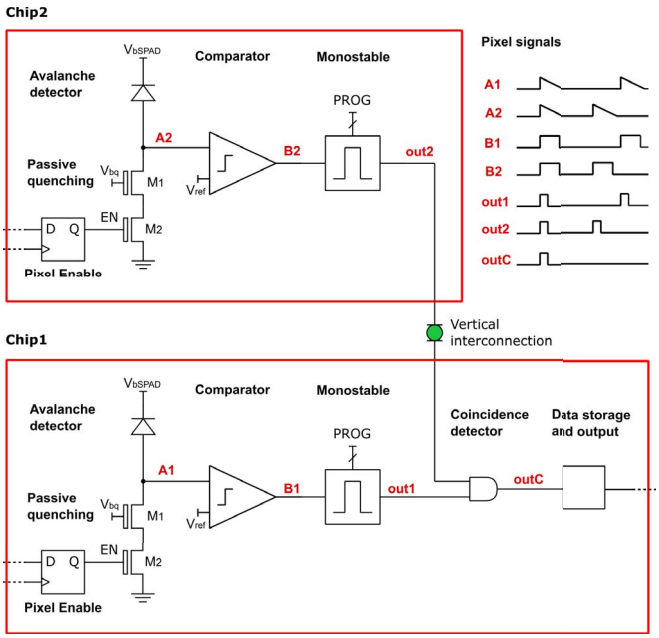

FIGURE 2. **Simplified schematic of the pixel and illustration of pixel signals timing.**

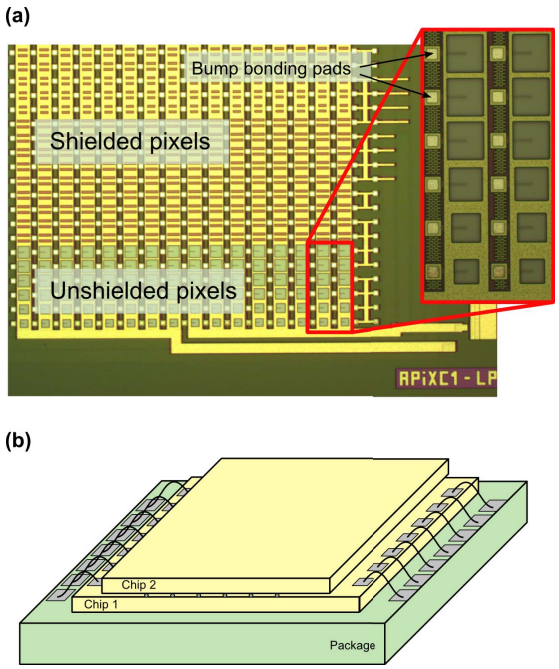

FIGURE 3. **(a) Micrograph of the bottom chip (partial view) with detail of a group of pixel (b) Concept view of the vertically-integrated sensor assembly.**

The measurements reported hereafter were conducted on detectors with an active junction of type pwell/deep nwell (indicated as Type 2 in [27]). The DCR cumulative distribution measured at different temperatures for two different excess voltages is shown in Figure 4 for the largest detectors, having 43 μm $\times$ 45 μm active area. A median DCR of 3 kHz, corresponding to 1.5 Hz/μm^2 was measured at

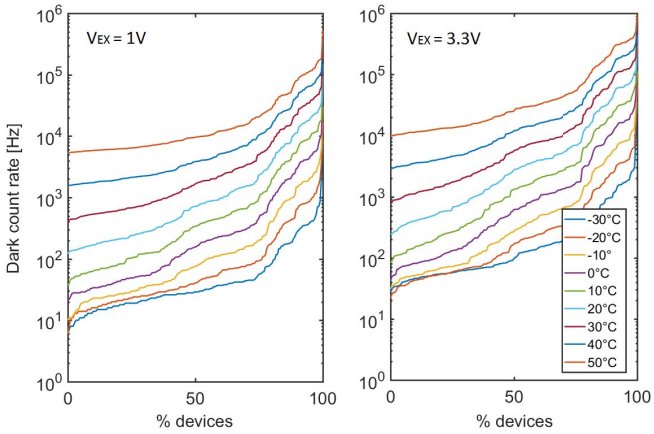

FIGURE 4. **Pixel DCR distribution for 43 μm $\times$ 45 μm active area at two different excess bias voltages and at different temperatures.**

room temperature and 3.3V overvoltage. It is worth noting that, for the best devices in the low part of the distribution, a DCR 10 times lower than the median value was measured. It can also be observed that, for these low-DCR devices, the DCR temperature coefficient tends to become very low at temperatures lower than -10^{o}C, indicating a generation rate dominated by band-to-band tunneling.

At room temperature, the DCR distribution is spread over more than two orders of magnitude. Analyzing the activation energy of the DCR time dependence, we found out that in most devices its value is lower than silicon $E_G/2$, indicating that the origin of DCR at room temperature is mainly due to trap-assisted tunnelling [27]. The large spread in the measured DCR can be explained considering that the shape of the DCR distribution is affected by the distribution of trapping centers inside the non-uniform electric field of the space-charge region. A similar distribution can be found in other SPAD-related works [5], [6].

Cross-talk measurements were also conducted at different voltages, demonstrating an average optical cross-talk in the range of a few percent between neighboring pixels at 3V overvoltage [28]. Preliminary single-photon timing resolution measurements, performed on unshielded samples with a blue picosecond laser, showed a timing resolution in the order of 200ps FWHM, even though the array electronics was not optimized for timing. The core of each chip, working at 1.8V, absorbs a current of 8mA, mainly due to the static current required by the comparators. A summary of the electrical tests performed on the single chips before vertical integration is presented in [27] and [28].

In the vertically integrated assemblies, the functionality of both layers was preserved after bump bonding, even though a small number of pixels was not working in the bottom chip. The measurements presented hereafter were conducted on a 8 $\times$ 24 subarray, where all the pixels have the same detector type and size and are all functional. Also in this case, the detectors active area is 43 μm $\times$ 45 μm and the pixels have 51.6% Fill Factor. The DCR could be mapped correctly on

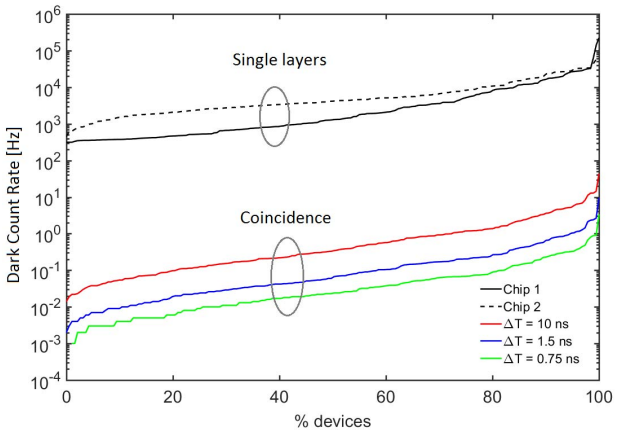

FIGURE 5. DCR distribution of the pixels measured separately in the two chips and distribution of the DCR in coincidence for 3 different settings of the pixel monostable circuit. Measurements are done at T=20^{o}C and V_{EX} = 1 V.

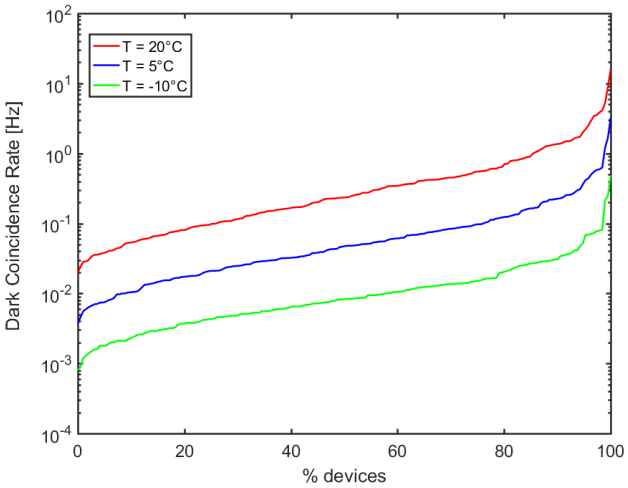

FIGURE 7. DCR distribution of the pixels as a function of temperature. Measurements are done at V_{EX} = 2 V and ΔT = 0.75 ns.

both layers and was in agreement with previous measurements. The distribution of dark coincidence measurements in the array, with the 3 different monostable width settings, are shown in Figure 5 together with the DCR of the separate layers. The average coincidence DCR (DCR_C) is as low as 93 mHz per pixel with the minimum pulse width, corresponding to 24 Hz/mm^2. This value is in good agreement with the theoretical value predicted by

$$DCR_C = DCR_1 \cdot DCR_2 \cdot 2\Delta T \tag{1}$$

where DCR_1 and DCR_2 is the DCR of the two layers, separately, and ΔT is the coincidence resolution time defined by the monostable pulse width.

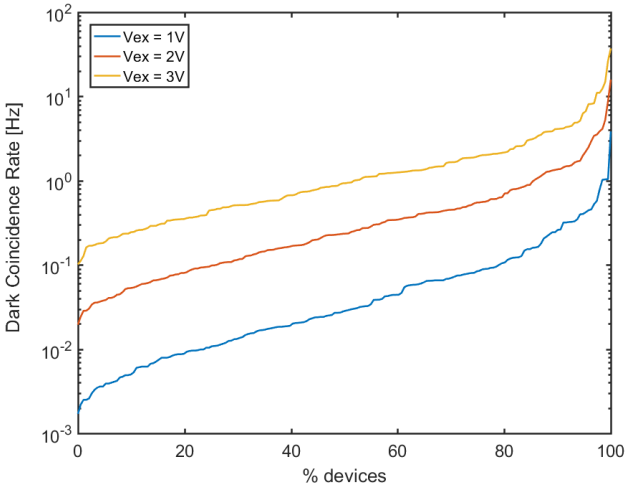

FIGURE 6. DCR distribution of the pixels as a function of V_{EX}. Measurements are done at T=20^{o}C and ΔT = 0.75 ns.

The coincidence DCR distribution is shown as a function of V_{EX} and temperature in Figures 6 and 7. It is worth noting that both the voltage and temperature dependence of DCR is enhanced by the coincidence, since they affect both terms DCR_1 and DCR_2 in equation 1.

A validation of the sensor operation with charged particles was carried out using a ^{90}Sr β source with 39 kBq±6% activity and 2 cm^2 area. The source was placed on top of the sensor at 5 mm distance from its surface. The setup was placed in a climate chamber and cooled to 5^{o}C, in order to reduce the DCR to levels comparable or lower than the count rate induced by the β source, and the sensors were biased with V_{EX} = 1V. In the measurements, a large number of frames with 1 ms integration time were summed, to obtain a total accumulation time of 10000 s. The count rate distribution was acquired both in the presence and in the absence of the source, and is shown in Figure 8(a), while the distribution of the count rate difference is shown in Figure 8(b). Figure 8(c) shows a response map of the array, that does not exhibit any apparent gradient. This is not surprising, since the source size is much larger than the detector and was centered on it for the measurements.

The average count rate per pixel induced by β particles is approximately 33mHz, while the distribution follows the Poisson statistics. Since the total measurement time was 10^4 s, considering only the beta events, the expected uncertainty due to Poisson statistics should be $\sigma = \sqrt{0.033/10^4} =$ 1.8 mHz. The measured uncertainty is σ = 2 mHz, in good agreement with the estimated value.

IV. DISCUSSION

The measurements carried out with the beta source provide a first means to evaluate the performance of the sensor in particle counting applications. The measured count rate corresponds to a detection rate of 8.8 events/(mm^{2}s), to be compared with 197±6% events/(mm^{2}s) emitted by the ^{90}Sr source. Monte Carlo (MC) simulations were used to quantify the different effects accounting for the observed charged-particle detection efficiency.

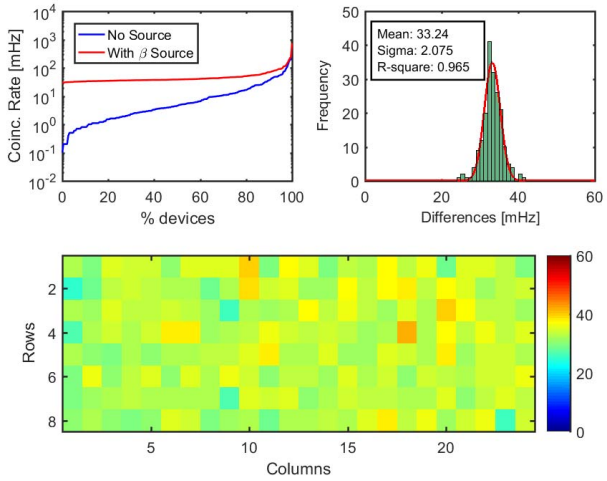

FIGURE 8. (a) Count rate distribution with and without β source. (b) Distribution of the count rate difference. (c) Map of the count rate difference.

Among the several factors accounting for the measured inefficiency, the most relevant one is the geometric acceptance of the detector, which depends on the relative position between source and detector. According to MC simulations, with the geometrical arrangement used in the measurements, the hit rate on the detector surface should amount to 50 Hz/mm^2.

Another important contribution is given by the pixel fill factor, whose design value is around 50%. Previous measurement campaigns conducted on SiPMs suggest that the geometrical fill factor in the case of particles might be larger than the one measured optically [17], but this should be experimentally confirmed on this CMOS prototype using a controlled particle beam with nearly orthogonal incidence.

The thickness of the top chip is 280 μm, so a consistent fraction of the low-energy particles emitted by the ^{90}Sr source is absorbed in the substrate of the top chip before arriving to the active region. According to MC simulations, only 40% of the β particles arriving at the surface can reach the active layer.

The angle of incidence constitutes another source of inefficiency, since particles hitting the sensor with a non-orthogonal angle might generate a signal only in one of the two layers. Particles incident at large angles are more likely to fail hitting both layers.

Some events, despite crossing the sensor within the active volume, might not generate charge due to the granularity of charge release in the very thin active region. MC simulations predict that, in more than 99% of the cases, at least 1 electron is released in the active volume, while at least 5 electrons are generated in 97.5% of cases.

Last, even if one or more electron-hole pairs are generated within the active volume, there might be a small chance that the avalanche is not self-sustaining since the avalanche triggering probability P_t is lower than 100%. The value of P_t due to charged particle could be estimated starting from optically measured data. If P_{t1} is the triggering probability associated with 1 generated electron-hole pair, i.e., the value measured optically, the combined triggering probability P_{tN}, due to the generation of N electron-hole pairs, can be estimated as

$$P_{tN} = 1 - (1 - P_{t1})^N. \quad (2)$$

If, for example, P_{t1} = 50%, according to equation 2 P_{t5} = 97% and P_{t10} = 99.9%. Therefore, even though the optically-measured avalanche triggering probability is far from 100%, in most cases several electrons are generated with charged particles and the combined probability can be very close to 100%.

Taking all these effects into account, MC simulations predict a particle-induced count rate of 7.3 Hz/mm^2, in good agreement with the experimentally measured 8.8 Hz/mm^2 rate.

V. CONCLUSION

In this paper, we have presented the first demonstration of a pixel array for charged particles based on Geiger-mode avalanche detectors in coincidence. The experimental results indicate that detectors with a fine pixelation, a good uniformity and small power consumption are feasible with the adopted technology. The coincidence DCR depends on the DCR statistics of the single detectors, that in turn is strongly affected by the distribution of defects in the sensor active volume. MC analysis has showed that the main limitations to the detection efficiency are the thickness of the top-chip substrate and the geometrical fill factor of the detectors.

It is worth noting that the aforementioned factors can be addressed and both the sensor DCR and its particle detection efficiency can be improved. In fact, sensors based on the proposed concept can benefit from the technological developments of CMOS-integrated SPADs. The pixel DCR can be reduced by employing dedicated implantations and processes customized for image sensors [5], while the geometrical fill factor, not optimized in this first trial, can be increased by adopting a more scaled CMOS process [23]. With an advanced process node, the pixel size can also be reduced with a minimum loss of efficiency. Since the devices have a very small active thickness and are isolated from the substrate, the substrates can be thinned down to a few microns without compromising sensor functionality and DCR.

An aggressive thinning would enable the stacking of more than two layers for improved efficiency while maintaining a low material budget. These properties, together with the picosecond timing resolution achievable thanks to Geiger-mode operation, make the proposed sensors appealing for particle counting and timing in high-energy physics and medical applications.

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