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Sub-60-mV/decade Negative Capacitance FinFET With Sub-10-nm Hafnium-Based Ferroelectric Capacitor

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ABSTRACT The negative capacitance (NC) of ferroelectric materials has paved the way for achieving sub-60-mV/decade switching feature in complementary metal-oxide-semiconductor (CMOS) field-effect transistors, by simply inserting a ferroelectric thin layer in the gate stack. However, in order to utilize the ferroelectric capacitor (as a breakthrough technique to overcome the Boltzmann limit of the device using thermionic emission process), the thickness of the ferroelectric layer should be scaled down to sub-10-nm for ease of integration with conventional CMOS logic devices. In this paper, we demonstrate an NC fin-shaped field-effect transistor (FinFET) with a 6-nm-thick HfZrO ferroelectric capacitor. The performance parameters of NC FinFET such as on-/off-state currents and subthreshold slope are compared with those of the conventional FinFET. Furthermore, a repetitive and reliable steep switching feature of the NC FinFET at various drain voltages is demonstrated.

INDEX TERMS Negative capacitance, steep switching devices, Hafnium-based ferroelectric material, FinFET.

I. INTRODUCTION

Following Moore's Law over the past few decades, the number of transistors per unit area in integrated circuits (ICs) has been successfully doubled every two years. In order to pursue constant-field scaling, the power supply voltage (V_{DD}) of a transistor should be reduced by the same degree that the physical size of the transistor is minimized. Unfortunately, V_{DD} has not been successfully scaled down; therefore, the power density per unit area in ICs has been exponentially increasing. One solution to address the issue of ever-increasing power density is to improve the subthreshold slope (SS) of conventional devices. SS indicates the inverse slope of the input transfer characteristic plot of a transistor in the subthreshold region, and it cannot be lower than 60 mV/decade at 300 K in a conventional device owing to the Boltzmann distribution of carriers in the device. There are two primary ways to implement SS below 60 mV/decade at 300 K. The first method is to adopt a novel operating principle instead of the thermionic emission process. For example, tunnel field-effect transistor (FET) [1], spintronic device [2], and nanoelectromechanical switch [3] are representatives of this solution. The other method is to lower the 'm' factor, which indicates the sensitivity of the gate voltage (V_G) to the surface potential (φ_S). Accordingly, $m < 1$ can be achieved using the negative capacitance (NC) effect [4]–[9]. Contrary to the aforementioned steep switching devices, when transforming a FET to an NCFET, a single ferroelectric layer is only required in the gate stack of a conventional transistor. While the polarization switching occurs inside the ferroelectric material, the

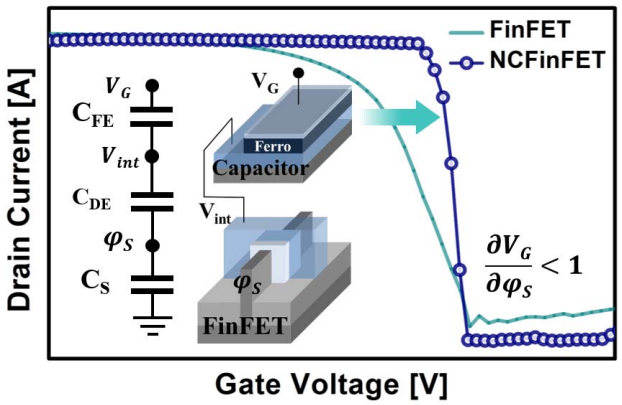

FIGURE 1. **The input transfer characteristic of NC FinFET (vs. FinFET) shows the concept of steep switching event. The 'm' factor (i.e., $m = \Delta V_G / \Delta \varphi_S$) can be lower than 1, and thereby, steep switching of sub-60-mV/decade SS occurs. The device structure of p-type NC FinFET and its capacitive network are included as inset.**

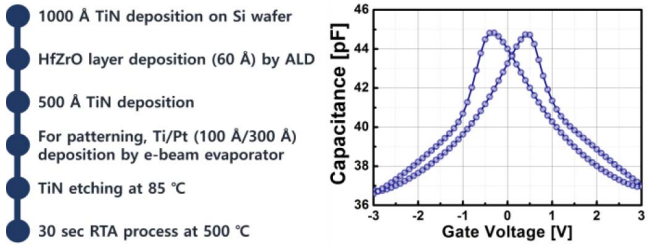

FIGURE 2. **Brief process flow of the HfZrO ferroelectric capacitor (left), and the measured capacitance-voltage (*C–V*) plot of the fabricated capacitor (right).**

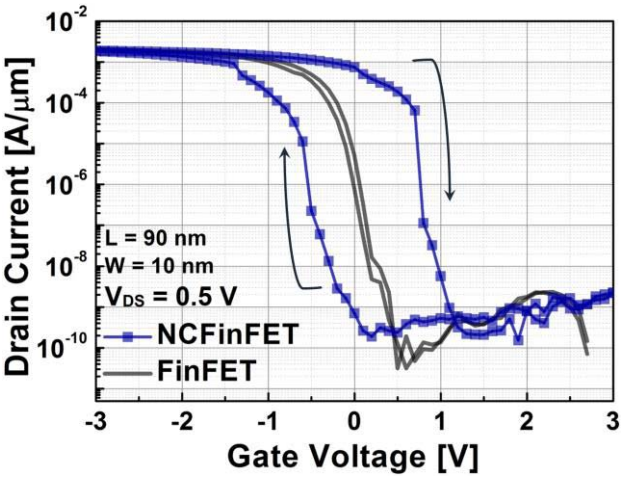

FIGURE 3. **Measured input transfer characteristic of NC FinFET (vs. FinFET). The channel length and fin width of the FinFET were 90 nm and 10 nm, respectively. The drain voltage was 0.5 V.**

internal voltage is amplified (e.g., $V_G < \varphi_S$) by the NC of the ferroelectric material. Consequently, the factor 'm' can be reduced below 1, resulting in sub-60-mV/decade SS at 300 K (refer to Fig. 1). Various studies using typical ferroelectric materials such as BFO [4] or PZT [10] have been conducted with the NCFET. However, it is difficult to adopt these materials in conventional CMOS logic devices, since they are not compatible with current CMOS fabrication processes. Hence, a CMOS-compatible ferroelectric material, e.g., hafnium-based ferroelectric material [11]–[13], is mandatory for sub-10-nm CMOS technology. In recent studies, the ferroelectricity of a hafnium-based material and the steep switching characteristic of an NCFET with a hafnium-based ferroelectric capacitor have been experimentally demonstrated [14], [15]. In this work, the steep switching characteristic of a p-type NC FinFET (which electrically integrates a 6-nm-thick Zr-doped HfZrO ferroelectric capacitor in its gate stack) is demonstrated. The performance of the NC FinFET is compared to that of a conventional FinFET. Furthermore, repetitive steep switching characteristic of the NC FinFET is clearly observed at various drain voltages (V_{DS}).

II. DEVICE DESIGN AND FABRICATION PROCESS

Figure 2 shows the brief fabrication process flow and the measured capacitance-voltage (*C–V*) of a standalone HfZrO ferroelectric capacitor. First, 1000 Å TiN was prepared/deposited as the bottom electrode of the ferroelectric capacitor. Subsequently, an HfZrO layer was deposited on top of the TiN layer via the atomic layer deposition (ALD) technique (which is used for Zr doping). Consequently, a 60-Å-thick HfZrO layer was obtained with a uniformity of approximately 1 %. Subsequently, a 500-Å-thick TiN layer was deposited as the top electrode. In the patterning process, a Ti/Pt (100 Å / 300 Å) layer was formed via e-beam evaporation. Subsequently, a TiN layer was etched at 85 °C for 5 min. Finally, the ferroelectric layer was annealed via the rapid thermal annealing (RTA) process for 30 s at 500 °C. The area of the fabricated HfZrO capacitor was 4.9×10^{-5} cm^2, and the maximum capacitance value was approximately 45 pF. The measured *C–V* curve of the fabricated HfZrO capacitor shows a typical ferroelectric characteristic, and the coercive voltages of capacitor were 0.5 V and -0.5 V.

In order to design the NC FinFET structure, the bottom contact (TiN) of the HfZrO capacitor was electrically connected to the gate of the FinFET with a gold wire of purity approximately 99.99 %. The physical device dimensions of the FinFET were as follows: gate length, fin width, fin height, the number of fins, fin pitch, oxide thickness, and source/drain extension length were 90 nm, 10 nm, 40 nm, 5, 200 nm, 1.4 nm, and 90 nm, respectively. The bird's-eye view and capacitive network of the NC FinFET are shown in Fig. 1. In order to measure the input transfer characteristic of the NC FinFET, the probe for the gate was connected to the top contact of the HfZrO capacitor, and the probe for the source/drain was connected to the source/drain of the FinFET. The internal voltage (V_{int}) was directly measured at the node between the bottom contact of the HfZrO capacitor and the gate electrode of the FinFET device. Note that Keithley 4200A-SCS was used to measure the device performance.

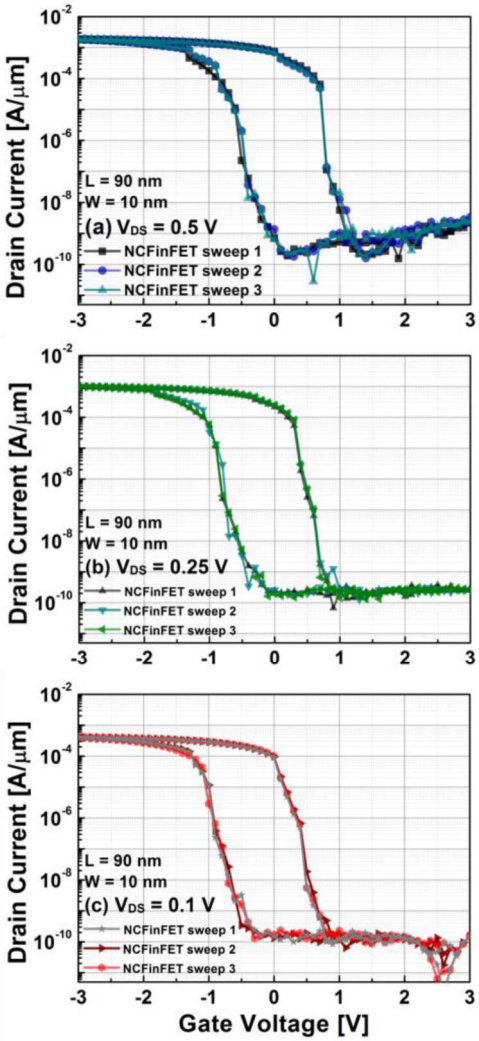

FIGURE 4. **Measured input transfer characteristics of NC FinFET for (a) V_{DS} = 0.5 V, (b) V_{DS} = 0.25 V, (c) V_{DS} = 0.1 V.**

III. RESULTS AND DISCUSSION

Figure 3 shows the measured input transfer characteristic of the FinFET and NC FinFET at V_{DS} of 0.5 V. Owing to the NC effect of the HfZrO ferroelectric capacitor, the steep switching characteristic and hysteresis are observed together. Notably, the drain current was normalized to the effective width (i.e., 2 × fin height + fin width) of the FinFET. Specifically, the device performance parameters of the NC FinFET and FinFET are compared and summarized in Table 1. In order to fairly compare the on-current (I_{ON}) and off-current (I_{OFF}), I_{OFF} was fixed at approximately 2×10^{-10} A/μm. Subsequently, I_{ON} (i.e., the drain current at V_G = -1 V) of the FinFET and NC FinFET were measured as 3.48×10^{-4} A/μm and 3.09×10^{-4} A/μm, respectively. SS_{min} indicates the minimum subthreshold slope, and SS_{avg} indicates the average SS in the range of drain current from I_{OFF} to 1×10^{-4} A/μm. SS_{min} of the NC FinFET is lower than that of the FinFETs, since the NC effect induces a step-up internal voltage amplification. However, SS_{avg} of the NC FinFET was higher than that of the FinFET at forward biasing sweep because the amount of voltage amplification at forward sweep was smaller than that at reverse sweep. Figure 4 shows the repetitive measurement results of the input transfer characteristics of the NC FinFET at various drain voltages. It is confirmed that steep switching occurs in every sweeping cycle. Based on these experimental results, the steep switching characteristic and negligible threshold voltage variation of the NC FinFET with an HfZrO ferroelectric capacitor were confirmed. However, for the NC FinFET with an HfZrO capacitor to be adopted in CMOS logic circuits, there are various barriers to be overcome such as the removal of hysteresis and the boosting of I_{ON}.

TABLE 1. **Comparison of device performance parameters (NC FinFET vs. FinFET).**

Parameters	NC FinFET	FinFET
On current, I_{ON} [$\times 10^{-4}$ A/μm]	3.09	3.48
Off current, I_{OFF} [$\times 10^{-10}$ A/μm]	2.20	1.92
I_{ON}/I_{OFF} [$\times 10^{6}$]	1.40	1.81
Reverse sweep SS_{avg} [mV/decade]	109.79	127.93
Forward sweep SS_{avg} [mV/decade]	151.09	137.69
Reverse sweep SS_{min} [mV/decade]	36.31	86.16
Forward sweep SS_{min} [mV/decade]	58.86	75.97

IV. CONCLUSION

By utilizing the NC effect in a ferroelectric material, the sub-threshold slope of conventional devices (e.g., planar bulk MOSFET, FinFET) can be effectively reduced below 60 mV/decade at 300 K owing to the internal voltage amplification. However, typical ferroelectric materials such as PZT or BFO are not appropriate in terms of CMOS compatibility; for instance, the thickness of the ferroelectric layer should be <10 nm to be smoothly adopted in the current CMOS gate stack. Therefore, a novel CMOS-compatible sub-10-nm-thick ferroelectric material should be developed, such as doped Hf-based ferroelectric material. In this study, the steep switching characteristic of the NC FinFET with a sub-10-nm-thick HfZrO capacitor was developed and compared with the baseline FinFET. In particular, the minimum subthreshold slope of the NC FinFET was ∼36 mV/decade at 300 K, which indicates that the internal voltage amplification occurring due to the NC effect of the Hf-based ferroelectric layer is sufficient.

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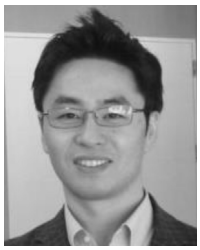

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