Received 30 June 2017; accepted 6 July 2017. Date of publication 21 July 2017; date of current version 23 August 2017.
The review of this paper was arranged by Editor C. C. McAndrew.

Digital Object Identifier 10.1109/JEDS.2017.2725340

An Analytical Model for the Gate C–V Characteristics of UTB III–V-on-Insulator MIS Structure

MUHAMMAD MAINUL ISLAM[1], MD. NUR KUTUBUL ALAM[1], MD. SHAMIM SARKER[1], MD. RAFIQUL ISLAM[1], AND ANISUL HAQUE[2]

1 Department of Electrical and Electronic Engineering, Khulna University of Engineering and Technology, Khulna 9203, Bangladesh
2 Department of Electrical and Electronic Engineering, East West University, Dhaka 1212, Bangladesh

CORRESPONDING AUTHOR: M. N. K. ALAM (e-mail: alamjhilam@gmail.com)

ABSTRACT We propose a physics-based analytical model for gate capacitance-voltage characteristics of ultra-thin-body III–V-on-insulator (XOI) MIS structure. The accuracy of the analytical model is verified by comparing with TCAD results. The model is general and is applicable to different III–V channel materials.

INDEX TERMS Gate capacitance, compact model, XOI, III-V-on-insulator.

I. INTRODUCTION

Scaling of transistor improves cost, speed, and power per function with every new technology generation [1]. As Si CMOS technology approaches the physical limits of scaling, various alternatives are proposed. One of the potential candidates for future nanoscale devices is the so called XOI, compound semiconductor-on-insulator devices [2]. A number of experimental studies have reported excellent performance of XOI devices with only a few nanometer channel thickness [3], [4]. We have recently shown [5] that unlike other MOS devices, such as, bulk Si MOSFET, FINFET or SOI FET, the XOI devices exhibits completely unique C-V characteristics showing staircase like behavior.

C-V models are used for device parameter extraction of MOS devices. Analytical models are necessary for fast and accurate estimation of device characteristics in circuit simulations. Moreover analytical models provide insight into device response when device parameters or excitations are varied. Predictability is an important requirement in an analytical model. Quantum mechanical and other complex physical phenomena determine the characteristics of modern semiconductor devices owing to the nanoscale dimensions and bandgap engineering. Thus empirical models fail to predict the characteristics of such devices. The motivation of this work is to develop a physics based analytical model for the gate C-V characteristics of XOI devices with different channel materials. To demonstrate the generality and the accuracy of the model, we have also calculated the electrostatics of the device by self-consistently solving Schrodinger-Poisson equations using the TCAD tool Silvaco Atlas. Excellent match between analytical results and TCAD simulations have been obtained for two different channel materials. It is to be noted that the TCAD simulation for determining device electrostatics is considered acceptable even for most advanced nanoscale devices [6]–[8].

II. DEVICE STRUCTURE

We developed a general analytical model to express the C-V characteristic of the device structure shown in Fig. 1(a). In order to validate the model against numerical calculation we took 10nm HfO_2 as Front Gate Oxide (FOX) and 50nm SiO_2 as Bottom Gate Oxide (BOX). $In_{0.3}Ga_{0.7}Sb$ or $InAs_{0.7}Sb_{0.3}$ is taken as the channel material. Details of the numerical simulation procedure for the chosen dimensions are available in our previously published paper [5].

III. C-V MODELING

The gate capacitance is expressed by the fundamental relationship

$$C_G = -\frac{dQ_{ch}^{QM}}{dV_G} \tag{1}$$

2168-6734 © 2017 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

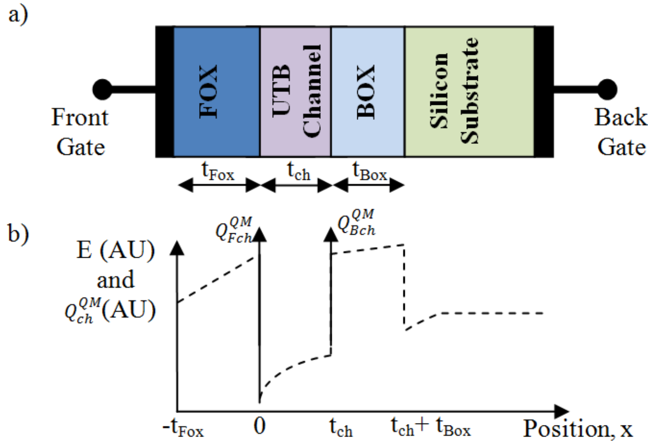

FIGURE 1. Along the thickness of the device- a) Schematic diagram of device and b) Band diagram showing the positions of sheet inversion charges.

Here Q_{ch}^{QM} is the total charge in the channel considering quantum mechanical effects. We neglect the presence of any charge in the substrate region as the buried oxide is relatively thick and the substrate is undoped. For simplicity we assume that the channel charge may be represented by two sheet charges located at FOX-channel interface and BOX-channel interface, respectively. Electron density in the ith quantized state is given by [9]

$$n_i = \frac{4\pi gm^*kT}{h^2}\ln\left[1+e^{(E_F-E_{min})/kT}\right] \tag{2}$$

where g is the number of equivalent minima in conduction band, m^* is the effective mass, k is the Boltzmann constant, h is the Planck's constant, T is the temperature and E_F is the Fermi level. E_{min} is equal to

$$E_{min} = E_C + E_i - q\psi_{ch} \tag{3}$$

where ψ_{ch} is the channel potential, E_i is the ith subband energy, and E_C is the conduction band minima. Therefore the total charge per unit area becomes

$$Q_{ch}^{QM} = -q\frac{4\pi gm^*kT}{h^2}\sum_i ln\left[1+e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}\right] \tag{4}$$

For our device, the depth of the channel quantum well is greater than 4eV. This can be considered as an infinite quantum well even for narrow channel thicknesses, as long as energies only up to the 2nd eigen level are taken into consideration. Thus E_i is calculated using the well known solution for infinite rectangular quantum wells [10]

$$E_i = \frac{n^2\pi^2\hbar^2}{2m^*t_{ch}^2} \tag{5}$$

To buildup the gate voltage dependent gate capacitance relationship, we have to find a correlation between the channel potential and gate voltage. Using Fig. 1(b), integrating the depletion mode Poisson's equation over the channel in the range $0^+ \le x \le t_{ch}^-$, we have,

$$\xi_{Bch} - \xi_{Fch} = \frac{q}{\varepsilon_{ch}}N_D t_{ch} \tag{6}$$

Here N_D is the doping concentration, ε_{ch} is the dielectric constant of the channel material, ξ_{Fch} and ξ_{Bch} are the electric fields of the channel at the FOX-channel interface and channel-BOX interface respectively. Integrating Poisson's equation twice we get

$$\psi_{sf} - \psi_{sb} = \frac{1}{2}\left(\xi_{Fch} + \xi_{Bch}\right)t_{ch} \tag{7}$$

Here ψ_{sf} is the front surface potential and ψ_{sb} is the back surface potential of the channel. Combining (6) and (7) we express the surface electric fields of the channel in terms of the two surface potentials.

$$\xi_{Fch} = \frac{\psi_{sf} - \psi_{sb}}{t_{ch}} - \frac{qN_D}{2\varepsilon_{ch}}t_{ch} \tag{8}$$

Applying Gauss's law at the oxide/channel interfaces, we can relate the electric field inside the FOX (ξ_{Fox}) with ξ_{Fch} while taking the channel charge into consideration. Then using $\xi_{Fox} = (V_{FG} - \phi_{msf} - \psi_{sf})/t_{Fox}$ in the continuity equation, we get

$$\xi_{Fch} = \frac{C_{Fox}}{\varepsilon_{ch}}\left(V_{FG} - \phi_{msf} - \psi_{sf}\right) + \frac{Q_{Fch}^{QM}}{\varepsilon_{ch}} \tag{9}$$

where $C_{Fox} = \varepsilon_{Fox}/t_{Fox}$. Here V_{FG}, ϕ_{msf} and C_{Fox} are the front gate voltage, front gate flat band potential and FOX capacitance, respectively. Similarly, the back surface electric field can be written as

$$\xi_{Bch} = \frac{C_{Box}}{\varepsilon_{ch}}\left(\psi_{sb} - V_{BG} + \phi_{msb}\right) - \frac{Q_{Bch}^{QM}}{\varepsilon_{ch}} \tag{10}$$

where $C_{Box} = \varepsilon_{Box}/t_{Box}$. Here V_{BG}, ϕ_{msb} and C_{Box} are the back gate voltage, back gate flat band potential and BOX capacitance, respectively. V_{FG} maybe expressed as

$$V_{FG} = \phi_{msf} + \psi_{sf} + \frac{\varepsilon_{ch}\left(\psi_{sf} - \psi_{sb}\right)}{C_{Fox}t_{ch}} - \frac{Q_{Fch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Fox}}t_{ch} \tag{11}$$

Similarly, the back gate voltage V_{BG} is given by

$$V_{BG} = \phi_{msb} + \psi_{sb} - \frac{\phi_{ch}\left(\psi_{sf} - \psi_{sb}\right)}{C_{Box}t_{ch}} - \frac{Q_{Bch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Box}}t_{ch} \tag{12}$$

Equations (4), (11) and (12) are coupled to each other through the channel charge. Therefore, these equations cannot be solved exactly independent of one another. At this stage we neglect this coupling for the time being. When $V_{BG} = 0V$, putting $Q_{Bch}^{QM} = 0$ and using (12) we get,

$$\psi_{sb} = \frac{\frac{\varepsilon_{ch}\psi_{sf}}{C_{Box}t_{ch}} + \frac{qN_D}{2C_{Box}}t_{ch} - \phi_{msb}}{1 + \frac{\varepsilon_{ch}}{C_{Box}t_{ch}}} \tag{13}$$

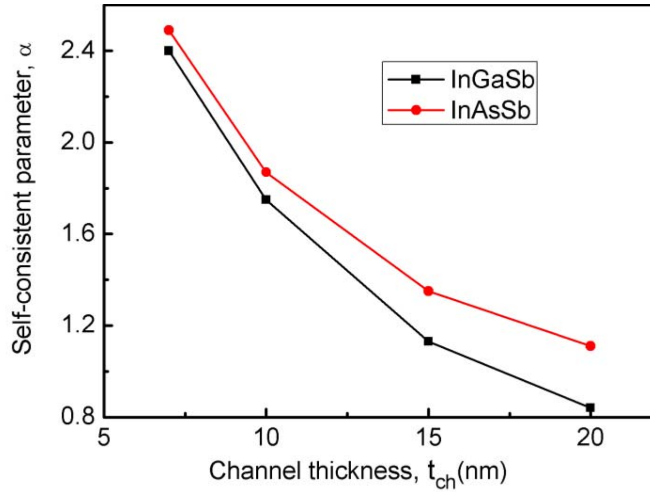

FIGURE 2. Variation of the self-consistent parameter, α as a function of channel thickness.

Putting this value into (11) we get

$$V_G = V_{FG} = \phi_{msf} + \psi_{sf} + \frac{\varepsilon_{ch}\psi_{sf}}{C_{Fox}t_{ch}} - \frac{\varepsilon_{ch}}{C_{Fox}t_{ch}}\left(\frac{\frac{\varepsilon_{ch}\psi_{sf}}{C_{Box}t_{ch}} + \frac{qN_D}{2C_{Box}}t_{ch} - \phi_{msb}}{1 + \frac{\varepsilon_{ch}}{C_{Box}t_{ch}}}\right) - \frac{Q_{Fch}^{QM}}{C_{Fox}} - \frac{qN_D}{2C_{Fox}}t_{ch} + \psi_{SCF} \quad (14)$$

Note that a self-consistent potential $\psi_{SCF}=\alpha Q_{Fch}^{QM}/C_{ch}$ is added on the right hand side of (14), to balance the two sides by offsetting the error induced due to neglecting the coupling of potential equations with the channel charges. Here $C_{ch} = \varepsilon_{ch}/t_{ch}$, and α is a self-consistent parameter. Value of α is determined from a comparison between results obtained from analytical calculation and numerical simulation using Silvaco Atlas simulator. As the value depends on the channel material as well as on the thickness of the channel, α must be calibrated for each particular device technology by comparing with either TCAD or experimental results. Note that its value does not have any dependency on the doping concentration. Fig. 2 shows the value of α for InGaSb and InAsSb at different channel thicknesses.

For a particular gate voltage, as all other parameters of (14) are known, we can solve for ψ_{sf} iteratively. As V_{BG} is set to 0V, we can write $\psi_{ch} = \psi_{sf}$. Then using (4), we have calculated the channel charge considering two subbands. The capacitance is then calculated by differentiating the charge equation with respect to gate voltage.

Fig. 3(a) shows the variation of channel charge with the channel potential in both linear and logarithmic scale. At increased channel potential, higher eigen states start to populate which in turn increases the slope. The change in channel potential with gate voltage – flatband voltage is also shown in Fig. 3(b).

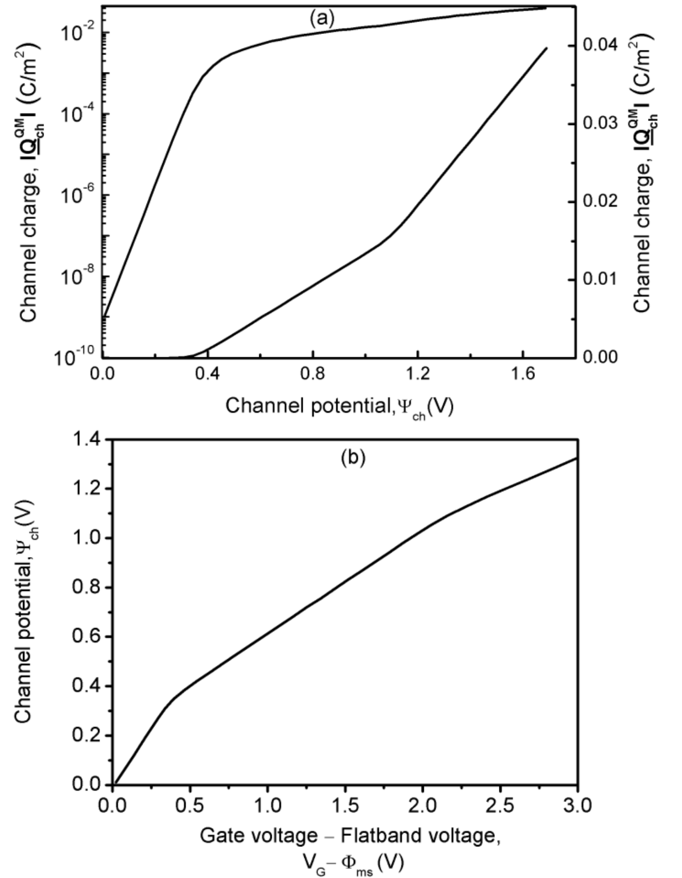

FIGURE 3. (a) Channel charge versus channel potential and (b) Channel potential versus gate voltage–flatband voltage curve of 7nm $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET.

IV. VALIDATION OF MODEL

Results obtained from the analytical model are compared with the TCAD (Silvaco Atlas) results for a single gate $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET. The back gate potential, V_{BG} is set to 0V and $\psi_{ch} = \psi_{sf}$. Differentiating (4) and (14), the gate capacitance can be expressed as

$$C_G = \frac{\frac{4\pi gm^*q^2}{h^2}\sum_i \frac{e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}{1+e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}}{1 + \frac{\varepsilon_{ch}}{t_{ch}C_{Fox}}\left(1 - \frac{\varepsilon_{ch}}{\phi_{ch}+t_{ch}C_{Box}}\right) - \left(\frac{1}{C_{Fox}} - \frac{\alpha}{C_{ch}}\right)\frac{4\pi gm^*q^2}{h^2}\sum_i \frac{e^{(E_F-E_C+q\psi_{ch}-E_i)/kT}}{1+e^{(E_F-E_C+q\psi_{ch}-E_i)}\big/kT}} \quad (15)$$

As shown in Fig. 4(a), the results obtained from the analytical model and the numerical analysis show excellent agreement for 7nm and 10nm channel thicknesses in devices with $In_{0.3}Ga_{0.7}Sb$ channel. But for 15nm and 20nm channel thicknesses the analytical model is not as accurate although the analytical model captures the essential physics. It is due to the fact that in analytical calculation, we model the channel charge as sheet charges localized at the oxide-channel interface. But in numerical calculation it is distributed along the thickness of the channel and therefore centroid of the charge gets shifted from the interface.

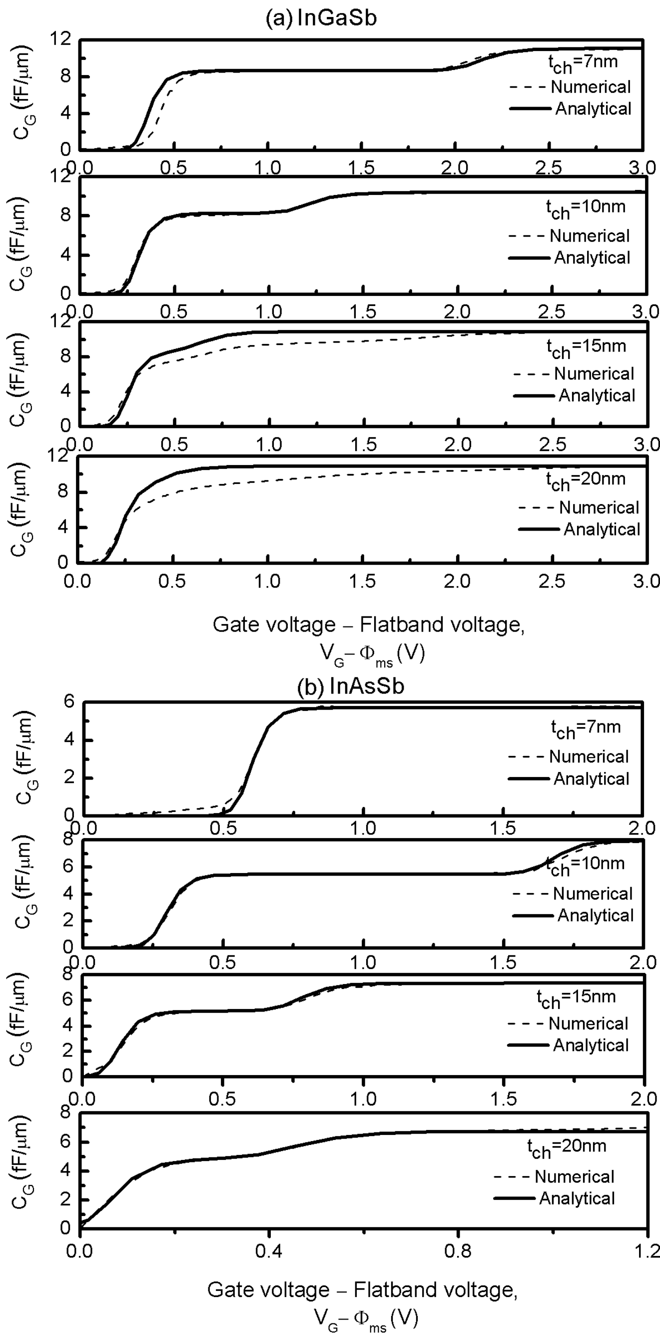

FIGURE 4. Comparison between analytical (solid lines) and numerical (dotted lines) results (a) $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET and (b) $InAs_{0.7}Sb_{0.3}$-on-Insulator FET at different channel thicknesses.

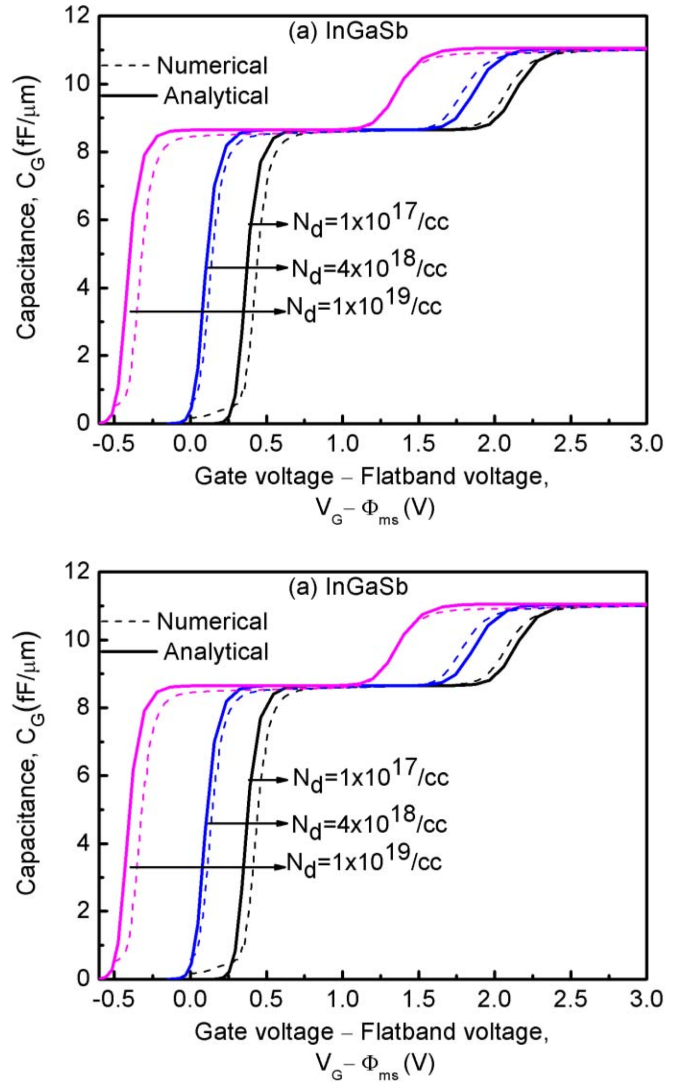

FIGURE 5. Comparison between analytical (solid lines) and numerical (dotted lines) results (a) $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET and (b) $InAs_{0.7}Sb_{0.3}$-on-Insulator FET at different doping concentration.

In order to confirm the generality of the model, it is verified for a device with $InAs_{0.7}Sb_{0.3}$ channel material. We found excellent match as shown in Fig. 4(b) for all four channel thicknesses. The result between InGaSb and InAsSb varied due to difference in effective masses, permittivities and the eigen energies of the channel material. Also, the bandgap, intrinsic carrier concentration and composition of the materials are also responsible for such variations. The model is also validated for different doping concentrations of 7nm $In_{0.3}Ga_{0.7}Sb$-on-Insulator FET and 10nm $InAs_{0.7}Sb_{0.3}$-on-Insulator FET which is shown in Fig. 5(a) and 5(b), respectively. The numerical and analytical results are found to be in an excellent agreement.

V. CONCLUSION

We have presented a physics based analytical model for gate C-V characteristics of ultra-scaled XOI FET. To investigate the accuracy of the model, we have compared analytical results with numerical calculations from Silvaco Atlas for two different channel materials with a variety of channel thicknesses and doping concentrations. Except for the channel thicknesses greater than 15 nm with the InGaSb channel, the quantitative agreement between the model and the TCAD results are excellent.

REFERENCES

[1] (2015). *The International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs.net/Links/2015ITRS/Home2015.htm
[2] H. Ko *et al.*, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature*, vol. 468, no. 7321, pp. 286–289, Nov. 2010.
[3] H. Fang *et al.*, "Ultrathin-body high-mobility InAsSb-on-insulator field-effect transistors," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 504–506, Apr. 2012.
[4] S. Kim *et al.*, "Sub-60-nm extremely thin body InxGa1-xAs-on-insulator MOSFETs on Si with Ni-InGaAs metal S/D and MOS interface buffer engineering and its scalability," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2512–2517, Aug. 2013.
[5] M. N. K. Alam, M. S. Islam, M. G. Kibria, and M. R. Islam, "Anomalous staircase CV characteristics of InGaSb-on-insulator FET," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3910–3913, Nov. 2014.
[6] J. Lin, L. Czornomaz, N. Diax, D. A. Antoniadis, and J. A. del Alamo, "Ultrathin body InGaAs MOSFETs on III-V-on-insulator integrated with silicon active substrate (III-V-OIAS)," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3088–3095, Aug. 2016.
[7] J.-S. Yoon, K. Kim, T. Rim, and C.-K. Baek, "Performance and variations induced by single interface trap of nanowire FETs at 7-nm node," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 339–345, Feb. 2017.
[8] P. Banerjee and S. K. Sarkar, "3-D analytical modeling of dual-material triple-gate silicon-on-nothing MOSFET," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 368–375, Feb. 2017.
[9] F. Stern, "Self-consistent results for n-type si inversion layers," *Phys. Rev. B, Condens. Matter*, vol. 5, no. 12, pp. 4891–4899, Jun. 1972.
[10] B. H. Bransden and C. J. Joachain, *Quantum Mechanics*, 2nd ed. Harlow, U.K.: Prentice-Hall, 2000.

MUHAMMAD MAINUL ISLAM received the B.Sc. and M.Sc. degrees in electrical and electronic engineering from the Khulna University of Engineering and Technology, Khulna, Bangladesh, in 2013 and 2017, respectively, where he is currently a Faculty Member with the Department of Electrical and Electronic Engineering. His research interests include low power electronic devices and nanotechnology.

MD. NUR KUTUBUL ALAM received the B.Sc. and M.Sc. degrees in electrical and electronic engineering from the Khulna University of Engineering and Technology (KUET), Khulna, Bangladesh, in 2012 and 2015, respectively, where he is currently a Faculty Member with the Department of Electrical and Electronic Engineering. His present research interests include low power electronic devices and nanotechnology. He was a recipient of the Academic Gold Medal from KUET.

MD. SHAMIM SARKER received the B.Sc. and M.Sc. degrees in electrical and electronic engineering from the Khulna University of Engineering and Technology, Khulna, Bangladesh, in 2013 and 2017, respectively, where he is currently a Faculty Member with the Department of Electrical and Electronic Engineering. His present research interests include 2-D electronic devices and integrated circuit design.

MD. RAFIQUL ISLAM received the B.Sc. degree in EEE from the Khulna University of Engineering and Technology (KUET), in 1991, the M.Sc. degree in EEE from the Bangladesh University of Engineering and Technology in 1998, and the D.Eng. degree from the Kyoto Institute of Technology, Japan, in 2004. He is currently a Professor with the Department of EEE, KUET. His current research interests are modeling and simulation of low dimension electronic and opto-electronic devices and optical communications.

ANISUL HAQUE has been a Professor with the Department of Electrical and Electronic Engineering, East West University, since 2006. He was with the Electrical and Electronic Engineering Department, BUET, as a Faculty Member for eighteen years. He has been a Visiting Faculty with the Tokyo Institute of Technology, Japan, the University of Connecticut, USA, and Clarkson University, USA. His research interests include the physics, modeling, simulation, and characterization of nanoelectronic devices and photovoltaic devices and systems. He is also interested in engineering education. He serves on the Board of Accreditation for Engineering and Technical Education and is a member of the Institute of Engineers, Bangladesh. He was a recipient of the Bangladesh University Grants Commission Award in 2006 and the Gold Medal from the Bangladesh Academy of Science in 2010. He is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES and an Associate Editor of IEEE ACCESS. He has been serving as an IEEE Distinguished Lecturer since 2009.