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# Design and Application of Virtual Inductance of Square-Shaped Defected Ground Structure in 0.18-$\mu$m CMOS Technology

**NUSRAT JAHAN[1], SITI AMALINA ENCHE AB RAHIM[1], ADEL BARAKAT[1,2] (Member, IEEE), TAKANA KAHO[1,3] (Member, IEEE), AND RAMESH K. POKHAREL[1] (Member, IEEE)**

1 Faculty of Information Science and Electrical Engineering, Kyushu University, Fukuoka 8190395, Japan
2 Microstrip Circuits Department, Electronics Research Institute, Giza 12622, Egypt
3 NTT Network Innovation Laboratories, Yokosuka 239-0847, Japan

CORRESPONDING AUTHOR: N. JAHAN (e-mail: 3IE16609S@s.kyushu-u.ac.jp)

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**ABSTRACT** This paper investigates a possibility of application of a virtual inductor realized by an integrated defected ground structure (DGS) to design a front-end circuit in CMOS technology. Two types of DGS are analyzed and found that the inductance realized by a square-shaped DGS achieves smaller size and higher quality factor than an H-shaped DGS. Then, a 15-GHz low phase noise voltage-controlled oscillator (VCO) employing the proposed square-shaped DGS in 0.18-$\mu$m 1P6M CMOS technology is designed. The fabricated VCO operates from 15.2 to 16.12 GHz and consumes 5-mW power. The measured phase noise is -132.08 dBc/Hz at 10-MHz offset frequency, and this results in the figure of merit (FoM) and FoM taking account of the area to be 189.1 and 199.9 dB, respectively.

**INDEX TERMS** Integrated DGS resonator, *K*u-band oscillator, phase noise, CMOS technology.

## I. INTRODUCTION

Ahigh quality ($Q$-) factor resonator or an inductor is challenging to realize in Complementary-Metal-Oxide-Semiconductor (CMOS) technology, yet an essential component for microwave and millimeter-wave front-end circuits [1]. Therefore, a lot of research has been carried out to improve $Q$-factor of a spiral inductor which is indispensable to design matching circuits, oscillators, amplifiers and so on [2]–[5]. For example, the use of high resistivity substrate [2], proton bombardment techniques [3], helium bombardment techniques [4], and substrate removal by post micromachining [5] were proposed. In [2], Kim *et al.* used 8 copper metal layers process and high resistivity substrate to boost inductor Q-factor by at least 50% by reducing substrate losses. The main drawback with this high resistivity substrate method [2] is that the self-resonant frequency of an on-chip inductor decreases due to the increasing capacitance between the bottom metal layer and the substrate. Lee *et al.* [3], used high-energy protons to create a local semi-insulating silicon region for device isolation and realization of high-Q IC inductors. Similarly, in [4], helium-3 ion bombardment technique was used to create semi-insulating substrate areas, which in return improves the inductor Q- factor by 38%. Later, this inductor was applied to an 8-GHz oscillator, and an 8.5 dB improvement in the phase noise had been achieved. One of the main problems with this bombardment technique [3], [4] is that it requires an enormous amount of dose which results in less reliability as well as less feasibility. In [5], inductor was fabricated on both Si and glass wafer using surface micromachining which increases inductor Q- factor almost by 50%. However, all of them require complicated post-processing of the CMOS wafer which may increase the cost. Furthermore, the patterned ground shield was proposed in [6] to reduce the substrate loss. In that method, a ground plane with slots is inserted between the inductor and the

substrate, preventing the electrical field entering from the substrate.

A defected ground structure (DGS) etched on the ground plane of a substrate below a microstrip line (MSL) interrupts the electromagnetic (EM) fields resulting in a notch at a certain frequency [7], and this results in a virtual inductor of high quality ($Q$-) factor. The application of DGS has been exploited in microwave and millimeter wave passive circuits such as the wireless power transfer system [7], band pass filters [8], antenna [9], and so on [10]. In addition, DGS was exploited to design a high-performance voltage-controlled oscillator (VCO) on PCB with discrete transistors [11]. However, the application of an integrated DGS as an inductor or a resonator to design a CMOS front-end circuit such as a voltage-controlled oscillator (VCO) has not been reported yet.

In this manuscript, we first propose a new DGS structure to realize a high Q-factor inductor in 0.18 $\mu$m CMOS technology and employed it to design a low phase-noise Ku-band VCO. The proposed design offers following advantages: (i) the DGS is etched on the ground plane (M1) below MSL on the top layer (M6), so that the resources on top layer (M6) above the DGS could be used for future design of other system circuit components, and (ii) a smaller size of the chip die area makes the VCO ease of implementation to the advanced CMOS technology, and (iii) The DGS could be fabricated by a standard CMOS process and does not require an additional post-processing method so that no additional cost is required unlikely in [2]–[5].

## II. PROPOSED SQUARE-SHAPE DGS RESONATOR, INDUCTANCE, AND Q-FACTOR

When an MSL excites DGS etched on a ground plane, fields are interrupted resulting in a notch at a certain frequency [6], and this results in a virtual series inductor. To investigate this, two types of DGS on 1-poly 6-metal (1P6M) 0.18 $\mu$m CMOS technology as shown in Fig. 1 is analyzed, where H-shape DGS which are usually used in wireless power transfer system [7] and BPF design [8], is shown in Fig. 1(a) with current distribution. As shown, an H-shape DGS consists of two current loops in parallel which makes the equivalent inductance ($L_{EQ}$) of the DGS to be half of the inductance of each loop so that the unloaded $Q$-factor will worsen. To mitigate this problem, we propose a square-shaped DGS as shown in Fig. 1(b) where H-shape DGS is first halved and then area of the square-shaped DGS is made equal to the original H-shape DGS. As shown, the proposed square-shape DGS has only one current loop, and $L_{EQ}$ will be the same as the inductance of each loop of an H-shape DGS.

In the layout of Fig. 1, the white area is the etched DGS implemented on the M1 layer of 0.18 $\mu$m CMOS technology, and a 50Ω MSL on M6 excites the DGS through a capacitive coupling which is also called an excitation gap. The excitation gap has dimensions of $g \times k$ for both DGSs.

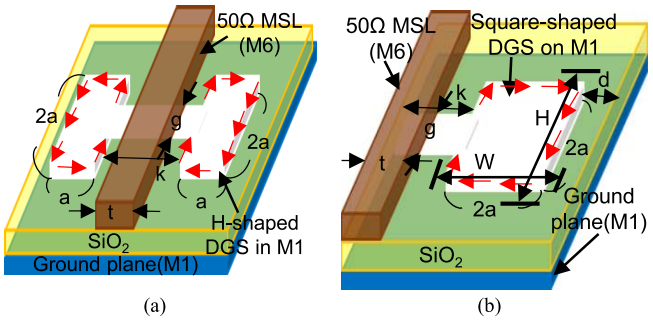


**FIGURE 1.** The current distribution of two types of DGS in 0.18 $\mu$m CMOS technology. (a) Conventional H-shape DGS. (b) Proposed square-shape DGS.

High Frequency Structure Simulator (HFSS) by ANSYS Inc. is employed to simulate both models of the DGS resonator. A lumped port is inserted into the excitation gap of both DGS to calculate the unloaded $Q$-factor ($Q_U$). Then, the self-inductance ($L_{EQ}$), resistance ($R_{EQ}$), and $Q_U$ are calculated by,

$$L_{EQ} = Im\,(Z_{11})\,/\omega \qquad R_{EQ} = Re\,(Z_{11})$$
$$Q_U = Im\,(Z_{11})\,/Re\,(Z_{11}) \tag{1}$$

where $\omega = 2\pi f$ is the angular frequency, and $f$ is the frequency. $R_{EQ}$ is the total losses resulting from the conduction losses and the dielectric losses of the substrate. While $L_{EQ}$ results from the magnetic current following through the DGS. Fig. 2 shows the comparison of computed $L_{EQ}$, $R_{EQ}$ and $Q_U$ of both DGS. The proposed square-shape DGS resonator has a higher inductance and the unloaded $Q$-factor ($Q_U$) than that of a conventional H-shape DGS. In conventional DGS like in antenna or filter, DGS with coupled structure is used to improve coupling whether by narrowing bandwidth or by improving insertion loss [7]–[9]. In our VCO design, DGS is used as an inductor. Then extra capacitor is added to resonate at targeted frequency band. And the equivalent circuit becomes parallel LC circuit which will act as band stop filter (BSF). In the design, the 50Ω MSL is used only for the field excitation, whereas the values of $L_{DGS}$, $R_{DGS}$, and $C_{DGS}$ depend on the size of the DGS.

**TABLE 1.** Design parameters of square-shape DGS resonator.

| Parameters | $a$ | $t$ | $k$ | $H$ | $W$ | $d$ | $g$ |
|---|---|---|---|---|---|---|---|
| Dimension (μm) | 15 | 14 | 25 | 50 | 50 | 20 | 10 |

We designed the square-shaped DGS as shown in fig. 1(b), as BSF on Si substrate with $\varepsilon_r = 4$, thickness 200$\mu$m and metal thickness h = 0.53$\mu$m. We summarize the optimized dimension of the square-shaped DGS in Table 1. After that, using quasi-static modeling [15], we extracted a circuit

model for the square-shaped DGS resonator.

$$L_{DGS} = e\,(W+H)\left(0.0234\left[\begin{array}{c} log\left(\frac{2WH}{h+d}e\right) - \frac{W}{W+H} \\ \times log\left[\left(W+\sqrt{W^2+H^2}\right)e\right] - \frac{H}{W+H} \\ \times log\left[\left(H+\sqrt{W^2+H^2}\right)e\right] \end{array}\right] + 0.01\left[\begin{array}{c} 2\left(\frac{\sqrt{W^2+H^2}}{W+H}\right) - 0.5 \\ +0.447\left(\frac{h+d}{W+H}\right) \end{array}\right]\right) nH$$

$$e = 39.37 \tag{2}$$

$$C_{DGS} = \frac{2k}{\pi}\varepsilon_0\varepsilon_{reff}\cosh^{-1}\left(\frac{2a}{g}\right)F \tag{3}$$

$$\epsilon_{reff} = \frac{\varepsilon_r+1}{2} \qquad R_{DGS} = R_{dc} + R_{ac}\Omega$$

$$R_{dc} = \frac{2(W+H)}{\sigma\, dh}$$

$$R_{ac} = \frac{(W+H)}{d+h}\sqrt{\frac{\pi f\mu}{\sigma}} \tag{4}$$

As can be seen in Fig. 1(b), the extracted equivalent circuit includes inductance $L_{DGS}$ due to the square loop of length H, width W, and thickness d. In addition, the equivalent circuit comprises capacitance $C_{DGS}$ due to the slot of length, $g$ and width, $k$. The equivalent circuit of the square-shaped DGS resonator is extracted from its physical dimensions where the inductance $L_{DGS}$ is calculated as (2), the slot capacitance $C_{DGS}$ as (3) [7], and the resistance as (4). By substituting with the calculated design parameters from Table 1 into (2)–(4) we get the following equivalent circuit parameters $L_{DGS} = 0.099$ nH, $R_{DGS} = 0.39\Omega$, and $C_{DGS} = 1.9$ fF which are in good agreement of EM simulations as shown in Fig. 2(a) and (b), respectively.

## III. FIELD DISTRIBUTION AND POSSIBILITY OF AREA REUSE ON TOP LAYER ABOVE DGS

In the case of a spiral inductor, the area on the top layer in the vicinity cannot be re-used. To investigate the possibility of area reuse in the event of a DGS resonator, electric ($E$-) and magnetic ($H$-) fields on the top layer are simulated and compared in Figs. 3 and 4, respectively. Fig. 3 shows the $E$-field distribution on the top layer with and without the proposed DGS. The E-field in Fig. 3(a) remains focused below an MSL in a similar way without the DGS in Fig. 3(b), and there is not much effect in the vicinity of MSL. However, the fields very close to the MSL are affected. Fig. 4 shows the $H$-field distribution in the similar condition, where likely in $E$-field distribution, the effect of the proposed DGS on the H-field distribution is minimum. As with DGS structure, the design worked as band stop filter (BSF), the E- and H- fields are suddenly terminated around half height of the MSL. Moreover, E- and H- fields simulation have been done by placing M1 to M6 above the DGS area, and results show that the characteristics of the square-shaped DGS are merely affected. This opens up a possibility of area-reuse on top layer above DGS to design other system components without affecting the DGS characteristics. The area-reuse will reduce overall chip size and fabrication cost whereas this could not be possible in case of a spiral inductor.

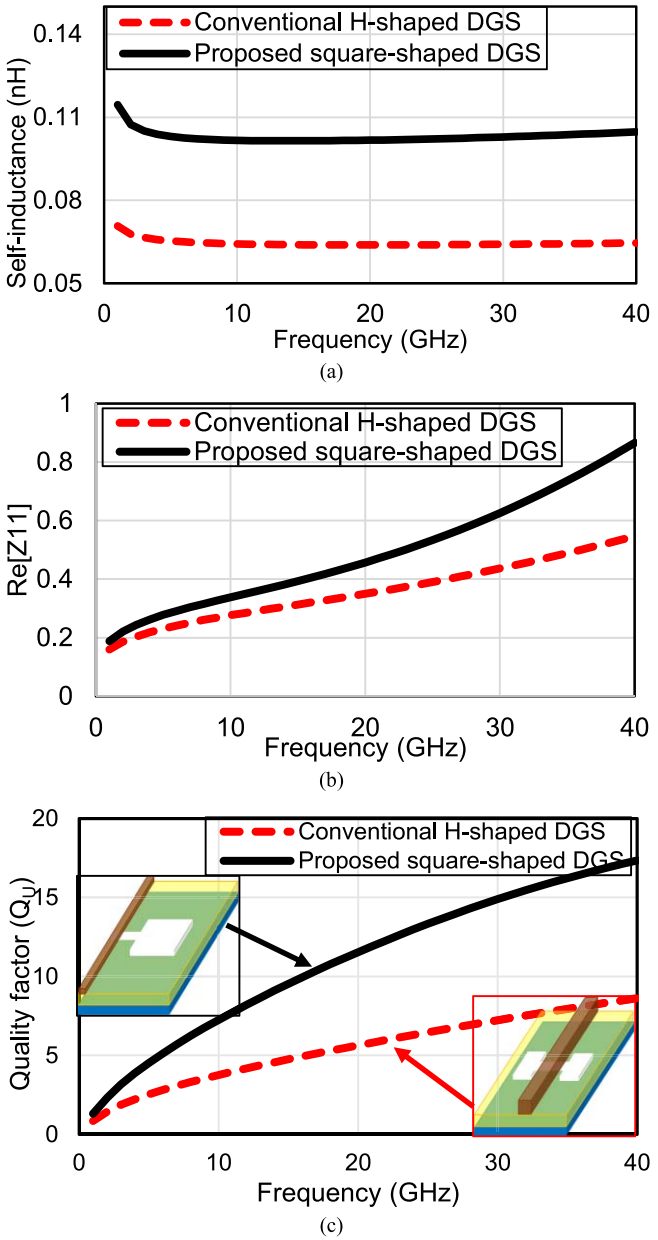


**FIGURE 2. Comparison of (a) self-inductance ($L_{EQ}$) between Square shape and H-shape DGS (b) computed resistance $R_{EQ}$ (c) unloaded Q-factor ($Q_U$).**

## IV. IMPLEMENTATION OF DGS INDUCTOR TO DESIGN A VCO

To prove the concept of DGS resonator, a simple cross-coupled topology as shown in Fig. 5 is designed. PMOS ($T_1$, $T_2$) and NMOS ($T_3$, $T_4$) are cross-coupled pairs, which generate negative resistance ($Z_{IN}$) to cancel the losses of the DGS resonator.

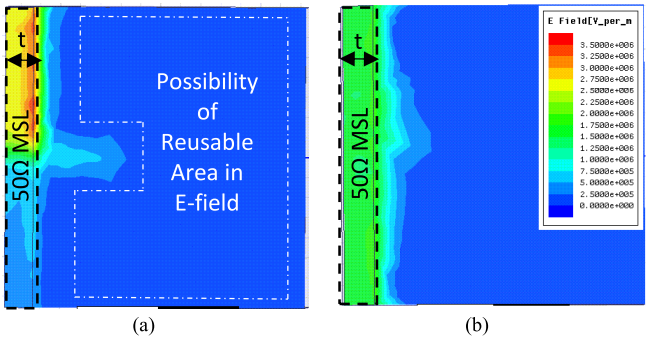


**FIGURE 3.** E-field distribution (a) With DGS (b) Without DGS.

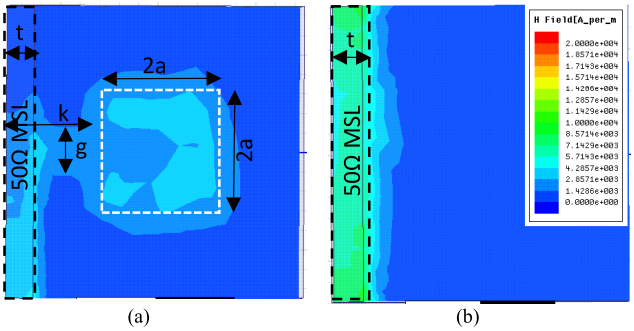


**FIGURE 4.** H-field distribution (a) With DGS (b) Without DGS.

At resonance, the DGS can be represented as a parallel LC circuit shown in Fig. 5. In the first half period of the oscillation, the transistor T1 and T4 are ON, T2 and T3 are OFF, the current through the DGS resonator from left to right, in these second half period is opposite, the current through the DGS resonator from right to left. The equivalent capacitor ($C_{EQ}$) is contributed by cross-coupled transistors.

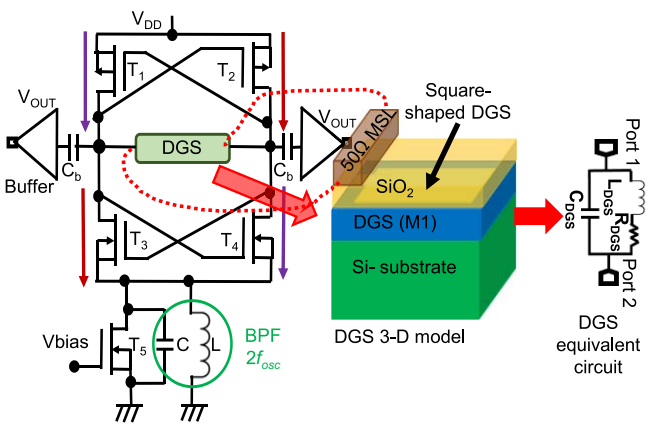


**FIGURE 5.** Implemented cross-coupled VCO with an integrated DGS resonator.

The simplified equivalent circuit of the VCO with DGS resonator is shown in Fig. 6. Generated negative resistance ($Z_{IN}$) and oscillation frequency of the VCO ($f_{OSC}$) can be

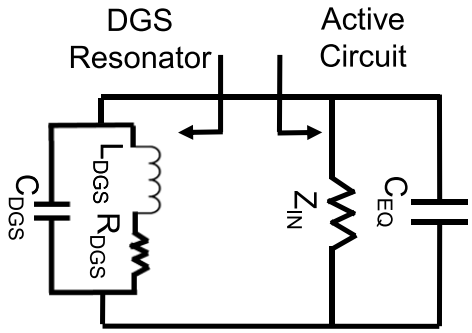


**FIGURE 6.** Simplified VCO equivalent circuit (between DGS and Active circuit).

calculated using (5).

$$Z_{IN} = -\frac{2}{g_{mn} + g_{mp}}$$
$$f_{OSC} = 1/2\pi\sqrt{\left(L_{DGS} \times \left(C_{DGS} + C_{EQ}\right)\right)} \quad (5)$$

where $g_{mn}$ is the transconductance of the NMOS transistors, $g_{mp}$ is the transconductance of the PMOS transistors.

To verify the design, we implemented VCO in both Cadence and Agilent ADS. The scattering parameters (S-parameter) and the impedance parameters (Z-parameter) are obtained after EM simulation by the commercial High Frequency Structure Simulation (HFSS) 13.0 from the Ansoft Corporation. The simulated time domain response for $f_{OSC}$ = 15.83 GHz is shown in Fig. 7.

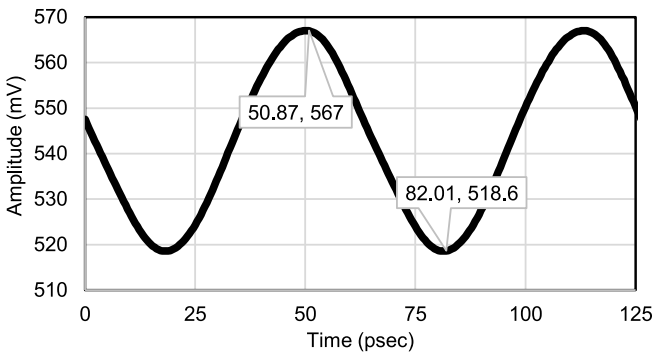


**FIGURE 7.** Simulated time domain response for $f_{OSC}$ = 15.83 GHz.

The comparison of the simulated phase noise for $f_{OSC}$ =15.83GHz is shown in Fig. 8. Use of DGS resonator in oscillator can reduce phase noise by 5 dB compared with the conventional TSMC inductor ($L$ = 281.2pH) and capacitor ($C$ = 31fF). The lower tail components ($L$, $C$, and T5) form a filtered current source [16] and $2\omega_{OSC}$ band pass filter (BPF), to improve phase noise performance of the oscillator. A source inductor and a capacitor in parallel are therefore used to resonate the parasitic of the source node at $2f_{OSC}$. This filtering technique improves phase noise by 2.7 dB.

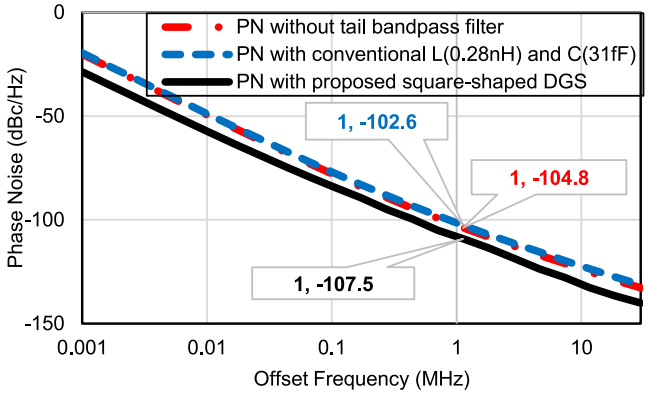


**FIGURE 8.** **Simulated phase noise (*PN*) comparison for $f_{OSC}$ = 15.83*GHz* using conventional inductor, without tail bandpass filter and square-shape DGS.**

## V. FABRICATION, MEASUREMENT, AND COMPARISON

The designed VCO with an integrated DGS resonator was implemented in 0.18 $\mu$m 1P6M CMOS technology. Fig. 9 shows the chip photo of the proposed VCO with square-shaped DGS. The VCO core occupies an area of 440 $\mu$m $\times$190 $\mu$m. While, the total area including the RF and DC measurement pads is 600 $\mu$m $\times$ 600 $\mu$m. The measurements are performed with a probe station using on-wafer probing with Infinity RF and Quadrant DC probes from Cascade Microtech. The pads on the left side are the RF infinity probe for the output signals (G-S-G) from the buffer. The pads on the top are the DC probe (P-G-P-P-G-P), is used for supply and bias voltages. The measured output spectrum and phase noise are shown in Figs. 10(a) and 10(b), respectively. The measurement was performed using a Signal Source Analyzer (ROHDE&SCHWARZ FSUP.SSA, 1166.3505.27).

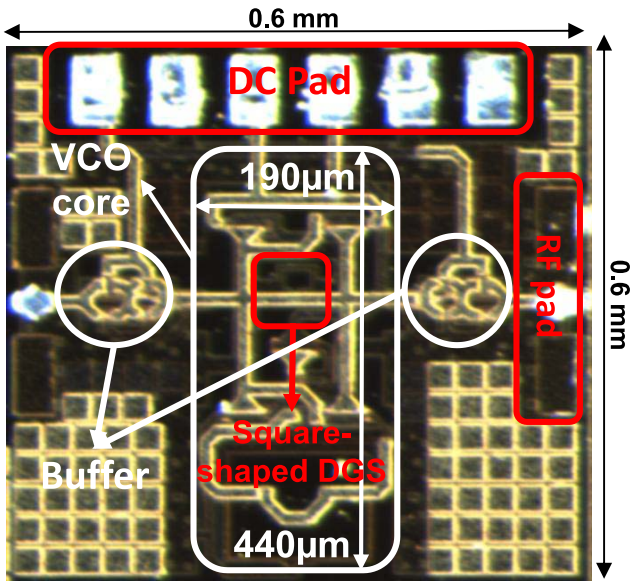


**FIGURE 9.** **Chip photo of the fabricated VCO.**

The measurement shows that the VCO operates from 15.2 GHz to 16. 12 GHz and the phase noise is 132.08 dBc/Hz at 10 MHz offset with the variation of 3.5 dBc/Hz based on the carrier frequency. Fig. 11 shows the measured phase noise at 1MHz and 10MHz offset frequency. The corresponding frequency tuning range (FTR) is 5.88%. The proposed high Q-factor of square-shaped DGS improves phase noise by 1.5dB in comparison with the recently published high-Q spiral inductor [13].

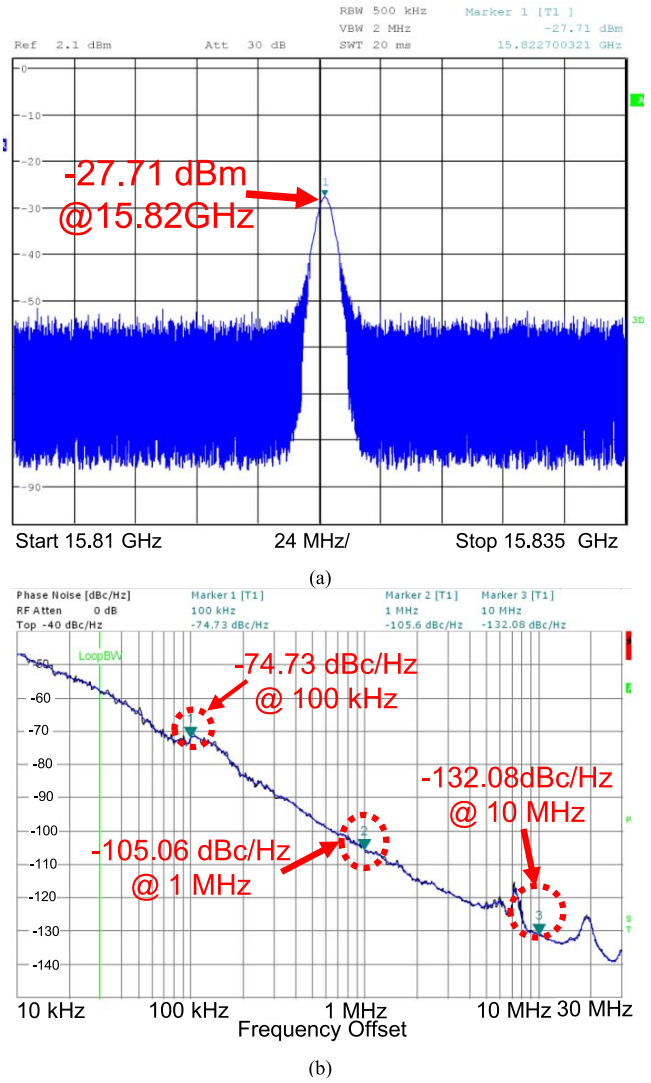


**FIGURE 10.** **The measured result of the VCO (a) Output spectrum at 15.82 GHz (b) phase noise.**

The figure of merit (*FoM*) and the *FoM* considering area ($FoM_A$) are calculated by,

$$FoM = PN + 20log\frac{f_{OSC}}{\Delta f} - 10\log P_{DC}$$
$$FoM_A = FoM - 10\log[A] \quad (6)$$

where PN is the phase noise, $f_{OSC}$ is the oscillation frequency; $\Delta f$ is the offset frequency, $P_{DC}$ is the DC power consumption of mW. And A is the active area in mm$^2$. The DC power consumption is 5mW. The FoM is 189.1 dB. The core area is 0.083 mm$^2$ that results in a $FoM_A$ to be 199.9 dB

which is an improvement of 0. 4 dB and more than 16 dB compared to its counterparts [13], [14], respectively in the same technology. The proposed VCO has the highest $FoM_A$ among the fabricated designs listed in Table 2.

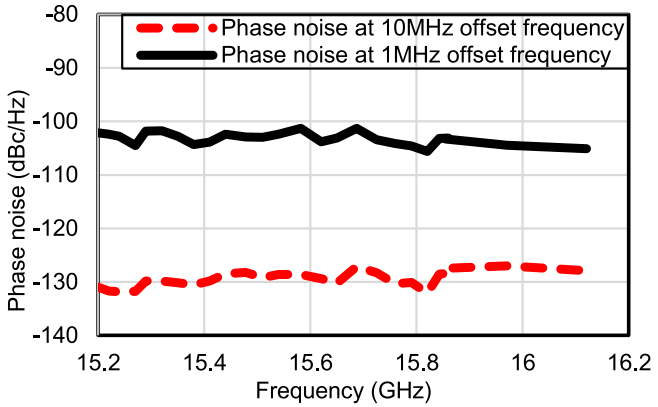


**FIGURE 11.** Measured phase noise with respective oscillation frequency.

**TABLE 2.** Performance comparison of low phase noise VCO.

| Reference | [12] | [13] | [14] | This work |
|---|---|---|---|---|
| $f_{OSC}$ (GHz) | 10.3-11.1 | 14.1-15.1 | 24.27 | 15.2- 16.12 |
| *FTR (%)* | 7.5 | 7.1 | 2.2 | 5.8 |
| Power Dissipation (mW) | 15.8 | 3 | 7.8 | 5 |
| Phase Noise @ 10 MHz (dBc/Hz) | -137 ($f_{OSC}$=10. 58 GHz) | −130.54 ($f_{OSC}$=15.1 2 GHz) | -120 ($f_{OSC}$=24.3 GHz) | -132.08 ($f_{OSC}$=15.82 GHz) |
| Resonating Method | NMOS switched inductor | High Q inductor | Asymmetric width transformer | Square shaped DGS |
| Technology | 180 nm | 180 nm | 180 nm | 180 nm |
| VCO core area ($mm^2$ ) | 0.75 | 0.098 | 0.42 | 0.0836 |
| *FoM* [dB] | 184.7 | 189.4 | 179.1 | 189.1 |
| $FoM_A$ [dB] | 186 | 199.5 | 183.3 | 199.9 |

## VI. CONCLUSION

A novel method to realize virtual inductance of high $Q$-factor by using a square-shaped DGS resonator is investigated in CMOS technology. The square-shaped DGS has only one current loop unlikely in H-shape DGS so that it results in a higher inductance of higher $Q$-factor. Finally, the proposed DGS resonator is employed to design a low phase noise 15GHz-band VCO in 0.18 $\mu$m CMOS technology. The *FOM* and $FOM_A$ of the implemented VCO are 189.1 dB and 199.9 dB, respectively.

## REFERENCES

[1] T. S. D. Dheung and J. R. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006, doi: 10.1109/JSSC.2006.872737.

[2] J. Kim *et al.*, "High-performance three-dimensional on-chip inductors in SOI CMOS technology for monolithic RF circuit applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2003, pp. 591–594, doi: 10.1109/RFIC.2003.1214016.

[3] L. S. Lee *et al.*, "Isolation on Si wafers by MeV proton bombardment for RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 928–934, May 2001, doi: 10.1109/16.918241.

[4] N. Li *et al.*, "High-$Q$ inductors on locally semi-insulated Si substrate by helium-3 bombardment for RF CMOS integrated circuits," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1269–1275, Apr. 2015, doi: 10.1109/VLSIT.2014.6894430.

[5] J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, and C.-K. Kim, "Surface micromachined solenoid on-Si and on-glass inductors for RF applications," *IEEE Electron Device Lett.*, vol. 20, no. 9, pp. 487–489, Sep. 1999, doi: 10.1109/55.784461.

[6] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998, doi: 10.1109/4.668989.

[7] S. Hekal *et al.*, "A novel technique for compact size wireless power transfer applications using defected ground structures," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 591–599, Feb. 2017, doi: 10.1109/TMTT.2016.2618919.

[8] A. Barakat, R. Pokharel, and T. Kaho, "60 GHz on-chip mixed coupled BPF with H-shaped defected ground structures," *IET Electron. Lett.*, vol. 52, no. 7, pp. 533–535, Apr. 2016, doi: 10.1049/el.2015.4465.

[9] W.-C. Liu, C.-M. Wu, and Y. Dai, "Design of triple-frequency microstrip-fed monopole antenna using defected ground structure," *IEEE Trans. Antennas Propag.*, vol. 59, no. 7, pp. 2457–2463, Jul. 2011, doi: 10.1109/TAP.2011.2152315.

[10] C. W. Ryu, C. S. Cho, J. W. Lee, and J. Kim, "New balanced self oscillating mixer using DGS resonator," in *Proc. Eur. Microw. Conf.*, Munich, Germany, 2007, pp. 648–651, doi: 10.1109/EUMC.2007.4405275.

[11] Y.-T. Lee, J.-S. Lim, J.-S. Park, D. Ahn, and S. Nam, "A novel phase noise reduction technique in oscillators using defected ground structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 2, pp. 39–41, Feb. 2002, doi: 10.1109/7260.982870.

[12] S.-L. Liu, K.-H. Chen, and A. Chin, "A dual-resonant mode 10/22-GHz VCO with a novel inductive switching approach," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 7, pp. 2165–2177, Jul. 2012, doi: 10.1109/TMTT.2012.2195674.

[13] Z.-Y. Yang and R. Y. Chen, "High-performance low-cost dual 15 GHz/30 GHz CMOS LC voltage-controlled oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 9, pp. 714–716, Sep. 2016, doi: 10.1109/LMWC.2016.2597174.

[14] J. Yang, C.-Y. Kim, D.-W. Kim, and S. Hong, "Design of a 24-GHz CMOS VCO with an asymmetric-width transformer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 3, pp. 173–177, Mar. 2010, doi: 10.1109/TCSII.2010.2043381.

[15] N. C. Karmakar, S. M. Roy, and I. Balbin, "Quasi-static modeling of defected ground structure," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 5, pp. 2160–2168, May 2006.

[16] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001, doi: 10.1109/4.972142.

**NUSRAT JAHAN** received the B.Sc. degree in electrical and electronic engineering from the Chittagong University of Engineering and Technology (CUET), Chittagong, Bangladesh, in 2010, and the M.Sc. degree in electrical and electronic engineering from Kyushu University, Japan, in 2016, where she is currently pursuing the Ph.D. degree, with a focus on millimeter-wave frequency generation and RF integrated circuits. She also served as a Lecturer with the Department of Electrical and Electronic Engineering, CUET from 2010 to 2013.

Ms. Jahan was a recipient of the Monbukagakusho (MEXT) Scholarship at Kyushu University.

**SITI AMALINA ENCHE AB RAHIM** received the Ph.D. degree in electrical and electronic engineering from Kyushu University, Fukuoka, Japan, in 2016. She is currently with the Fakulti Kejuruteraan Elektrik, Universiti Teknologi Mara, Shah Alam, Malaysia. Her current research interests include oscillators and RF integrated circuits design.

**ADEL BARAKAT** (GS'13–M'15) received the B.Sc. degree from Mansoura University, Mansoura, Egypt, in 2008, and the M.Sc. and Ph.D. degrees from the Egypt–Japan University of Science and Technology (E-JUST), Alexandria, Egypt, in 2012 and 2015, respectively, all in electronics and communications engineering. He has joined Kyushu University, Fukuoka, Japan, in 2015. He is currently a Post-Doctoral Fellow with E-JUST. His research interests are in the fields of metamaterials, planar antennas, on-chip antennas and filters, and wireless power transfer. He was a recipient of the certificate of appreciation from E-JUST President in 2010, and the Best Student Paper Award at the 1st Japan–Egypt Conference in Electronics, Communications and Computing in 2012.

**TAKANA KAHO** received the B.S. and M.S. degrees in physics from Tokyo Metropolitan University, Tokyo, Japan, in 1994 and 1996, respectively. In 1996, she joined the NTT Wireless Communication System Laboratories (currently, NTT Network Innovation Laboratories), NTT Corporation, Yokosuka, Japan, where she has been engaged in research of satellite on-board amplifier. She was a recipient of the 1998 Japan Microwave Prize presented at the Asia–Pacific Microwave Conference. She is a member of the Institute of Electronics, Information and Communication Engineers, Japan.

**RAMESH K. POKHAREL** (M'04) received the M.E. and Doctorate degrees from the University of Tokyo, Japan, in 2000 and 2003, respectively, all in electrical engineering. In 2005, he joined the Graduate School of Information Science and Electrical Engineering, Kyushu University, where he is currently a Professor. He was the Vice Director of the Center for Egypt–Japan Cooperation in Science and Technology, Kyushu University, from 2012 to 2013, where he has been serving as the Director since 2014. His current research interests include the low cost RFIC and analog circuits for microwave and millimeter wave wireless communications, and on-chip meta-materials in CMOS. He served as the Secretory of the IEEE MTT-S Japan Society from 2012 to 2013, where he has been serving as the Vice Chair for the Education Committee 2014–2016. Since Jan. 2017 he has been serving as the chair of the committee.