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p-GaN Gate Enhancement-Mode HEMT Through a High Tolerance Self-Terminated Etching Process

YU ZHOU[1], YAOZONG ZHONG[1,3], HONGWEI GAO[1], SHUJUN DAI[1], JUNLEI HE[1], MEIXIN FENG[1], YANFEI ZHAO[2], QIAN SUN[1], AN DINGSUN[2], AND HUI YANG[1]

1 Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou 215123, China
2 Vacuum Interconnected Nanotech Workstation, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou 215123, China
3 School of Materials Science and Engineering, Shanghai University, Shanghai 201900, China

CORRESPONDING AUTHOR: Q. SUN (e-mail: qsun2011@sinano.ac.cn)

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ABSTRACT An enhancement-mode high-electron-mobility transistor with a p-GaN gate was fabricated by using a chemistry-ease $Cl_2/N_2/O_2$-based inductively coupled plasma etching technique. This etching technique features a precise etching self-termination at the AlGaN barrier surface, which enables a broad process window with a large tolerance of etching time. With a post-annealing process, the property of two-dimensional electron gas (2DEG) can be restored to a high level after the etching. The mechanisms of etching self-termination and 2DEG recovery were clarified. The fabricated device exhibits a drain saturation current of 355 mA/mm with a threshold voltage of +1.1 V, an on/off ratio of 10^7, and a static on-resistance R_{ON} of 10 Ω·mm. Furthermore, normally-off operation of the device can be achieved across the wafer.

INDEX TERMS Enhancement-mode, HEMT, p-GaN gate, self-terminated etching.

I. INTRODUCTION

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have emerged as excellent devices for high power applications owing to their superior properties like high breakdown field, high carrier concentration, and high electron mobility. The common AlGaN/AlN/GaN-based HEMTs are naturally depletion-mode (D-mode) due to the existence of high density two-dimensional electron gas (2DEG) at the heterointerface [1]. For the consideration of cost and safe operation, true enhancement-mode (E-mode) devices are more desirable in the practical applications. Several approaches have been proposed to realize E-mode operation, such as fluorine-plasma ion implantation [2], recessed gate [3], [4], and p-GaN gate [5]–[10]. Among them, HEMT with a p-GaN gate (p-GaN E-HEMT) is the most promising candidate because of its excellent figure-of-merits and robust normally-off operation [11]–[13]. In principle, the conduction band of the AlGaN/AlN/GaN at the channel is lifted up through the p-GaN gate, resulting in a normally-off operation with a positive threshold voltage [7], while for the access region, selective removal of the overgrown p-GaN by uniformly etching is required to recover the 2DEG for a low conduction resistance [6]–[10], [14]–[22]. Generally, the critical etching step is fulfilled by using Cl_2/BCl_3-based slow rate inductively coupled plasma (ICP) etching technique through the control of etching time. Challenges arise from the fact that the slow etching rate is sensitive to the ICP chamber condition. Consequently, a stable and reproducible etching process is difficult to be achieved, leading to a narrow window for etching time. Hence either under-etching or over-etching of the p-GaN grown on the AlGaN/AlN/GaN for the non-gate region will occur uncontrollably. In fact, in the case of under-etching, the residual p-GaN layer will deplete the 2DEG more or less, while the 2DEG density will also decrease because of the thinner AlGaN barrier in the case of over-etching. And both will deteriorate the conduction of the device.

Some experimental methods on the selective ICP etching of GaN over AlGaN (or AlN) were proposed to obtain high selectivity ranged from 38 to 60 [23]–[25]. However, so far few of them have been reported for the real fabrication of

the nitride-based devices. In this work, p-GaN E-HEMTs were fabricated successfully by using the chemistry-ease $Cl_2/N_2/O_2$-based ICP etching technique. This technique features an etching self-termination at the AlGaN barrier surface, which generates a wide process window with a large tolerance of etching time. With a post-annealing process, the 2DEG property can be restored to a high level, and the normally-off operation of the device can be achieved across the wafer. And the etching-induced surface damage can be partially repaired with a dielectric passivation layer, mitigating the current collapse.

II. DEVICE STRUCTURE AND FABRICATION

The p-GaN/AlGaN/AlN/GaN HEMT structure was grown on a 2-inch p-Si (111) substrate with AlN/AlGaN stress-engineering transition layers [26]–[28]. The overgrown device structure consisted of a 2-μm-thick GaN highly resistive buffer layer, a 150-nm-thick un-doped GaN channel layer, a 1-nm-thick AlN interlayer, a 16-nm-thick $Al_{0.25}Ga_{0.75}N$ barrier layer, and an 85-nm-thick p-GaN cap layer. The Mg concentration of p-GaN was 5×10^{19} /cm^3. During the etching process, the RF and ICP powers were tuned carefully to 25 and 1750 W (DC Bias = 100 V), respectively, and the chamber pressure was 20 mTorr. By using a $Cl_2/N_2/O_2$-based gas mixture with a flow rate of 40/10/5 sccm, the etching rate of 45 nm/min can be attained for p-GaN. As a matter of fact, the p-GaN etching can terminate precisely at the AlGaN barrier after a 150-sec-long etching as shown in Figs. 1(a) and (b), suggesting that the over-etching time is about 35 sec. The etched surface was analyzed by X-ray photoelectron spectroscopy (XPS) at a take-off angle of 45°. Compared with an as-grown sample with an AlGaN(16 nm)/AlN/GaN structure which is named as A0 (shown in bottom of Fig. 1(c)), the peak of O 1s is enhanced intensively from 5.8 % to 20.2 % (atomic concentration), and a new peak of Cl 2p appears after ICP etching as shown in middle of Fig. 1(c). Both of them decrease sharply after a buffered-oxide etchant (BOE) wet treatment for 2 min (O 1s from 20.2 % to 4.6 %, Cl 2p from 1.7 % to 0.3 %) as shown in top of Fig. 1(c). Afterwards, a rapid thermal annealing was carried out at 500 °C in N_2 ambient for 5 min (post-RAT). The resulting surface maintains smooth step-flow morphology (Fig. 1(d)) which is similar to that of the as-grown ample A0 shown in Fig. 1(e). A Ti/Al/Ni/Au metal stack (20/130/50/150 nm) was used to form ohmic contacts, annealed in ambient N_2 at 850 °C for 30 sec. The p-GaN gate was metallized with a Pd Schottky gate. The work function $q\phi_m$ of Pd is known to be 5.1 eV. Thus the Schottky barrier height $[q\phi_{Bp} = E_g - q(\phi_m - \chi)]$ can be theoretically estimated to be 1.7 eV in Pd/p-GaN contact. A Ti/Au interconnection layer was patterned to finish the device.

To investigate the mechanism of the etching self-termination and evaluate the tolerance of etching time, sample A0 was deliberately exposed to the above-mentioned ICP for 60 sec (A1), followed by a 500 °C post-RTA treatment

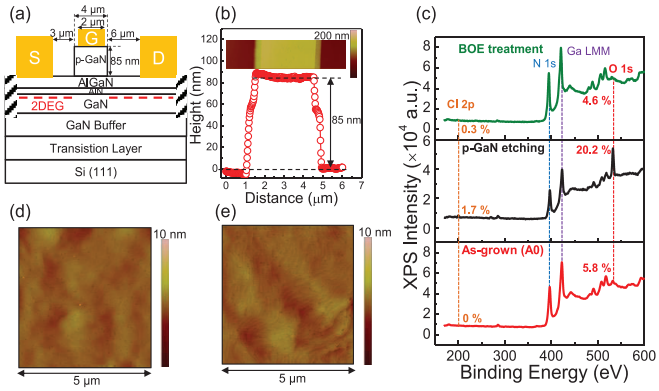

FIGURE 1. **(a) Schematics of the device structure (gate width $W_G = 100$ μm). (b) Atomic-force microscope (AFM) image of the p-GaN gate region and the depth profile of the p-GaN gate. (c) XPS spectra for sample A0, the etched surface of a p-GaN E-HEMT before and after BOE treatment (from bottom to top). (d) AFM image of the etched surface of a p-GaN E-HEMT after annealing with an RMS roughness of 0.35 nm. (e) AFM image of sample A0 with an RMS roughness of 0.33 nm (as-grown AlGaN(16 nm)/AlN/GaN structure).**

TABLE 1. **Summary of sample preparation.**

	As-grown→	ICP →	post-RTA
AlGaN(16 nm)/AlN/GaN	A0	A1	A2
p-GaN/AlGaN(16 nm)/AlN/GaN	B0	B1	B2

in N_2 ambient (A2). In addition, another as-grown sample with a p-GaN/AlGaN(16 nm)/AlN/GaN structure (B0) was used to monitor the p-GaN etching process. It underwent a 150-sec-duration p-GaN planar etching (B1) and then the 500°C post-RTA (B2) sequentially along with the device processing (see TABLE 1). The Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) measurements were implemented for samples A0 and A1 to determine the surface profiles of O-related elements accurately before and after ICP etching. As shown in Figs. 2(a) and (b), both $^{43}AlO^-$ and $^{85}GaO^-$concentrations within the 6-nm-thick surface region increase significantly after ICP etching (signals around 16∼17 nm are related to the AlN interlayer). This is consistent with the XPS result shown in Fig. 1(c), indicating that oxygen easily binds with Al and Ga. As a result, when the O-containing ICP etching reaches AlGaN barrier, Al atoms with Ga atoms nearby form a network-like $(Al,Ga)O_x$ thin film with high bond energy, acting as an etching-resistant oxide layer (Details can be seen in [29]). It is worthwhile to note that the newly formed oxide thin film can be removed by the BOE wet treatment which has been preliminarily shown in Fig. 1(c). In order to determine the thickness of the oxide layer further, an "ICP-BOE cycle" experiment was carried out on a sample with an AlGaN(30 nm)/AlN/GaN heterostructure, in which a 60-sec-duration O-containing ICP and a 120-sec-duration BOE treatment were done successively for 3 cycles, and a C-V characterization by Agilent-B1500A was made in each cycle as shown in Fig. 2(c). From the C-V data, a transformation to electron bulk density N_{C-V} as a function of the depth z

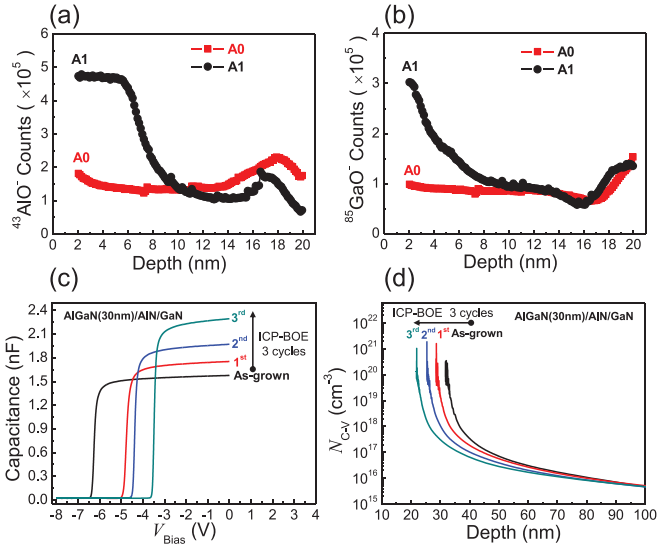

FIGURE 2. (a) $^{43}AlO^-$ profiles and (b) $^{85}GaO^-$ profiles for samples A0 and A1 measured by TOF-SIMS. (c) C-V characteristics measured on an as-grown and ICP-BOE treated AlGaN(30 nm)/AlN/GaN heterostructure at 10 kHz ($A = 0.6$ mm^2). (d) Local electron density as a function of the depth.

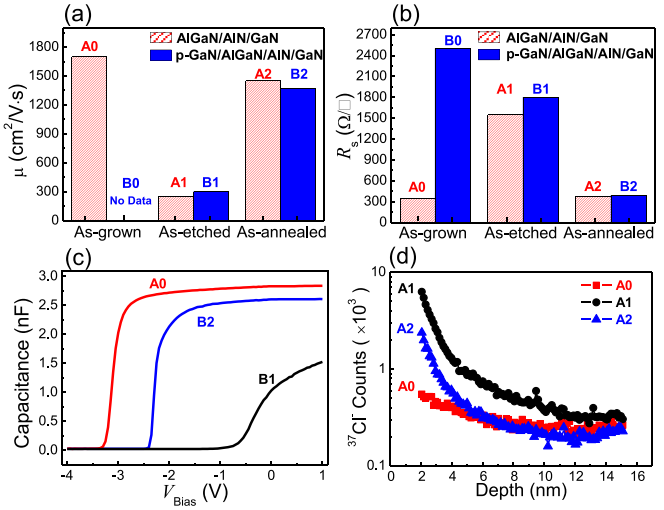

FIGURE 3. (a) Electron mobility and (b) sheet resistance of the AlGaN(16 nm)/AlN/GaN and p-GaN/AlGaN(16 nm)/AlN/GaN samples measured by Lehighton-1600 (non-contact microwave). (c) C-V curves of samples A0, B1, and B2 measured by Agilent-B1500A. (d) $^{-}Cl^{37}$ profiles for samples A0, A1, and A2 measured by TOF-SIMS.

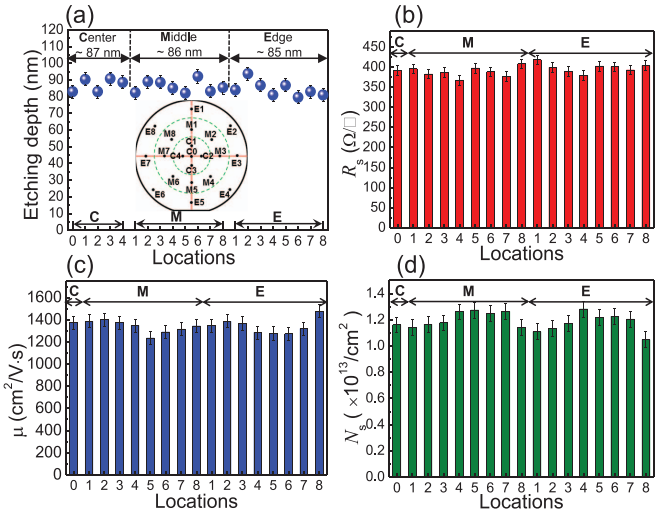

FIGURE 4. (a) Uniformity of the p-GaN gate etching depth. (b)-(d) Uniformity of sheet resistance R_S, electron mobility μ, and electron density N_S after the combined etching and annealing process (sample B2).

is performed based on the following equations [1]:

$$N_{C\text{-}V}(z) = -\frac{C^3}{q\varepsilon_0\varepsilon_{AlGaN}A^2}\left(\frac{dC}{dV}\right)^{-1} \quad (1)$$

and

$$z = \frac{\varepsilon_0\varepsilon_{AlGaN}}{C} \quad (2)$$

where ε_0 is the vacuum permittivity, q is the elementary charge, and A is the area of the electrode contact. The thickness of the oxide layer after the 60-sec-duration ICP etching is estimated to be $\sim$ 3.5 nm as shown in Fig. 2(d), implying that the AlGaN barrier is only thinned slightly with a long ICP etching followed by a dip in the BOE solution. This means it will have little influence on the 2DEG density in the real fabrication of p-GaN E-HEMTs, in which the over-etching time is shorter, about 35 sec as mentioned above.

Figs. 3(a) and (b) show that the 2DEG of sample A2 is greatly recovered after the post-RTA process, confirming that the AlGaN barrier layer can barely be etched by the O-containing ICP. Actually, an etching experiment on the AlGaN(16 nm)/AlN/GaN heterostructure with even longer time (120 sec) was also made, and a similar result was obtained (not shown here). Thus it indicates that there is a quite wide process window for etching time. Hence the developed etching method will ensure the reproducible run-to-run uniformity regardless of the etching chamber condition. The capacitances as a function of voltage for samples A0, B1 and B2 were measured by Agilent-B1500A to characterize the influence of etching and post-RTA on 2DEG. As shown in Fig. 3(c), the C-V curve of sample B1 exhibits a positive $\sim +3$ V shift from that of sample A0, but a negative shift of about 1.8 V after the post-RTA process. The shape of C-V curve of sample B2 is similar to that of sample A0, meaning that the 2DEG is recovered to a great extent after the post-RTA. In fact, both the electron mobility and the sheet resistance of sample B2 reach levels close to those of sample A0 (Figs. 3(a) and 3(b)), indicating that the etching with a post-annealing process works effectively. To explore the possible cause of the 2DEG degradation and recovery, $^{-}Cl^{37}$ profiles were also measured by TOF-SIMS for samples A0, A1, and A2. Fig. 3(d) indicates that negatively charged Cl ions which have the kinetic energy of $\sim$ 100 eV (DC Bias = 100 V as mentioned above) were infused into the AlGaN barrier (A1) during the ICP etching. This agrees well with the XPS result shown in Fig. 1(c). The density of the infused $^{-}Cl^{37}$ ions is estimated to be about $10^9 - 10^{10}$ cm^{-2} according to the detection limit range for Cl in (Al)GaN ($10^{15} - 10^{16}$ cm^{-3}). Quantitatively

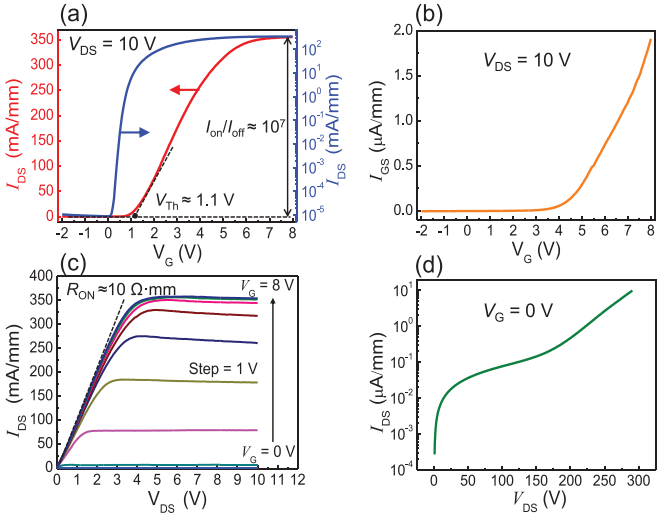

FIGURE 5. Device performance of an as-fabricated p-GaN E-HEMT. (a) Transfer characteristics under V_{DS} = 10 V. (b) Gate leakage characteristics under V_{DS} = 10 V. (c) Output characteristics. (d) Off-state drain leakage under V_G = 0 V.

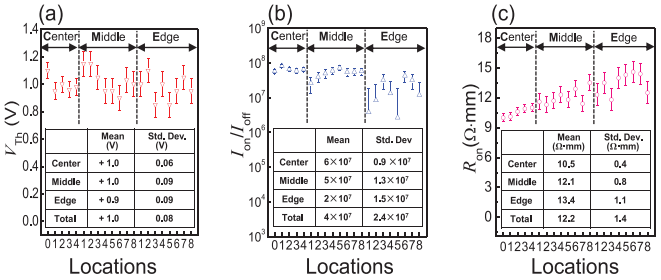

FIGURE 6. Distribution of the device performance for the as-fabricated p-GaN E-HEMTs across the wafer. (a) V_{Th}, (b) I_{on}/I_{off}, and (c) static R_{on}.

speaking, the infusion length is around 10 nm as seen in log-scale, meaning that the as-infused Cl ions are very close to the 2DEG. Therefore, it leads to a degradation of electron mobility caused by Coulomb scattering as well as a distinct positive shift in C-V curve as shown for sample B1. Fortunately, most of the as-infused Cl ions in the AlGaN barrier can be driven out significantly by the post-RTA process as shown by the curve of A2, resulting in the remarkable 2DEG recovery. It is noteworthy that the concentration of $^{-}Cl^{37}$ within 4 nm beneath the surface is still a bit higher than the as-grown sample (A0). This might be attributed to the newly formed network-like $(Al,Ga)O_x$ thin film which may solidify the Cl ions. In fact, the surface Cl ions can be almost removed because of the BOE wet treatment used in the practical process. Further study on the exact mechanism of 2DEG recovery is ongoing.

With the O-containing ICP etching, the depth uniformity of p-GaN gate etching was investigated across the wafer as shown in Fig. 4(a). Highly uniform etching depth of p-GaN gates with an average height of 86 ± 3 nm was achieved during the device fabrication. The 2DEG characteristics across the wafer after the planar etching with a post-RTA process (sample B2, see TABLE I) are summarized in Figs. 4(b)-(d). Sheet resistance, electron mobility, and electron density of the 2DEG all reach normal levels with high uniformity, showing a small fluctuation with average values of 390 ± 12 Ω/□, 1340 ± 59 $cm^2/V{\cdot}s$, $(1.20 \pm 0.06)\times10^{13}$ cm^{-2}, respectively.

III. DEVICE RESULTS AND DISCUSSION

Fig. 5(a) shows the transfer characteristics of a typical as-fabricated p-GaN E-HEMT at V_{DS} = 10 V. A normally-off operation with a V_{Th} of 1.1 V is achieved. The maximum drain current, I_{DS}, is 355 mA/mm. As seen in log-scale, the I_{on}/I_{off} ratio is as high as 6×10^7. As shown in Fig. 5(b), the as-fabricated p-GaN E-HEMT has a low gate leakage $I_{GS} \sim 1.9$ μA/mm at V_{DS} = 10 V and V_{GS} = 8 V. Fig. 5(c) shows well-behaved DC output characteristics with a static R_{on} of ~10 Ω·mm at V_{GS} = 8 V. With the p-Si substrate grounded, the soft electrical breakdown does not happen until the drain bias, V_{DS}, is increased to 300 V, taking 10 μA/mm as a criterion as shown in Fig. 5(d). It is interesting that the characteristic of off-state drain current is very similar to that of the GaN-on-Si Vertical Schottky diode reported by MIT [30]. And this I-V behavior may be associated with the dislocation or trap-related leakage paths in the GaN channel layer.

On-wafer uniformity of the device performance was evaluated across the wafer. A simple statistical analysis on V_{Th} and I_{on}/I_{off} is presented in Figs. 6(a) and (b), showing that the normally-off operation can be realized across the whole wafer. The relatively large Std. Dev. ($\sim1.5\times10^7$) of the I_{on}/I_{off} ratio for the edge region might be caused by the non-uniformity of the Mg doping during the growth, which will be improved in future. In Fig. 6(c), the static on-resistance, R_{on}, exhibits a slight variation from the center to the middle, with an average value of 10.5 to 12.1 Ω·mm and a standard deviation (Std. Dev.) of 0.4 to 0.8 Ω·mm, indicating that p-GaN etching has only little influence on ohmic contact and channel resistance. The higher R_{on} for the edge region with a relative large Std. Dev. Of ~ 1.1 Ω·mm may result from the inherent inhomogeneity of the ICP etcher itself, e.g., mainly the inhomogeneity of ionized gas distribution and the direction of the plasma bombardment. Since the p-GaN etching process has an intimate relation with the on-state performance of the device, the static on-resistance R_{on} and saturation current I_{sat} are summarized (see Fig. 7). Compared with the other reported p-GaN E-HEMTs through the ICP etching method, the presented device exhibits both a relative low R_{on} and a high I_{sat}, showing that the developed O-containing p-GaN etching technique will cause little degradation of the DC performance.

The O-containing ICP etching can result in an etching stop at the AlGaN barrier perfectly through an oxide surface network. However, the inevitable etching damage will have a significant impact on the dynamic performance of the device without any passivation. A dynamic R_{on} characterization was carried out as illustrated in Fig. 8(a). The device

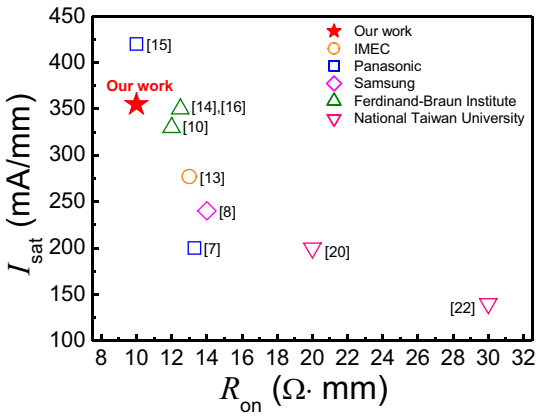

FIGURE 7. **Static on-resistance R_{on} and saturation current I_{sat} for p-GaN E-HEMTs fabricated by several main groups.**

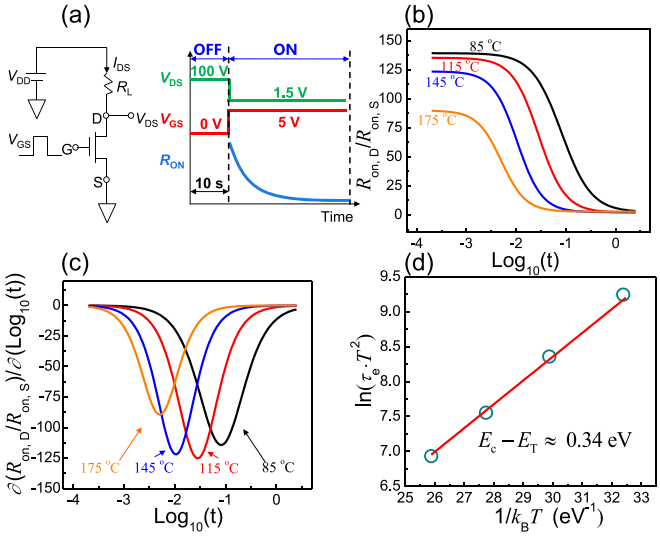

FIGURE 8. **(a) The schematic of the dynamic R_{on} measurement. (b) On-resistance transients measured at varied temperatures. (c) Time constant spectra (derivative of the on-resistance transients). (d) Arrhenius plot of the trap level.**

was stressed in the OFF state ($V_{GS} = 0$ V, $V_{DS} = 100$ V) for a very long time (10 sec), then it was switched to the ON state ($V_{GS} = 5$ V, $V_{DS} = 1.5$ V). With a HVSMU/HCSMU fast switch, $R_{on,D}$ can be measured accurately after 200 μs. Fig. 8(b) shows that dynamic $R_{on,D}$ at 200 μs ($R_{on,D}/R_{on,S}$) is as high as 139 at 85 °C. The time constant spectra feature an enhancement of electron emission by the elevated temperature shown in Fig. 8(c), suggesting that electron trapping was mainly responsible for the observed current collapse. Through an Arrhenius plot, the energy level of the traps was extrapolated as 0.34 eV as shown in Fig. 8(d). The traps may be related to N-vacancies and/or O-related surface states due to the O-containing ICP etching [31]. With the further dielectric surface passivation (ALD $Al_2O_3 \sim 15$ nm), the current collapse can be suppressed effectively as shown in Fig. 9. It is believed that with an optimized passivation processing, the current collapse observed in the presented

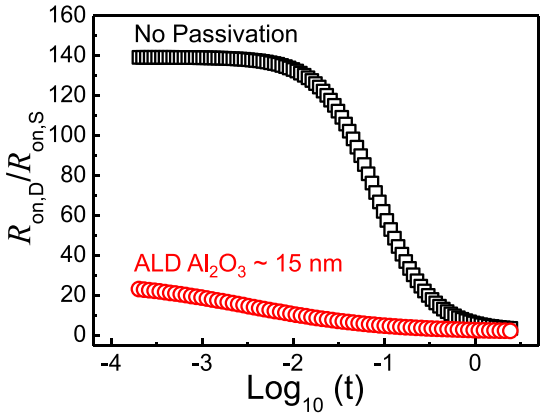

FIGURE 9. **Current collapse alleviation with further passivation (at 85 °C).**

device can be alleviated further. Therefore, CVD-based SiN_x passivation for p-GaN E-HEMT will be developed in future.

IV. CONCLUSION

In summary, the $Cl_2/N_2/O_2$-based ICP etching method was successfully developed and applied to the fabrication of p-GaN E-HEMTs. Compared with the conventional etching techniques, this O-containing etching process features a self-termination at AlGaN barrier, which enables a precise formation of the p-GaN gate and a broad process window with a large tolerance of etching time. With the surface treatment followed by a post-RTA process, 2DEG can be recovered to a great extent, and the fabricated devices exhibit good DC performance. Furthermore, normally-off operation of the device can be achieved across the wafer. With the dielectric surface passivation, current collapse can be alleviated significantly. Therefore, the as-developed technique may provide a powerful tool for a reliable fabrication of p-GaN E-HEMTs.

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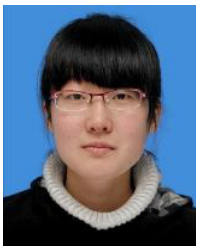
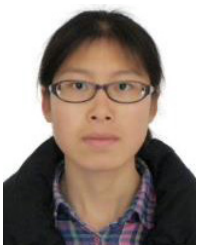
YU ZHOU received the Ph.D. degree in microelectronics and solid state electronics from the University of Chinese Academy of Sciences, Beijing, China, in 2013. From 2013 to 2016, he was a Post-Doctoral Research Fellow on GaN-based materials and power devices with the Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO), Chinese Academy of Sciences (CAS), Suzhou, China, where he joined the Key Laboratory of Nanodevices and Applications. He is currently an Associate Professor with the SINANO, CAS. His current research interests include GaN-on-Si epitaxial growth, power devices, and characterization techniques.

YAOZONG ZHONG received the B.S. degree in material science and engineering from Central South University, Changsha, China, in 2011. He is currently pursuing the M.S. degree in microelectronics and solid state electronics with the joint training of Shanghai University, Shanghai, China, and Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China. His main research interest focuses on the p-GaN gate enhancement-mode HEMT.

HONGWEI GAO received the B.S. degree in applied physics from Nanjing University, Nanjing, China, in 2010. He is currently a Research Assistant with the Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China. His current research interest includes III-nitride semiconductor material epitaxial growth.



SHUJUN DAI received the B.S. degree in material science and engineering from the Nanjing University of Science and Technology, Nanjing, China, in 2013. She is currently pursuing the Ph.D. degree in microelectronics and solid state electronics with the Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China. Her current research interests include quaternary alloy AlInGaN materials and related electronic devices.



JUNLEI HE received the B.S. degree in electrical engineering from Hubei University, Wuhan, China, in 2014. She is currently pursuing the Ph.D. degree in microelectronics and solid state electronics with the Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China. Her current research interest includes GaN-on-Si vertical power devices.

MEIXIN FENG received the Ph.D. degree in microelectronics and solid state electronics from the University of Chinese Academy of Sciences, Beijing, China, in 2014. He currently holds a Post-Doctoral position with the Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China. His current research interests include GaN-based laser diodes, high-efficiency light emitting diodes, and GaN-based high-electron-mobility transistors.

YANFEI ZHAO received the Ph.D. degree from the International Center for Quantum Materials, Peking University, Beijing, China. She is currently an Assistant Professor with Vacuum Interconnected Nanotech Workstation, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China. Her research interests focus on the surface and interface of semiconductor materials.

QIAN SUN received the B.S. degree in material science and engineering from the University of Science and Technology of China, Hefei, China, the M.S. degree from the Institute of Semiconductors, Chinese Academy of Sciences (CAS), Beijing, China, and the Ph.D. degree from Yale University, New Haven, CT, USA. He is currently a Professor with the Suzhou Institute of Nano-Tech and Nano-Bionics, CAS, Suzhou, China, where he is also the Director of the Key Laboratory of Nanodevices and Applications. His current research interests include GaN-based epitaxial growth, power devices, laser diodes, and high-efficiency light emitting diodes.

AN DINGSUN received the B.S. and M.S. degrees from Tsinghua University and the Ph.D. degree from the Institute of Semiconductors, Chinese Academy of Sciences (CAS), Beijing, China. He is currently a Professor with the Suzhou Institute of Nano-Tech and Nano-Bionics, CAS, Suzhou, China, where he is also the Director of the Vacuum Interconnected Nanotech Workstation. His research interests focus on the surface and interface of semiconductor materials.

HUI YANG received the B.S. degree from Peking University in 1982, and the Ph.D. degree from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, in 1997. He is currently the Director of the Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences. His current research interests include GaN-based laser diodes, high-efficiency light emitting diodes, GaN-based high electron mobility transistors, and solar cell of III–V compound semiconductor materials.