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Physics-Based Multi-Bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow

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ABSTRACT In this paper, a consistent DC to RF modeling solution for Al gallium nitride (GaN)/GaN high electron mobility transistors is demonstrated that is constructed around a surface-potential-based core. Expressions for drain current and intrinsic terminal charges in the form of surface-potential are used to simultaneously model the DC characteristics and the intrinsic capacitances of a commercial GaN device. Self-heating and trapping effects are incorporated to account for the non-linear nature of the device. We discuss the parameter extraction flow for some of the key model parameters that are instrumental in fitting the DC characteristics, which simultaneously determines the bias-dependent intrinsic capacitances and conductances that significantly eases the RF parameter extraction. Parasitic capacitances, gate finger resistance, and extrinsic bus-inductances are extracted, from a single set of measured non-cold-FET S-parameters, using the model process design kit. The extraction procedure is validated through overlays of broadband (0.5–50 GHz) S-parameters, load-pull and harmonic-balance (10 GHz) simulations against measured data, under multiple bias conditions to successfully demonstrate the model performance at large-signal RF excitations.

INDEX TERMS GaN HEMT, parameter extraction, physics-based RF compact model, load-pull.

I. INTRODUCTION

Gallium Nitride (GaN) HEMTs and their associated RF circuit applications have been a topic of aggressive academic and industrial research over the past couple of decades, due to the commendable level of performance promised by the GaN material system and the heterojunction that it forms with AlGaN, leading to features such as high mobility, high saturation velocity, high sheet carrier density, high breakdown voltage etc [1], [2]. In order to take full advantage of these properties and to translate them into viable microwave and RF circuit applications, a fully robust and accurate RF GaN HEMT model is of prime importance.

The existing literature encompasses a huge variety of models that are primarily empirical, table-based, artificial neural-network based or X-parameter based models [3]–[14]. High fidelity physics-based compact models for GaN HEMTs, particularly surface-potential-based, are desirable and the industry is looking for them for multiple reasons [15], [16]. First, GaN technology is still not fully matured and a physics-based model would help a great deal in the device design and therefore in the evolution of the GaN technology itself. Second, a physics-based model offers a relatively smaller set of parameters whose flow of extraction is simple and can be related to the intrinsic device physics, leading to a more meaningful model card. Finally, physics-based models are inherently scalable with regard to bias, temperature or geometry, which can be of significance to circuit designers so that they can explore a wider design space.

In our previous publications, we demonstrated an analytical calculation of surface potential (SP) in GaN HEMTs used to self-consistently evaluate the drain current and intrinsic charges, from which we obtain the capacitances [17]–[21]. It is named the Advanced SPICE Model for GaN HEMTs (ASM-GaN-HEMT) and is currently under consideration for industry standardization at the Compact Model Coalition (CMC) [22]. In this paper, we aim to present the RF performance of the model under small-signal and

large-signal considerations. Moreover, we present a simple RF model parameter extraction procedure wherein only the parasitic components of the intrinsic capacitances are to be extracted using RF measured data whereas the complex bias dependent model is naturally taken care of by fitting the DC-characteristics which is due to the dependence of the intrinsic charges and current on a single quantity, i.e., the surface-potential. As a result, the extraction procedure does not require any complex optimization programs [8], [12] as opposed to various empirical or artificial neural network based models in which the current source and intrinsic capacitances are essentially disconnected and bias-independent. This serves as our primary motivation for a physics-based RF compact model for GaN HEMTs that could be readily used as an industry standard for design of state-of-the-art RF circuits.

The paper is organized as follows: We briefly revisit the model description in Section II and its DC parameter extraction flow is presented in Section III. Trapping effects and their modeling are discussed in Section IV. In Section V, we carry out the extraction of the multi-bias RF small-signal model valid for a broadband frequency range whereas large-signal performance of the model is studied in Section VI. Finally, conclusions are drawn in Section VII.

II. MODEL DESCRIPTION

The heart of the model is the analytical modeling of surface-potential (ψ) and its variation with applied gate (V_g) and drain (V_d) biases. More details about ψ calculation can be found in [17]. The expressions for intrinsic gate (Q_{gi}) and drain (Q_{di}) charges [19], [20] and drain current (I_d) [23] after incorporating real device effects (see Fig. 1) such as velocity saturation, DIBL, mobility degradation, channel length modulation (CLM) are reproduced in (1)–(3), as shown at the bottom of this page, for the sake of completeness.

The source charge (Q_{si}) is derived from charge conservation among Q_{gi}, Q_{di} and Q_{si}, which offers the benefit of obtaining good convergence during simulation, and these quantities are used to compute the intrinsic capacitances. It is worth mentioning that the feature of having a simultaneous solution for the drain current as well as the capacitances offers a significant advantage in terms of parameter extraction at RF as well as accuracy of the S-Parameter simulations. Empirical models lack such an advantage, since the modeling approach followed in such cases involves isolated expressions for capacitances, transconductance, output conductance etc.

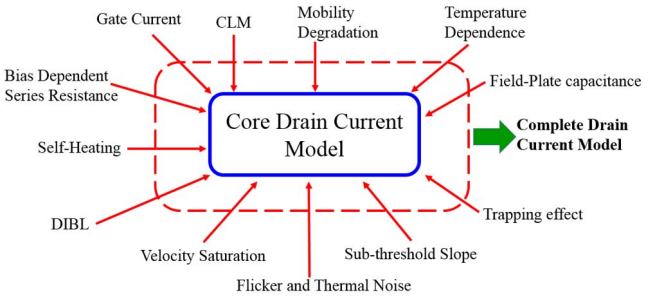

FIGURE 1. Various non-idealities in device behaviour added to the core surface-potential-based drain current model to realize a more realistic device.

The access region (AR) resistance model [24] is appended to the core model in order to capture the significant modulation of the ON-resistance in GaN devices due to large ARs particularly at drain so as to support a high breakdown voltage. The current in the AR is represented as in (4), as shown at the bottom of this page, [24], where L_{acc} is the AR length, N_{S0ACCS}, $V_{SATACCS}$ and U_{0ACCS} represent the AR 2DEG sheet carrier density, carrier saturation velocity and mobility respectively.

III. DC PARAMETER EXTRACTION

It is well known that various physical effects within the device are intertwined and, therefore, collectively influence the values of parameters. It makes the direct extraction of parameters complicated for the users, and may demand significant number of device measurements for the parameter extraction process. For instance, in order to extract parameters that govern the AR resistances, a set of TLM measurements might come very handy, however, absence of such data might make it tedious to directly extract not only AR resistance model parameters but also other parameters as well.

$$Q_{gi} = WLN_fC_g\left\{V_{go} - \frac{(\psi_s+\psi_d)}{2} + \frac{\psi_{ds}{}^2}{12\left(V_{go} - \frac{(\psi_s+\psi_d)}{2} + \frac{K_BT}{q}\right)}\right\} \tag{1}$$

$$Q_{di} = -\frac{WLN_fC_g}{2}\left\{V_{go} - \frac{(\psi_s+2\psi_d)}{3} + \frac{\psi_{ds}{}^2}{12\left(V_{go} + \frac{K_BT}{q} - \frac{(\psi_s+\psi_d)}{2}\right)} + \frac{\psi_{ds}{}^3}{120}\left(V_{go} + \frac{K_BT}{q} - \frac{(\psi_s+\psi_d)}{2}\right)^{-2}\right\} \tag{2}$$

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}}\frac{W}{L}C_gN_f\left[V_{go} - \left(\frac{\psi_s+\psi_d}{2}\right) + \frac{K_BT}{q}\right]\times\psi_{ds}(1+\lambda V_{ds}) \tag{3}$$

$$R_{ds,acc} = \frac{R_c}{W\cdot N_f} + \frac{L_{acc}}{W\cdot N_f\cdot q\cdot N_{S0ACCS}\cdot U_{0ACCS}}\times\left(1-\left(\frac{I_{ds}}{W\cdot N_f\cdot N_{S0ACCS}\cdot V_{SATACCS}}\right)^2\right)^{-1/2} \tag{4}$$

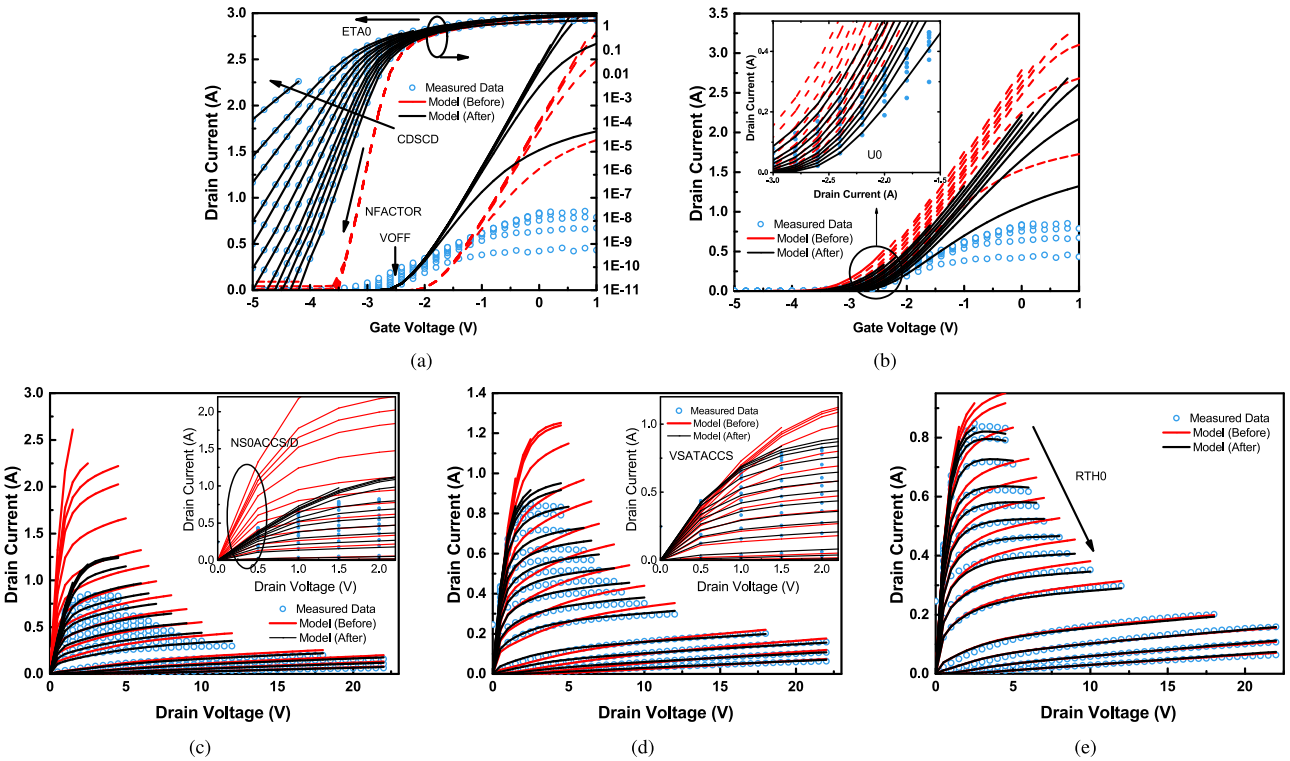

FIGURE 2. Step by step DC Parameter Extraction Flow using multiple bias $I_d - V_g$ and $I_d - V_d$ plots. (a) V_{OFF} identification from $I_d - V_g$ linear data. Optimization of N_{FACTOR}, η_0 and C_{DSCD} from logarithmic scale $I_d - V_g$ plot after V_{OFF} is extracted. (b) U_0 is optimized to fit the low V_g conditions. (c) The ON-resistance in the linear region of the $I_d - V_d$ plot is fitted by adjusting N_{S0ACCS}. (d) $V_{SATACCS}$ is extracted by fitting the saturation current in $I_d - V_d$. (e) R_{TH0} is adjusted to fit self-heating. The model results before and after the extraction of parameters are shown in red and black respectively.

TABLE 1. Key DC model parameters [23].

Parameter	Description	Extracted Value
V_{OFF}	Cutoff Voltage	-2.86 V
N_{FACTOR}	Subthreshold Slope Factor	0.202
C_{DSCD}	SS Degradation Factor	0.325 V^{-1}
η_0	DIBL Parameter	0.117
V_{DSCALE}	DIBL Parameter	2.981
U_0	Low Field Mobility	33.29 $mm^2/V-s$
N_{S0ACCS}	AR 2DEG density	$1.9e+17$ $/m^2$
$V_{SATACCS}$	AR saturation velocity	157.6k cm/s
R_{TH0}	Thermal Resistance	22 Ω

In this work, we turn our focus on certain key model parameters, listed in Table 1, and extract their values using fitting or data identification under different bias regions so that the different physical effects can be decoupled. The device under test (DUT) is a 125 nm GaN device with a gate periphery of 10×90 μm, and AR lengths of 200 nm and 1.7 μm between the gate-to-source and gate-to-drain nodes respectively. Fig. 2 has the intermediate plots where in parameters are extracted by identification from data or tuning within certain bias ranges.

To start with, Fig. 2(a) has the $I_d - V_g$ plot in linear and log scale for multiple V_d conditions. V_{OFF} can be identified from the data as the V_g value at which I_d begins to rise, marking the end of the subthreshold region. It can also be quantified using the well-known g_m-derivative or constant current method. The extracted value of V_{OFF} should correspond well with the $I_d - V_g$ log plot. This gives a good starting value of V_{OFF} and can be fine-tuned for better fitting. In the same plot, parameters N_{FACTOR}, C_{DSCD}, η_0 and V_{DSCALE} can be extracted from the log scale curves under subthreshold region. N_{FACTOR} is the subthreshold slope parameter and can be optimized to fit the subthreshold slope for low V_d values. Once N_{FACTOR} has been set, the parameter η_0 can be optimized to adjust DIBL or V_{OFF}-degradation with increasing V_d. Alternately, η_0 can be extracted from inspecting the data. The shift in subthreshold curves between linear and saturation V_d values for same current should give a rough estimate of η_0 whereas V_{DSCALE} determines the rate at which V_{OFF} changes with increasing V_d. The degradation in subthreshold slope with increasing V_d is decided by C_{DSCD}.

The low field mobility parameter U_0 is adjusted by fitting the low V_d and low V_g data conditions in the $I_d - V_g$ linear plot so that mobility as a result of degradation from the vertical field as well as field along the channel can be safely assumed to be U_0. The Fig. 2(b) and its zoomed inset highlight the fitting results after optimizing U_0.

The AR parameters N_{S0ACCS} and $V_{SATACCS}$ are extracted from $I_d - V_d$ linear and saturation regions respectively as shown in Fig. 2(c) and 2(d). N_{S0ACCS} is instrumental in

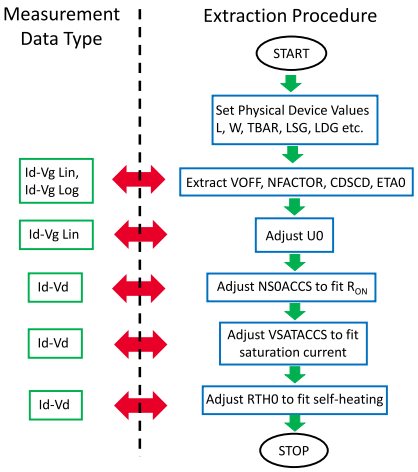

FIGURE 3. DC Parameter extraction flow as described in Section III to fit not only the drain current but also to obtain intrinsic capacitances. The AR model is incorporated into the intrinsic model as shown in Fig. 2.

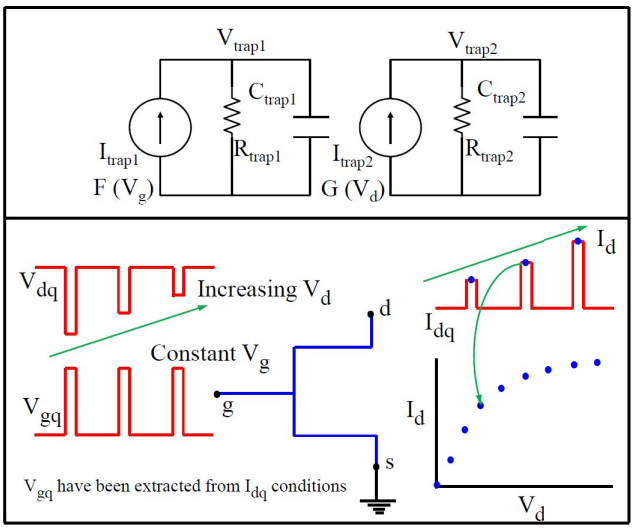

FIGURE 4. (I) Two R – C sub-circuits used for modeling trapping effects, one each for gate-lag and drain-lag. The voltages $V_{trap1,2}$ are fed back into the compact model to update its key parameters as shown in (5). (II) The dual-pulsed scheme to do the pulsed-IV simulation.

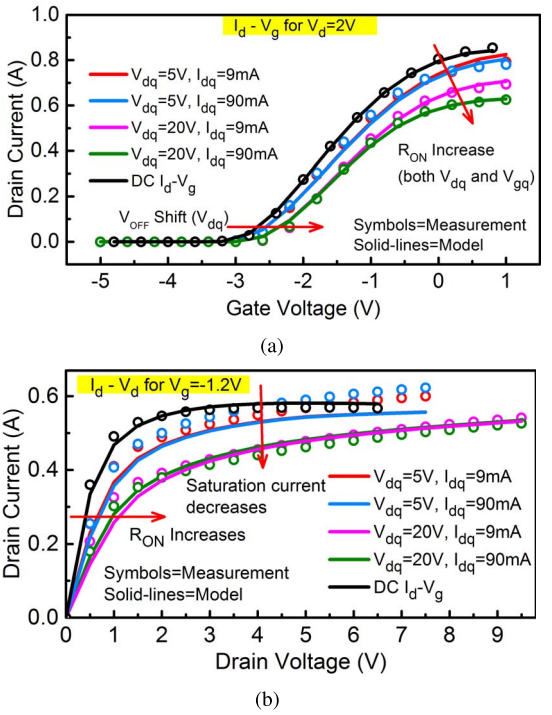

FIGURE 5. Correlation between measured and modeled (a) Pulsed $I_d - V_g$ and (b) Pulsed $I_d - V_d$ characteristics using the trap model. Accurate fits are seen for multiple quiescent bias conditions ($V_{dq} = 5, 20$ V and $I_{dq} = 10, 100$ mA/mm), which is essential for the non-linear RF behavior of the model.

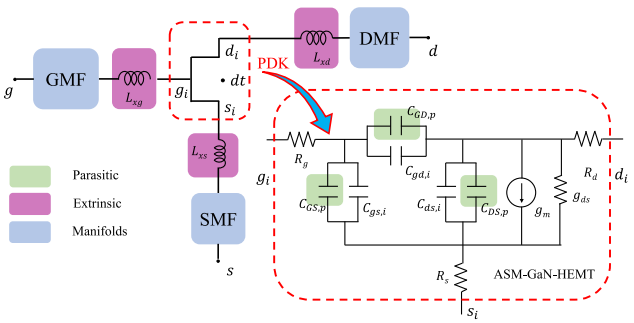

FIGURE 6. Small Signal Equivalent Circuit Model of the overall device including the intrinsic device as described by the ASM – HEMT model PDK. Access resistances R_g, R_d and R_s are included in the intrinsic core model whereas only the bus-inductances form the extrinsic level parasitics. Standard transmission line models are used for manifolds.

deciding the ON-resistance whereas $V_{SATACCS}$ settles the saturation current level. Self-heating effect (SHE) is modeled using the standard R – C network approach, which consists of a thermal resistance (R_{TH0}) and a thermal capacitance (C_{TH0}). The change in voltage at the thermal node gives the rise in temperature (ΔT), which is added to the nominal temperature (T_{NOM}) at which the device is operating. The negative slope for high current $I_d - V_d$ regions in the DC – IV plots, shown in Fig. 2(e), illustrates the SHE as predicted by the model and allows extraction of parameter R_{TH0}. The flow described above is summarized in Fig. 3.

IV. MODELING OF TRAPPING EFFECTS

An accurate trap model is crucial in order to estimate the large-signal RF behaviour of GaN HEMTs. A reduction in output power of RF power amplifiers as compared to the expected theoretical output power ($V_{pp}I_{pp}/8$) is ascribed to the various manifestations of trapping such as current collapse, knee walkout, drain-lag, gate-lag etc [25]–[28]. Pulsed IV characterization in dual-pulse mode at a pulse frequency of 1000 Hz with a duty-cycle of 0.02 %, as indicated in Fig. 4, is performed under multiple quiescent drain and gate bias conditions such that both the gate and the drain voltages are pulsed simultaneously from the quiescent bias point. The pulse width of 200 ns and the measurement window of 40 ns within these 200 ns is short enough to ensure iso-thermal and

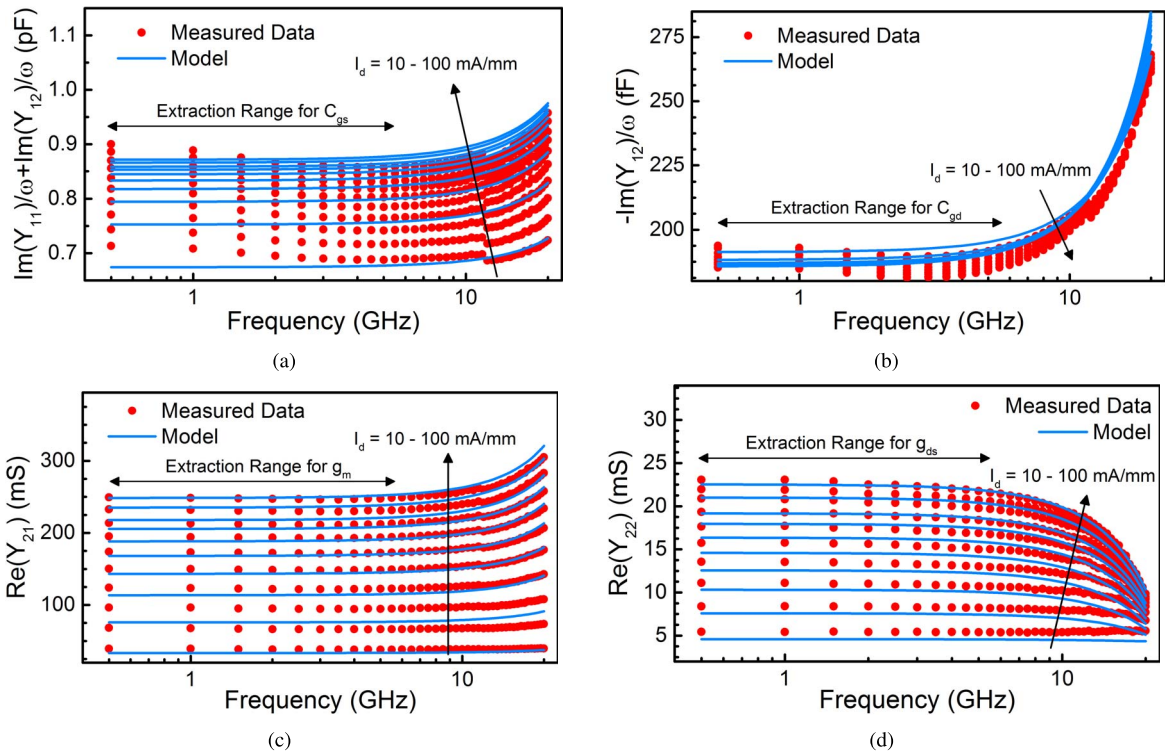

FIGURE 7. Extracted SS – EC (a) C_{gs} (b) C_{gd} (c) g_m and (d) g_{ds} for V_d = 5 V and 10 gate bias conditions. Parasitic capacitances are adjusted to values given in Table 2 to fit model and measured data for (a–b). A sufficiently broad frequency range (≈ 10 GHz) is observed for extraction for which frequency-independent behavior of SS – EC elements is seen after which inductive effects dominate.

iso-dynamic measurement of the pulsed-IV characteristics. From Fig. 5 we observe that the four most important parameters, in which dispersion due to trapping should be modeled, are V_{OFF}, η_0, C_{DSCD} and the drain/source AR resistances (R_{ds}). We model this with 2 R – C sub-circuits shown in Fig. 4. The node voltages V_{trap1} and V_{trap2}, which represent effects due to gate and drain lag respectively, are fed back into the model to update V_{OFF}, η_0, C_{DSCD} and R_{ds}, given as

$$\begin{aligned} V_{OFF}(\text{Trap}) &= V_{OFF} + (V_{OFFTR} \cdot V_{trap2}) \\ \eta_0(\text{Trap}) &= \eta_0 + (\eta_{0TR} \cdot V_{trap2}) \\ C_{DSCD}(\text{Trap}) &= C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2}) \\ R_{ds}(\text{Trap}) &= R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2}) \end{aligned} \quad (5)$$

where V_{OFFTR}, η_{0TR}, C_{DSCDTR}, R_{TR1} and R_{TR2} are used as parameters. Shown in Fig. 5 are accurate model fits for pulsed $I_d - V_g$ and $I_d - V_d$ for multiple quiescent bias conditions, validating the proposed trap model.

V. RF PARAMETER EXTRACTION

RF small-signal equivalent circuit (SS – EC) is shown in Fig. 6. The overall SS – EC has gate (GMF) and drain (DMF) manifolds or pads, feeding the signals to gate and drain ports respectively. It also has the source manifold (SMF) or via-holes, through which the source-pad is connected to the back-plane metallization. Beyond the manifolds are bus-inductances L_{xg}, L_{xd} and L_{xs} that represent the connection between the pads and the actual DUT, which itself is governed by the process design kit (PDK). The zoomed inset shows the equivalent circuit representation of the intrinsic DUT featuring parasitic capacitances $C_{GS,p}$, $C_{GD,p}$ and $C_{DS,p}$ and access resistances R_g, R_d and R_s.

With the bulk of the parameter extraction exercise done for DC – IV in Section III, the transconductance (g_m), output conductance (g_{ds}), intrinsic capacitances ($C_{gs,i}$, $C_{gd,i}$ and $C_{ds,i}$) and intrinsic gate resistance ($R_{g,i}$) are simultaneously determined since they depend on a single quantity, i.e., ψ. Additionally, AR resistances, R_d and R_s, are also fitted while extracting values for N_{S0ACCS} and V_{S0ACCS} during DC parameter extraction. So, we now are only left with the task of extracting the parasitic capacitances and the gate finger resistance ($R_{g,f}$) in addition to the inductances.

Keysight's ADS simulator is used to perform all the model simulations. Broadband S-parameters (0.5 – 50 GHz) measured under multiple bias conditions are used for RF parameter extraction. The manifolds are deembedded and S-parameters for each of the manifolds in the form of 2-port S-parameter files are obtained using on-wafer Thru Reflect Load (TRL) deembedding [29], [30]. The extrinsic-level measurements, obtained after deembedding the manifolds, are henceforth employed for parameter extraction. We start with the intrinsic element extraction following the standard low-frequency Y-parameter based approach [31]. It must be

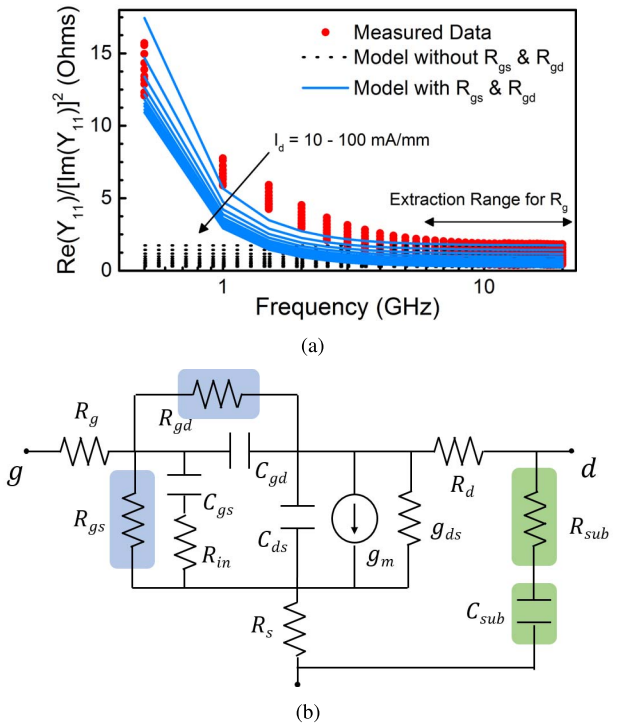

FIGURE 8. Large resistors R_{gs} and R_{gd} are included in the intrinsic SS − EC to capture the differential gate resistance accounting for current flowing through the gate-source and gate-drain Schottky diodes respectively. Their inclusion significantly impacts the overall gate resistance (R_g) at low frequencies as shown in Fig. 8(a). R_{sub} and C_{sub} are included to capture the substrate loss at the output port. It must be noted that AR resistances R_s and R_d have been omitted since their impact is already embedded in g_m and g_{ds} as described in Section III.

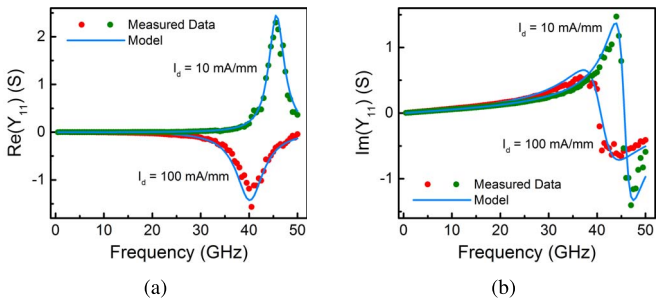

FIGURE 9. Comparison between modeled and measured broadband extrinsic-level Y-parameters. Y_{11} are shown here for illustration. The model accurately captures the peaks and dips and their bias dependence which is a manifestation of the interaction between the intrinsic capacitances and the extrinsic inductances. The values of bus-inductances can be fine-tuned to fit the peaks/dips in measured and modeled extrinsic-level Y-parameters.

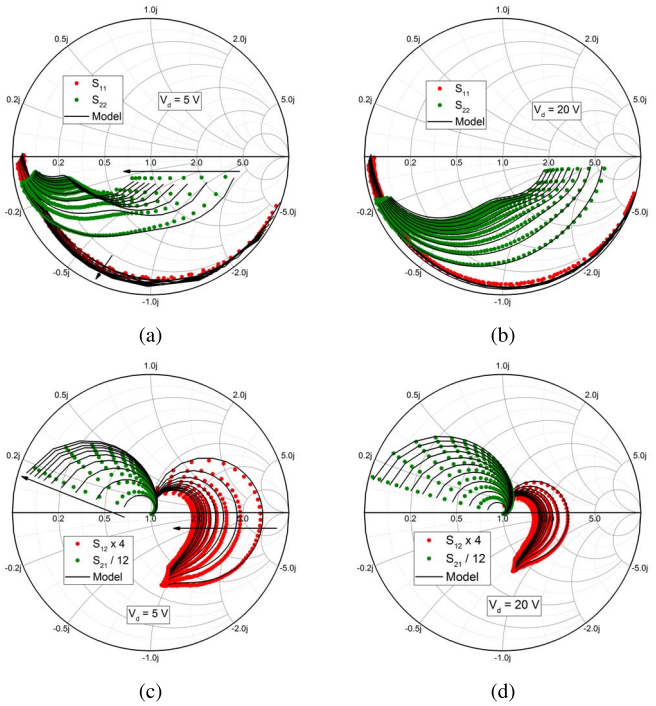

FIGURE 10. Comparison between modeled and experimentally measured data of broadband extrinsic-level S-Parameters for frequency 0.5 – 50 GHz. Smith plots for S_{11} and S_{22} (a–b), S_{12} and S_{21} (c–d) are shown for 2 different drain-bias conditions, with 10 different gate biases (I_d = 10 – 100 mA/mm) for each drain condition. The model is accurate in capturing the bias dependence of S-parameters which validates the accuracy of the core intrinsic model as well as the RF parameter extraction procedure. The kink-effect in S_{22} is very well reproduced by the model, which highlights the excellent modeling of the intrinsic characteristics of the device [33]. The arrows indicate the direction of increasing I_d.

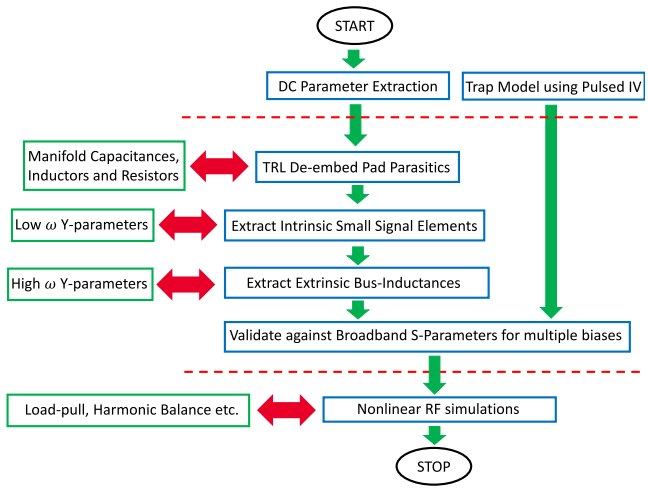

FIGURE 11. RF Parameter extraction flow as described in Section V to extract the RF small signal model for the GaN device. The flow is straightforward and does not require any optimization and is validated by accurate correlation between measured and modeled broadband S-parameters as shown in Fig. 10.

noted that due to the inclusion of the AR model in the core model, as explained in Section III, we can use it to our advantage by omitting R_s and R_d from the intrinsic SS − EC since their effect on g_m and g_{ds} is already captured. This significantly simplifies our hand-analysis for RF parameter extraction without compromising on the accuracy due to omission of AR resistances as reported in [31].

The overlays of measured and modeled plots for intrinsic SS − EC elements plotted against frequency are shown in Fig. 7. The values of the parasitic capacitances are adjusted to settle the levels of the capacitance plots, whereas the trap-model takes care of the g_{ds} dispersion. The only dispersion

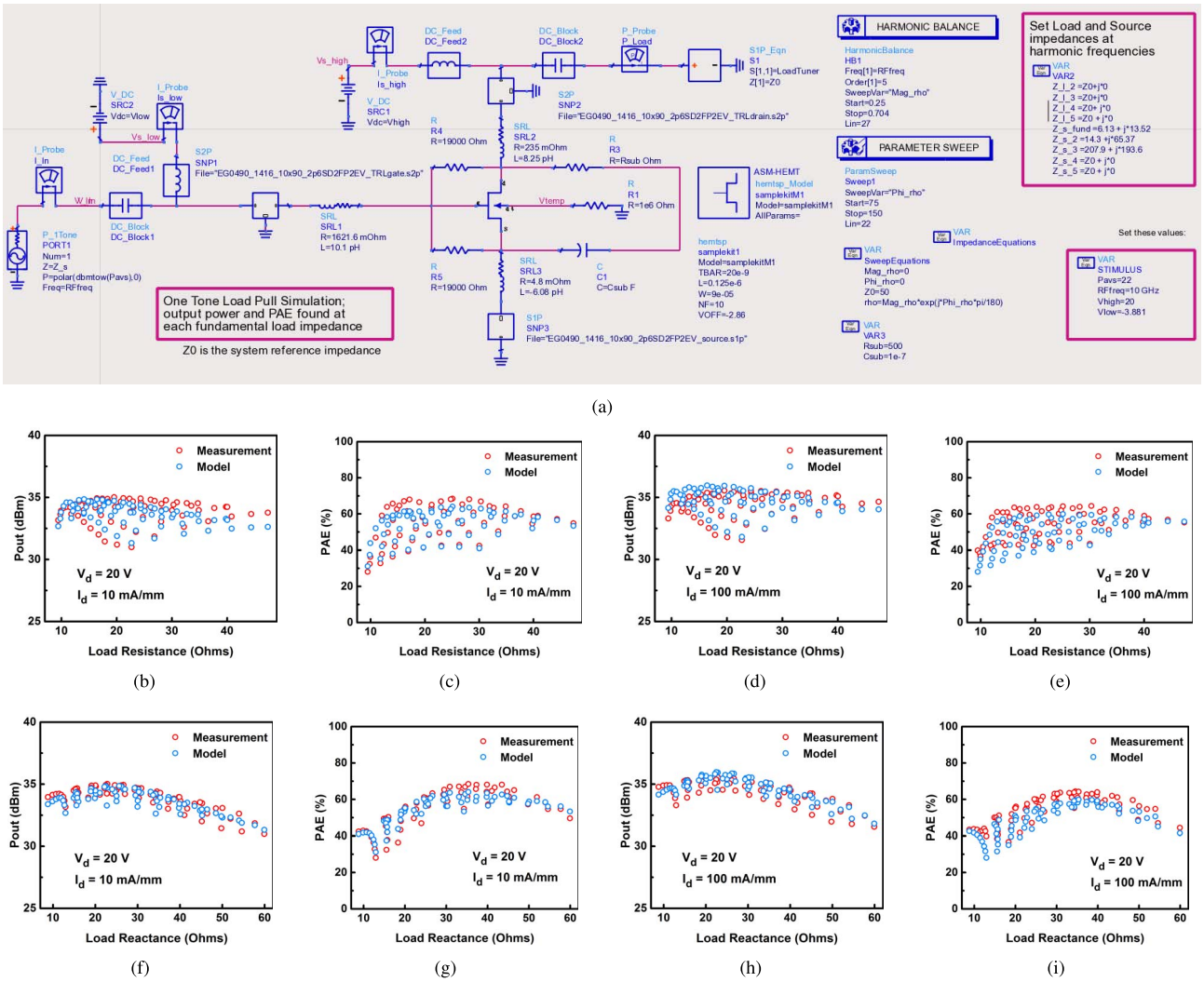

FIGURE 12. (a) ADS schematic for simulating load-pull contours using the embedded model. Pad level parasitics in the form of 2-port S-parameter components are added. Right in the centre is the DUT which is governed by the ASM-GaN-HEMT PDK. (b-i) Discrete load-sweeps for P_{OUT} and PAE against real and imaginary loads for multiple bias conditions, at 10 GHz signal frequency. The model accurately predicts the P_{OUT} and PAE maxima as well as their mutual tradeoffs upon varying the load resistance/reactance.

in g_m at low frequencies in our model is due to self-heating, and decided by the values of self-heating parameters R_{TH0} and C_{TH0}. However, their bias dependence is already taken care of by the core surface-potential-based model. The quasi-independence of these elements against frequency, which is a standard benchmark to verify the validity of the proposed RF model, is observed for nearly 10 GHz giving us a significant extraction range before which inductive effects come into the picture.

It must be noted that R_g increases abruptly as we move to lower frequencies (see Fig. 8(a)), which can be ascribed to the differential gate-channel resistances seen in GaN devices due to current flowing through gate-source and gate-drain diodes [32]. We model it by including large resistors R_{gs} and R_{gd} across gate-source and gate-drain terminals as shown in Fig. 8(b). Nonetheless, we still find a substantial frequency range for extraction of gate finger resistance $R_{g,f} = R_g - R_{g,i}$ as illustrated in Fig. 8(a). The extracted values of parasitic capacitances and resistances are shown in Table 2.

Substrate loss is captured using the standard RC series network across the drain and source nodes as shown in Fig. 8(b). The substrate network affects the g_{ds}-dispersion observed at low frequencies which in turn affects S_{22} of the device. Ideally, the time constant corresponding to the RC substrate network should be determined by low frequency Y-parameters. Since the broadband S-parameter measured data for the device at our disposal starts from 500 MHz, we therefore cannot extract the exact values of R_{sub} and C_{sub}. So, a convenient time constant is chosen such that it accounts for gds-dispersion well below 500 MHz while giving the best fits at the same time. In our case, its value was set to 50 μs or 20 kHz.

It is interesting to note that the extrinsic inductances and the bias-dependent intrinsic capacitances resonate at higher

TABLE 2. Extracted capacitances and resistances.

$C_{GS,p}$	$C_{GD,p}$	$C_{DS,p}$
510 fF	165 fF	182 fF
$R_{g,f}$	R_{gs}	R_{gd}
0.5Ω	19kΩ	19kΩ

TABLE 3. Bus-inductances (pH).

L_{xg}	L_{xs}	L_{xd}
10.1	−6.08	8.25

frequencies, a manifestation of which is the occurrence of dips and peaks in extrinsic-level Y-parameters, as shown in Fig. 9 as an illustrative example. These features can be used to extract the bus-inductances, tabulated in Table 3, in order to match the peaks corresponding to measured and modeled Y-parameters. As can be seen, the model is highly accurate in capturing the resonating behavior for multiple bias conditions due to varying capacitances with bias, thereby acting as an alternate way of validating the model extraction procedure. The negative value of L_{xs} can be ascribed to an improper calibration or de-embedding of the pad parasitics.

To conclude the RF parameter extraction process, overlays of the broadband S-Parameters for a frequency range of $0.5 - 50$ GHz are shown in Fig. 10. The results shown are for 20 different bias conditions: 5 V and 20 V at drain with 10 different voltage values at gate, that give a quiescent current spanning over an order of magnitude ($10 - 100$ mA/mm). A high level of correlation between the measured data and the model for a wide variety of bias conditions is observed, which is an important model capability as far as design of various PA classes under varying drain supply voltages is concerned. Also, the model is accurate in predicting the bias-dependence of the kink-effect in S_{22}, which can be of significance in design of the output matching network for PAs [34]. The entire parameter extraction flow is straightforward and does not require any optimization algorithms as is summarized in Fig. 11.

VI. LARGE-SIGNAL MODEL BEHAVIOR

To examine the large-signal performance of the proposed model, correlations between measured and model generated Output-Power (P_{OUT}) and Power-Added-Efficiency (PAE) load-pull plots are made. Shown in Fig. 12(a) is the ADS load-pull schematic using the model PDK and device extrinsic components. The measured load-pull data is obtained using load tuners from Focus Microwaves with an input-power (P_{IN}) level of 22 dBm at 10 GHz fundamental frequency. To get a deeper clarity on the impact of load impedances on P_{OUT} and PAE, the load-pull data reinterpreted into discrete load sweeps is compared for both measured data and model estimations in Fig. 12(b)–12(i). The variation of P_{OUT} and PAE and their mutual trade-offs as real and imaginary parts of the load are swept is captured accurately by the model.

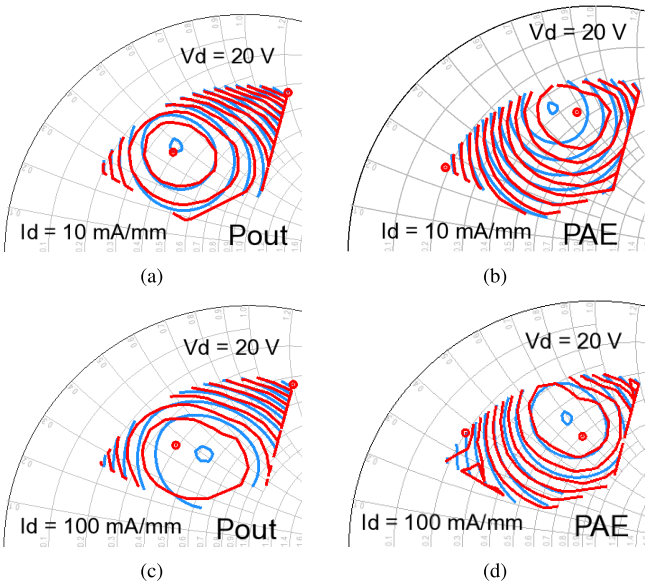

FIGURE 13. Comparison of measured and modeled P_{OUT} (a, c) and PAE (b, d) load-pull contours for $V_d = 20$ V at two current densities $I_d = 10$ and 100 mA/mm. The smith chart region is sampled for $0.26 <$ Magnitude(Γ) < 0.71 and $70° <$ Phase(Γ) $< 160°$ for standard 50 Ω impedance. The model accurately predicts the P_{OUT} and PAE maxima as well as their mutual tradeoffs upon varying the load impedance. Red Contours: Measured data, blue contours: Model.

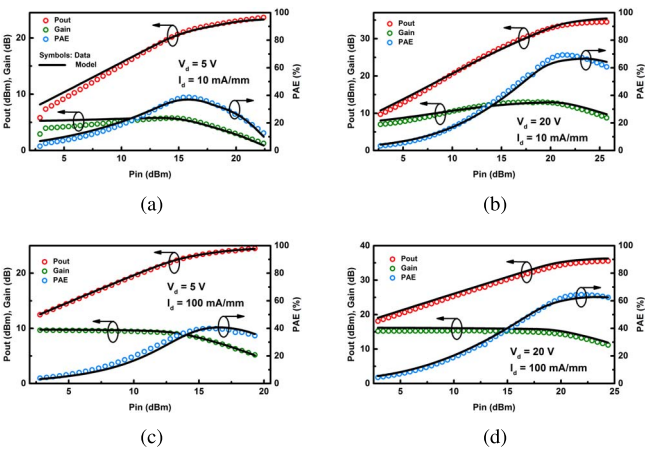

FIGURE 14. Comparison between modeled and measured P_{OUT}, Gain and PAE as functions of available input power (P_{IN}) for $V_d = 5$ and 20 V with two gate bias conditions $I_d = 10$ and 100 mA/mm. The frequency of the 22 dBm RF input signal is 10 GHz and the values of the load impedances are set for maximum PAE. Gain-compression is accurately reproduced by the model, which indicates an accurate non-linear model.

Given in Table 4 are the values of optimum load impedances obtained through load-pull contours for maximum P_{OUT} and PAE under different gate bias conditions. In Fig. 13(a)–13(d), the overlays for measured and modeled contours exhibit high degree of resemblance which highlights the capability of the proposed model to capture the non-linear nature of GaN HEMTs responsible for predicting P_{OUT} and PAE. Since the load-pull data is measured at pad-level, the model representation requires us to append the extracted manifolds from Section V to

TABLE 4. Load impedances.

	Freq	10 mA/mm	100 mA/mm
Max. PAE	f_0	$22.46 + j38.54$	$30.53 + j34.35$
	f_1	$40.61 - j93.39$	$37.32 - j73.44$
	f_2	$11.39 - j0.07$	$14.77 + j10.83$
Max. P_{OUT}	f_0	$19.57 + j22.83$	$19.57 + j22.83$
	f_1	$253.48 - j65.72$	$253.48 - j65.72$
	f_2	$15.66 - j31.21$	$15.66 - j31.21$

the extrinsic-level model in the ADS simulator as shown in Fig. 12(a).

Finally, power-sweep simulations are performed to study the model performance when the device is driven into compression as shown in Fig. 14. The load impedances are set for maximum PAE. The model does a decent job in predicting the non-linear behavior of the device particularly gain compression after the device hits the non-linearity and the subsequent peaking of PAE at power back-off. Such accuracy is achieved for multi-bias conditions with the help of precise modeling of trapping and self heating phenomena during large signal operation. These results indicate the readiness of the model to be used as an industry standard for GaN HEMT based state-of-the-art RF circuit design.

VII. CONCLUSION

A surface-potential-based RF large-signal model for GaN HEMTs was demonstrated and successfully validated against measured data for a commercial GaN device. It was shown that fitting the model for DC-IV characteristics would automatically generate the small-signal equivalent circuit for RF simulation due to the self-consistency between the device intrinsic charges and current, except for the extraction of parasitic capacitance and gate resistance, which need to be extracted using standard procedures. Additionally, trapping effects were modeled using RC circuits and broadband S-parameters were used to validate the RF model. Furthermore, the model capability to predict load-pull contours and their corresponding maxima for varying load-impedances was shown, which could be handy for an accurate first-pass power amplifier design.

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