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Effect of Charge Retention of Non-Volatile Memory TFTs Under Multiple Read Cycles

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ABSTRACT A hydrogenated amorphous silicon thin-film transistor with an engineered charge-trapping interface between the gate dielectric and the channel layer is fabricated to realize non-volatile memory. The memory devices possessed a large memory window and good endurance with an estimated 5-year lifetime. The charge retention lifetime under persistent read bias conditions was found to be ~50% less compared to floating conditions. Measured results indicate the importance of continuous read cycles for estimating the device lifetime and the need for a larger memory window to extend memory operation lifetime.

INDEX TERMS Hydrogenated amorphous silicon (a-Si:H), thin-film transistor (TFT), non-volatile memory, charge trapping.

I. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) are the basic elements for large-area electronic systems [1]. Having a non-volatile memory embedded into the a-Si:H TFT can enhance the functionality of applications such as flat-panel displays and image sensor arrays. Memory devices, exploiting the charge-trapping characteristics of thin-film interfaces can be used to create non-volatile memory that is easily integrated with existing fabrication processes [2], [3].

There have been reported charge-trapping non-volatile memory devices using a-Si:H TFT technology [4], [6], [7]. Kuo and Nominanda [4] have presented a floating-gate a-Si:H TFT using an etch-stop process with a thin a-Si:H layer (7 nm) as the charge-trapping medium. Trapped charge within the medium results in a threshold voltage change (ΔV_t) in the TFT that results in a programmed/written memory state. The ΔV_t may also be negative when electrons are released from the charge-trapping medium. This process creates the erased state. The difference between the threshold voltage (V_t) after programming and V_t after erasing is the memory window (M_W) of the device. In their implementation, charge retention (CR) characteristics under floating conditions were achieved for over 3,600 seconds [4]. However, the floating-gate memory TFT often suffers from the impact of drain-gate overlap capacitance (C_{ov}). The influence of C_{ov} leads to a ΔV_t dependence on the drain voltage (V_{ds}). This effect has greater impact on emissive displays where the brightness of the pixel depends on the drain current (I_{ds}) [5]. This C_{ov} effect was explained by Huang *et al.* [6] where an engineered defect layer was introduced between the amorphous silicon nitride (a-SiN_x) gate dielectric and the a-Si:H channel layer. They reported the memory behavior of the TFT with a CR of over 10 years under floating conditions. Choi *et al.* [7] also demonstrated a hydrogenated-amorphous-silicon germanium (a-SiGe:H) non-volatile memory TFT using a trilayer oxide stack (OO_XO_N) charge-trap layer. They showed that with a 20% Ge content, 58% of the initial trapped charge remained even after 10 years compared to a device without Ge.

The previous research characterized the CR of the memory TFT based on floating conditions with an estimated lifetime of ~10 years. However, in many applications such as flat-panel displays, when memory is integrated as a driver in a pixel circuit as proposed in [8], to reduce excess refresh cycles, the memory device is read periodically to display certain information. The driving scheme utilized to read can influence the stability of the memory device, and thereby

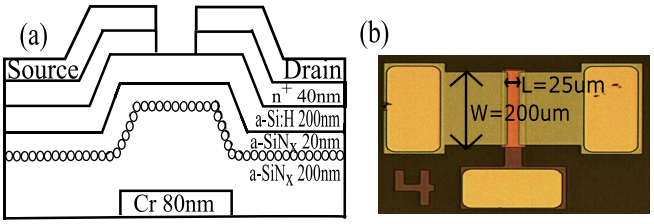

FIGURE 1. **(a) Schematic cross section of charge-trapping TFT (not drawn to scale) and (b) Optical microscope image of the fabricated bottom gate charge-trapping TFT.**

affect the CR and lifetime of the pixel under practical conditions compared to floating conditions. Hence, persistent read bias (PRB) is essential to determine the realistic lifetime of a memory device.

a-Si:H TFT structures with an engineered charge-trapping layer inserted into the a-SiN_x gate dielectric similar to [6] were fabricated to examine the effect of read-write cycles on the memory lifetimes. CR of memory devices was tested under floating conditions followed by PRB conditions. The PRB lifetime is experimentally derived to demonstrate the effectiveness of the drive scheme on memory lifetime and reliability. We show that the operational lifetime of charge-trapping memory TFTs strongly depends on the operation of the device under PRB conditions compared to floating conditions.

II. DEVICE FABRICATION

Bottom-gated a-Si:H memory TFTs (Fig. 1) with a charge-trapping layer were fabricated based on a standard back-channel etched (BCE) process. A previous report [6] used an etch-stop structure with a thin 100 nm control a-SiN_x. In our approach, the TFT was a BCE structure, employing a 200 nm thick a-SiN_x gate dielectric. The TFT process started with sputtering of a 80 nm Cr to pattern the bottom-gate metal. Next, a 200 nm a-SiN_x gate dielectric was deposited and followed by deposition of a thin 10 nm a-Si:H layer using 13.56 MHz plasma-enhanced chemical vapor deposition at 260°C. The thin a-Si:H layer was then completely dry-etched to create a defective interface on top of the gate dielectric surface. A trilayer of 20 nm a-SiN_x tunnel gate dielectric, 200 nm a-Si:H channel, and 40 nm n^+ a-Si:H ohmic contact layers was deposited consecutively at 260°C. After patterning the TFT active area by dry etching, 200 nm Al/Cr bilayer source/drain (S/D) metals were sputtered and patterned. The n^+ a-Si:H was then dry etched using the S/D metal as a mask to define the effective channel region followed by a gate contact opening. Here, 20-30 nm a-Si:H was intentionally over-etched to confirm complete n^+ a-Si:H etching. The TFTs were finally annealed in vaccum at 180°C for 2 hours before the measurements.

III. MEASUREMENT RESULTS AND DISCUSSION

Fig. 2 shows the transfer (I_{ds} vs. V_{gs}) characteristics of the memory and reference TFTs. Both the TFTs are programmed

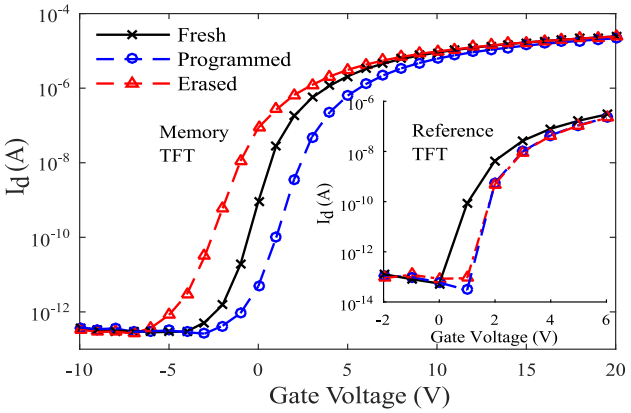

FIGURE 2. **Transfer characteristics of the memory and reference TFTs showing fresh, programmed and erased state. The program voltage = +30 V and erase voltage= −30 V for 10 s.**

and erased, with the S/D nodes grounded, by applying a gate voltage (V_G) of +30 V and −30 V for 10 seconds, respectively. In the memory TFT, a +30 V bias was applied to the gate, to create a positive V_t shift. A -30 V bias was applied to negatively shift V_t resulting in a M_W of 3 V (Fig. 2). The reference TFT shows a ΔV_t of 0.7 V upon programming due to the electrical instability of a-Si:H TFT under constant gate bias [9]. However, on erasing, the V_t stays constant, negating the memory behavior. This behavior demonstrates the memory operation due to trapping and de-trapping within the engineered defect layer in the memory TFT. The memory device shows good electrical properties with an I_{on}/I_{off} ratio of 10^8 and a sub-threshold swing (SS) of 500 mV/dec. The SS after programming as well as after erasing was found to be 700 mV/decade. This observation may be either due to the contribution of defect creation at the a-Si:H/a-SiN_x channel interface during the programming (erasing) condition as well as the charge-trapping (detrapping) into (from) the medium. However, since the SS did not change for both the conditions, we assume the dominant mechanism to be charge-trapping rather than defect creation in the memory devices.

The memory behavior due to programming and erasing started to show for V_G > +/- 20 V and the M_W increased with increasing V_G. This change allows the device to be able to be programmed (positive gate bias) and erased (negative gate bias) at relatively low voltages. At higher voltages of +/- 50 V, a large M_W of 8.6 V was observed and chosen as the default V_G for programming and erasing. In addition, the M_W for various bias times under the programming and erasing voltages of +/- 50 V was also analyzed to find the influence of time on the M_W as shown in Fig. 3. The M_W was observed to increase between 1 sec and 15 sec. The V_t shift after 15 sec began to saturate, suggesting the complete filling of traps within the defect medium.

The room-temperature CR characteristics of the memory TFT are shown in Fig. 4. While the device was kept floating, V_t was measured periodically for ~60 days. The initial M_W

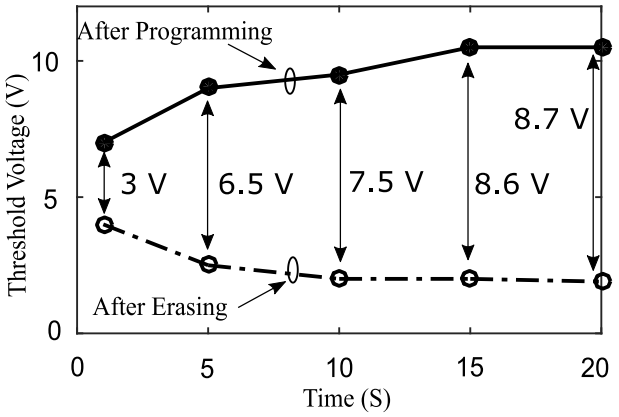

FIGURE 3. **The time dependent ΔV_t for programming and erasing voltage at +50 V and −50 V, respectively. The M_W varied between 3 and 8.7 V.**

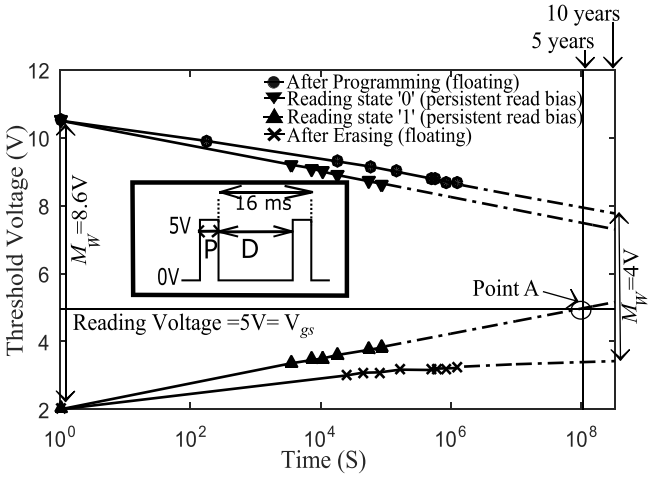

FIGURE 4. **Charge retention characteristics of the memory device on the glass substrate at room temperature (27°C) measured during floating conditions and PRB conditions. The dotted lines are extrapolated from measured data points. The inset shows the timing waveform of the gate input signal followed for reading state '1' and state '0'. P represents the programming phase which is 'ON' for 250 μs and D represents the driving phase which is 'OFF' for the remaining period (16 ms). The memory is lost when $V_t = V_{gs}$ (at Point A).**

after programming and erasing was 8.6 V and started to decrease with time due to the charge loss from the release of trapped charge. Memory lifetimes were determined through extrapolation [10] of the M_W and was calculated to be 4 V after 10 years with a charge loss rate of ~54%.

The impact of PRB conditions on the memory device was subsequently analyzed by reading one bit of information, represented by state '0' and state '1'. The overall lifetime of the non-volatile memory device was calculated based on the driving scheme used in display applications [5]. A voltage less than the V_t after programming represented the state '0' and a voltage greater than V_t after erasing was state '1'. The measurements were carried out with the gate input signal (Fig. 4) produced using a Tektronix AFG3052C function generator. The maximum (ON) and minimum (OFF) amplitude of the signal was +5 V and 0 V, respectively. The period of the signal was set to 16 ms to simulate a 60 Hz refresh rate in a display. Considering a 64 × 64 pixel array, the programming phase was 'ON' for 250 μs and 'OFF' during the remainder of the period for the driving phase. The TFT was connected using a probe station to the measuring equipment and the entire test was carried out in the dark. The I_{ds} was converted to a voltage signal using a two-stage operational amplifier configuration. At first, the TFT was programmed at +50 V for 15 sec resulting in a $\Delta V_t = 6.6$ V. The state '0' was read in saturation mode for 24 hours by applying a gate to source voltage (V_{gs}) of +5 V and a V_{ds} of +5 V. The TFT was erased by applying -50 V for 15 sec and state '1' was read in the same way for 24 hours.

The CR characteristics of the memory TFT under PRB conditions are also shown in Fig. 4. The results show that the V_t when reading state '1' increased more compared to the measurements under floating conditions (Fig. 4). On reading state '1', the gate is biased for every 16 ms at a voltage greater than the V_t of the device (inset of Fig. 4), due to erasing. It leads to the bias dependence instability issues of a-Si:H TFT [9], [11] thereby causing an increase in V_t. This eventually leads to a decrease in the M_W. Extrapolating shows that V_t crosses +5 V in about 5 years (Point A). Beyond this point, the stored memory is lost as the V_t becomes comparable to the V_{gs}. This results in almost 50% decrease in lifetime from measurements taken under floating conditions. The results demonstrate the negative impact of continuous read cycles on the device lifetime. The impact could be more severe with a device having a narrow initial M_W and the device lifetime is subjected to change with respect to the applied reading voltage. Table 1 provides a summary of our measurement results along with the recently published papers [4], [6], [7].

TABLE 1. **Summary of results.**

Reference	Dielectric thickness (nm)	Applied electric field (V/m) P: Program, E: Erase	Stress time	Initial M_W (V)	CR	
					Floating	PRB
Present Work	220	P: 22.7×10^7 & E: -22.7×10^7	15 s	8.6	~10 years	~5 years
[4]	~300	P: 3.3×10^7 & E: -3.3×10^7	1 s	0.7	~3600 sec	-
[6]	110	P: 31.8×10^7 & E: -25.9×10^7	10 ms	2.5	~10 years	-
[7]	37.5	P: -18.6×10^7 & E: 40×10^7	1 ms	6.75	~10 years	-

The M_W of a device is a function of various parameters such as dielectric thickness, applied electric field, and stress time. As apparent from the table, there is a wide ranging spread amongst these parameters reported by different groups. However, for a given dielectric thickness, the M_W is proportional to the applied electric field and stress time. For example, in [6], the stress time is in msec, but the thick dielectric induces small initial M_W despite high applied electric field. Similarly, [4] has stress time in seconds, but the thick dielectric and low applied electric field lead to very small initial M_W. The researchers in [7] achieved excellent

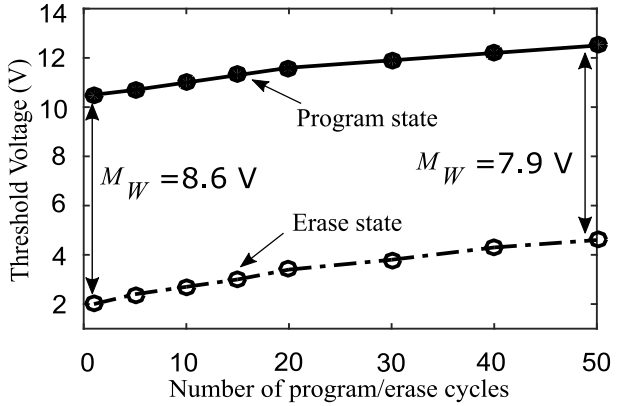

FIGURE 5. Endurance behavior of the memory TFT. The TFT was programmed and erased by applying V_G =+50 V and V_G=-50 V for 15 s, respectively.

initial M_W with msec stress time under very thin dielectric and high electric field.

Additionally, as illustrated in Fig. 3, we could achieve an initial M_W of 3 V for the stress time of 1 second. Moreover, we believe that the stress time can further be optimized given application requirements. However, in our study we highlighted that high initial M_W is important for a memory device operating under realistic reading circumstances. For example, the lifetime of a memory device changes significantly from floating to PRB conditions.

Figure 5 shows the endurance characteristics of the memory TFT where the device was programmed and erased continuously for 50 cycles. Both the V_t for programming and erasing cycles was observed to increase while the memory window slightly decreased. This observation may result from residual charges that are trapped in the deep states of the control a-SiN_x. The erase voltage applied might not be sufficient to remove the residual charges that result in the small increase in V_t [12]. However, the M_W after 50 cycles was reduced by only 0.7 V without affecting the reading voltage. This result implies that the memory device is reliable for multi-time programmable applications.

IV. CONCLUSION

In this work, a non-volatile memory TFT was fabricated using a standard process to introduce an engineered defect layer in the TFT structure. The memory device exhibited a good M_W, CR, and endurance. The impact of continuous read cycles has been demonstrated and it was shown that the overall lifetime of a charge-trapping memory device strongly depends on the PRB conditions. The results also suggest that a larger M_W results in longer device lifetime under PRB conditions. The lifetime of the memory devices is estimated to be ~10 years under floating conditions and ~5 years under realistic PRB conditions.

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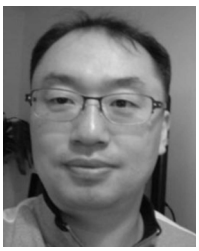

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