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Dimension Effect on Breakdown Voltage of Partial SOI LDMOS

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ABSTRACT Dimension effect on breakdown voltage (BV) of lateral double-diffused metal–oxide–semiconductor field-effect transistor in partial silicon-on-insulator (PSOI) technology is comprehensively studied. The maximum BV (BV_{max}) is examined under various settings of the device length L and the active silicon film thickness t. It is shown that there exists an optimal pair of (L, t) for PSOI at which the highest BV can be achieved. The ratio of L/t is better chosen between 5 and 7 for the device designs, in particular, $L/t = 6$ can be considered as the optimal one theoretically. Moreover, impacts of the silicon window length L_w and the drift doping concentration N_{dr} on the BV, the on-resistance (R_{on}) and the figure-of-merit ($=BV^2/R_{on}$) are also carefully studied.

INDEX TERMS LDMOS, partial silicon-on-insulator (PSOI), breakdown voltage, on-resistance.

I. INTRODUCTION

Lateral double-diffused metal-oxide-semiconductor (LDMOS) field effect transistor has been attracting a great deal of attention as a promise candidate of high-voltage power devices for integrated circuit (IC) applications [1]–[4]. Partial silicon-on-insulator (PSOI) has better thermal capability and higher breakdown voltage (BV) than silicon-on-insulator (SOI), and is thus introduced in the LDMOS design for better device performance [5], [6]. Recently, more improved structures based on the PSOI technology have been proposed to enhance the device performance further [7]–[11].

However, the impact of the silicon film thickness (t) on BV is rare to be discussed for PSOI LDMOS, while the device length (L) or the drift region length (L_{dr}) is barely referred in [12] and [13]. In [12], the devices with various L_{dr} were studied, but L_{dr} was treated only as an auxiliary parameter without any related discussion. In [13], the dependence of BV on (L, t) was studied for a novel PSOI. However, the doping profile in the silicon film for the novel PSOI was directly borrowed from the SOI structure, and the substrate-sustained voltage V_{sub} was assumed to be zero as the same as SOI. For the PSOI proposed in [13], V_{sub} can be ignored in comparison to BV. For conventional PSOIs, however, V_{sub} takes a considerable part of the BV, and thus the assumption of zero V_{sub} does not hold any more. Consequently, the conclusion from [13] is no longer valid for conventional PSOIs.

The conventional SOI film thickness can range from 2 μm to 20 μm. It is an important design aspect how to select the film thickness t in the PSOI designs. In the device design, it is generally expected that a smaller device would have an equivalent or even better performance than a larger device. However, thin-film (or short) LDMOS may remarkably degenerate unless other new technologies are adopted [14]–[16], which is often expensive and of poor quality. Thus, for conventional PSOIs with medium dimensions (i.e., L: 10 ∼ 100μm, t: 2 ∼ 20μm), the relationships between the performances (BV, R_{on}) and the size parameters (L, t) are highly desirable to be explored further and carefully.

Moreover, when L and t are fixed, the optimal drift doping concentration that corresponds to the optimal BV is actually not a constant. Instead, the optimal drift doping concentration is a function of the silicon window length L_w. This issue

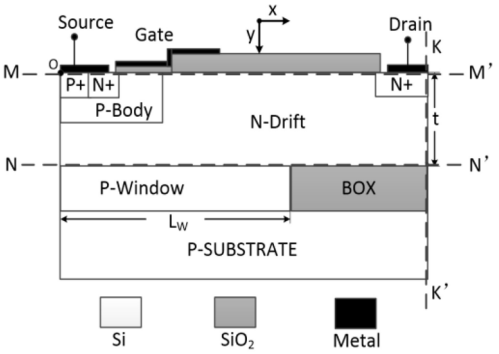

FIGURE 1. Schematic cross-section view of PSOI LDMOS.

is also an important design aspect in the PSOI LDMOS designs.

In this work, the PSOI LDMOS transistor is comprehensively studied under various device dimensions (i.e., different values for L and t) by Sentaurus TCAD. The maximum BV (BV_{max}) versus the dimension parameters L and t is carefully examined. It is shown that too thick or too thin SOI film can degrade BV_{max} for a given L. In addition, there exists a special correlation between the maximum BV and the ratio of L to t. It is further shown that, when L is fixed, the optimal silicon window length $L_{w,op}$ that corresponds to the optimal BV does not monotonously vary along with t either.

II. DEVICE STRUCTURE AND MECHANISM

The schematic cross-section view of PSOI LDMOS is illustrated in Fig. 1. The step gate and the field plate are adopted for the Reduce SURface Field (RESURF) effect. The length L_W of the p-type window, the original point and the axes are also shown in Fig. 1, and so do the locations of the MM', NN', and KK' cut lines. All the device geometrical and physical parameters used in the simulations are listed in Table 1. The substrate, source and gate electrodes are supposed to be grounded unless otherwise stated. It is assumed that the drift region is uniformly doped.

TABLE 1. Geometrical and physical parameters of devices.

Parameter	Value	Unit
Length of device (L)	50 ~ 120	μm
Length of drift region (L_{dr})	35 ~ 105	μm
Length of channel	5	μm
Length of window (L_W)	20 ~ 115	μm
Thickness of SOI	5 ~ 20	μm
Thickness of BOX	3	μm
Concentration of P-body	1×10^{17}	μm
Concentration of N-drift region (N_{dr})	4×10^{14} ~ 2.6×10^{15}	cm^{-3}
Concentration of P-substrate	2×10^{14}	cm^{-3}
Concentration of P-window	2×10^{14}	cm^{-3}

In a high-voltage device design, the maximum BV (denoted as BV_{max}) is the most important measure for performance. For PSOI LDMOS, BV is generally a function of four parameters: L, t, L_w and N_{dr}, denoted as $BV = f(L, t, L_w, N_{dr})$. When L and t are fixed, for any given L_w, there exists an optimal N_{dr} (denoted as $N_{dr,Lw}$) that corresponds to the maximum achievable BV (denoted as $BV_{max,Lw}$).

For all the L_w, the overall highest BV (denoted as BV_{max}) can be obtained as the largest one of all the $BV_{max,Lw}$. Herein, the optimal L_w and $N_{dr,Lw}$ that correspond to the overall highest BV (i.e., BV_{max}) are denoted as $L_{w,op}$ and $N_{dr,op}$, respectively. This implies that, once L and t are fixed, $L_{w,op}$ and $N_{dr,op}$ can be decided, and so does BV_{max}. As a result, BV_{max} can be defined as a function of two size parameters: L and t, i.e., $BV_{max} = f_m(L, t)$, in which L and t are independent variables.

The above process can be expressed as follows:

$$\begin{aligned} BV_{max} &= \max\left\{BV_{max,Lw} \middle| L_w \in (0, L)\right\} \\ &= \max\left\{\max\left[f\,(L, t, L_w, N_{dr}) \;\middle|\; N_{dr} \in R_{Ndr}\right)\right] \middle| L_w \\ &\qquad \in (0, L)\right\} \\ &= f\left(L, t, L_{w,op}, N_{dr,op}\right) \\ &= f_m\,(L, t) \end{aligned}$$

where R_{Ndr} represents the doping concentration range. In the initial step of a PSOI LDMOS design, only L and t need to be carefully selected, while L_w and N_{dr} can be ignored since L_w and N_{dr} are treated in the sequential design steps after L and t are decided, which avoids handling the four parameters simultaneously and thus greatly simplifies the design process.

III. STUDIES ON DIMENSION EFFECT

Fig. 2 depicts the vertical electric fields and the voltage distributions under the drain end (along KK') at $BV_{max,Lw}$ for PSOI LDMOS with $(L_W, N_{dr,Lw}) = (46\ \mu m, 1.46 \times 10^{15} cm^{-3})$, $(66\ \mu m, 1.42 \times 10^{15} cm^{-3})$ and $(80\ \mu m, 1.36 \times 10^{15} cm^{-3})$. The corresponding plots are denoted as curves A, B and C respectively. Curve B is the optimal curve with $(L_{W,op}, N_{dr,op})$ corresponding to BV_{max}. In Fig. 2, V_S, V_I and V_{Sub} denote the voltage drops across the SOI film, the buried oxide (BOX) layer and the substrate respectively. The breakdown voltage can be obtained via the equation: $BV = BV_{ver} = V_S + V_I + V_{Sub}$ [11], [17].

It can be seen in Fig. 2(a) that, as L_w increases, the vertical electric fields decrease in both the SOI film and the BOX layer. It is due to the fact that the electric fields induced into the SOI film and the BOX layer by N_{dr} are both in proportional to $N_{dr,Lw}$, which decreases as L_w increases.

However, the electric field in the substrate increases as L_w grows. When L_w increases, although $N_{dr,Lw}$ decreases, the carriers in the drift region can still more easily flow through the silicon window into the substrate, and thus the depletion can penetrate deeper into the substrate. Consequently, there are more fixed charges in the depletion layer of the substrate, which can induce higher electric field in the substrate. Additionally, it can be found that L_w dominates the electric field in the substrate, but not $N_{dr,Lw}$.

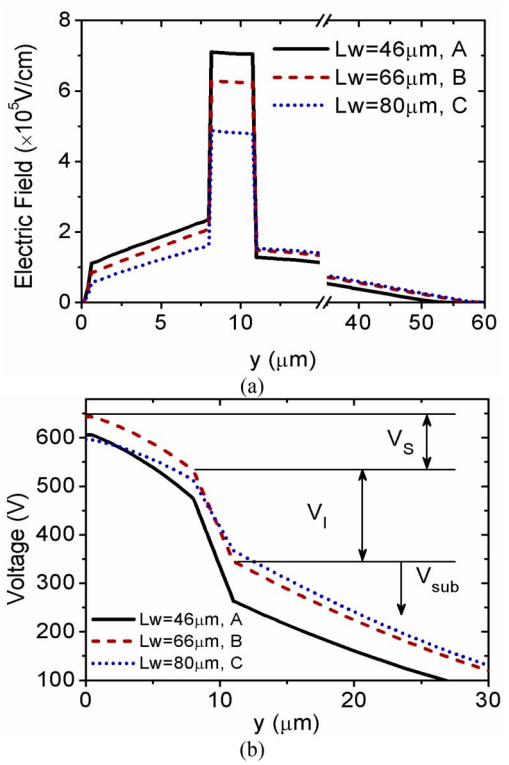

FIGURE 2. (a) Vertical electric field and (b) vertical voltage distribution under the drain end (along KK') at $BV_{max,Lw}$ for PSOI LDMOS with L_W = 46 μm, 66 μm and 80 μm, respectively. (L = 90μm, t = 8μm).

In Fig. 2(b), it is shown that the highest BV is achieved in curve B while the lowest BV occurs in curve C. Although V_S and V_I are higher in curve A (i.e., V_S = 131 V, V_I = 211 V) than those in curve B (i.e., V_S = 110 V, V_I = 187 V), V_{Sub} is much higher in curve B (i.e., 345 V) than that in curve A (i.e., 263 V). Consequently, BV from curve B (i.e., 642 V) is higher than that from curve A (i.e., 605 V). A similar analysis can be applied to curve B and curve C, and shows that BV from curve B (i.e., 642 V) is higher than that from curve C (i.e., 594 V).

From the above discussions, it can be found that, along the vertical direction, the silicon window plays a role of distributing V_S, V_I and V_{Sub} for PSOIs, especially "digging the substrate". As the constituent part of BV, V_{Sub} (or the substrate region) is the key factor to BV_{max} by comparison to V_S and V_I.

Fig. 3 shows lateral electric field distributions along the upper (along MM') and bottom (along NN') surfaces of the SOI film at $BV_{max,Lw}$. All the parameters of curves A, B and C are according to Fig. 2. In Fig. 3(a), it can be seen that peaks P1, P2 and P3 (of the upper surface) correspond to peaks P1', P2' and P3' (of the bottom surface), respectively. Along the upper surface, the electric field at the drain end from curve A is higher than that from curve B, while BV (the drain voltage) from curve B is higher than that from curve A. This implies that curve B has a better RESURF effect than curve A. When the silicon window is too close to the drain end, the RESURF effect induced by the peak point (e.g., P3) is degraded. This is why peak P3 is not conspicuous like peak P1 or peak P2. Thus, a better RESURF effect is achieved in curve B than that in curve C. In addition, different peak locations can result in different electric field increments, RESURF and thus different BVs. The larger the electric field increment is, the higher the corresponding BV achieves.

From another perspective, the RESURF effect can be readily determined by the tangents of the curves. As illustrated in Fig. 3(b), a tangent can be plotted for every curve. The more horizontal the tangent is, the better the RESURF effect is. However, this method can be better applied to the thin device (t < 10μm), since the peak at the upper surface (e.g., P1, P2 or P3) for the thick device is difficult to be observed from the electric field distribution curve. For the thick device (e.g., t = 15μm), the peak can be perceived when the device is very long (e.g., L > 100 μm).

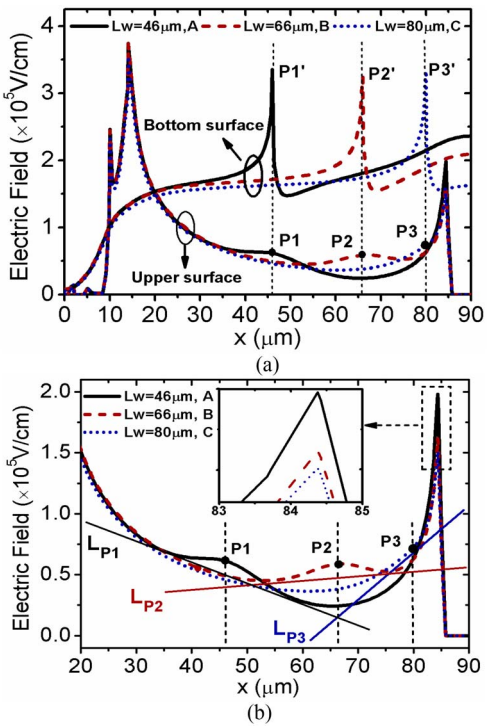

FIGURE 3. Lateral electric field distributions at $BV_{max,Lw}$ (a) the upper (along MM') and bottom (along NN') surface, (b) Tangents for three circumstances A, B and C.

Fig. 4 shows the dependences of BV on L_w for PSOI with various N_{dr}. The circle curve depicts "$BV_{max,Lw}$ versus L_w". At points A (L_W = 66 μm), B (L_W = 56 μm) and C (L_W = 75 μm), $BV_{max,Lw}$ is, respectively, achieved with $N_{dr} = 1.42 \times 10^{15}$, 1.44×10^{15} and 1.37×10^{15} cm^{-3}, in which the dependences of BV on L_w (i.e., "BV versus L_w") are also entirely depicted by the square, rhombus and triangle curves, respectively. Overall, the highest BV is reached at point A and thus point A represents ($L_{w,op}$, $N_{dr,op}$). Considering that the highest BV (L_W = 66 μm, at point

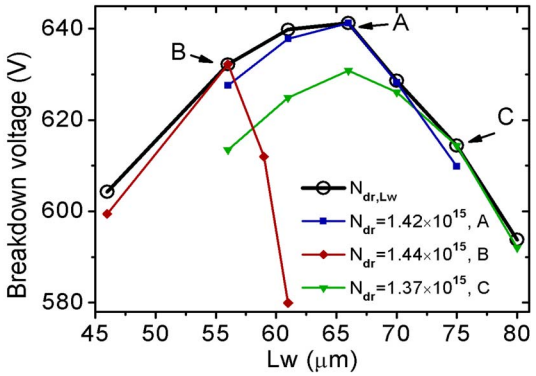

FIGURE 4. Dependences of BV on L_W for PSOI with various N_{dr}. ($L = 90$ μm, $t = 8$ μm).

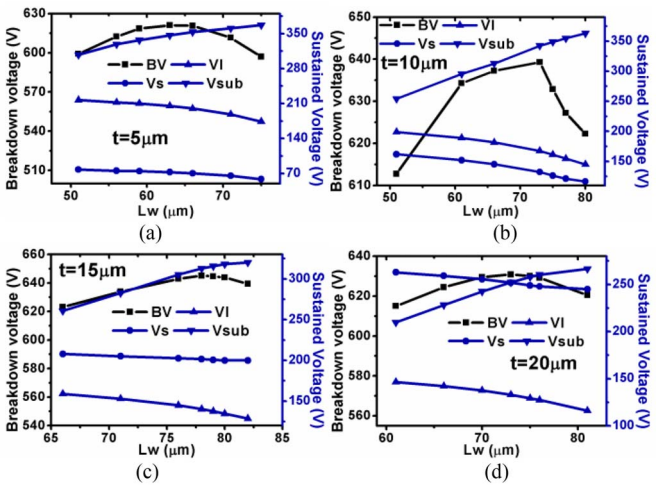

FIGURE 5. Dependences of $BV_{max,Lw}$, V_S, V_I, and V_{sub} on L_W for PSOI LDMOS with various t. ($L = 90$μm).

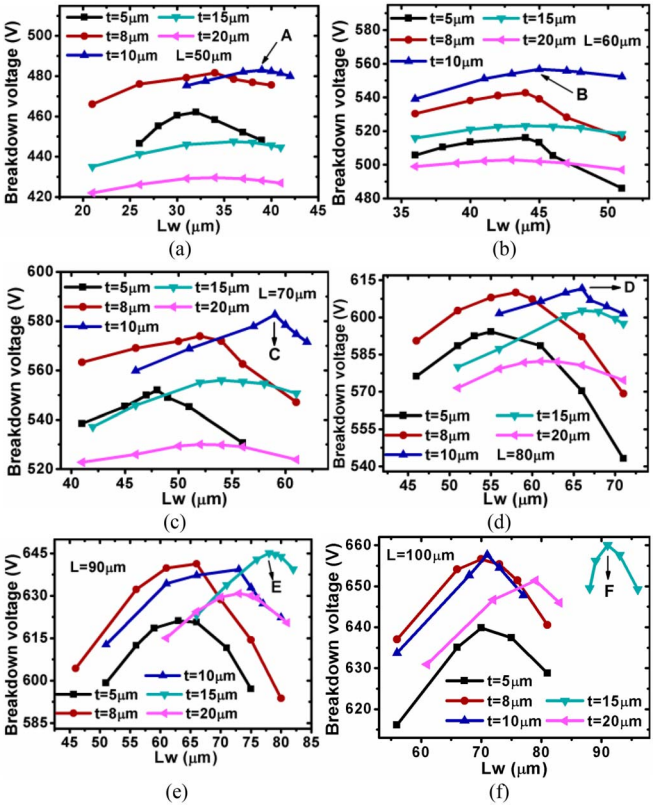

FIGURE 6. $BV_{max,Lw}$ versus L_W for PSOI with various L and t.

A) is sensitive to N_{dr} after $N_{dr} = 1.44 \times 10^{15}$ cm^{-3}, N_{dr} should be better selected less than 1.44×10^{15} cm^{-3} (e.g., $N_{dr} = 1.42 \times 10^{15}$ cm^{-3}). The lower limit of N_{dr} can be chosen as (1.44×10^{15} cm^{-3} $- \Delta N_{dr} \times 2$), where ΔN_{dr} is the process variation. This could provide a wider device design margin.

It can be observed in Fig. 4 that the square curve is close to the circle curve, while the rhombus and triangle curves are obviously much different from the circle curve. For different L_W, different N_{dr} is required to achieve the optimal BV. It can also be seen that the L_W-bandwidth of the rhombus (triangle) curve is narrower (wider) than that of the square curve. It is due to the fact that the RESURF effect and BV are sensitive to N_{dr}. The larger N_{dr} is, the more violently BV changes along with L_W. For the circle curve, every point corresponds to $BV_{max,Lw}$, implying that the best REUSRF effect and the highest BV are achieved at each given L_W and thus the L_W-bandwidth of the circle curve is the widest among all the curves.

Fig. 5 shows the dependences of $BV_{max,Lw}$, V_S, V_I, and V_{sub} on L_w for the PSOI LDMOS with various t. In Fig. 5, it can be seen that, for all the t values, the tendency of every curve keeps consistent. As L_w increases, V_S and V_I always decrease, while V_{sub} increases all the time.

In Fig. 5, it can be seen that $BV_{max,Lw}$ first increases and then decreases with increasing L_w, where the turning point is the overall highest breakdown voltage BV_{max} at ($L_{W,op}$, $N_{dr,op}$). It is due to the fact that, when L_W increases, V_{sub} almost uniformly increases while V_I deceases rapidly beyond $L_{W,op}$. The former is mainly because the depletion penetrates deep uniformly in the substrate as L_W increases. The latter is mainly due to the fact that, when L_W increases beyond $L_{W,op}$, the holes at the SOI/BOX interface can be easily swept into the substrate, and thus the number of holes decreases fast and the electric field (or voltage) decrease rapidly in the SOI film and the BOX layer.

In Fig. 5, it can also be observed that, when t increases, V_S obviously increases whereas V_I significantly decreases. The former is due to the fact that a thicker SOI film can sustain a higher voltage. The latter is because N_{dr} decreases for PSOI LDMOS with a fixed L when t increases, according to the REUSRF theory. Moreover, when t is larger (less) than 15 μm, V_{Sub} decrease (almost keep unchanged) as t increases. The highest BV is achieved when $t = 15$ μm.

Fig. 6 depicts $BV_{max,Lw}$ versus L_w for PSOI with various L and t. It is shown in Fig. 6 that, for a fixed L, $L_{W,op}$ first increases and then decreases as t increases. It is interesting that the largest $L_{W,op}$ corresponds to the highest BV among all t. The peak points A, B, C, D, E and F are labeled in

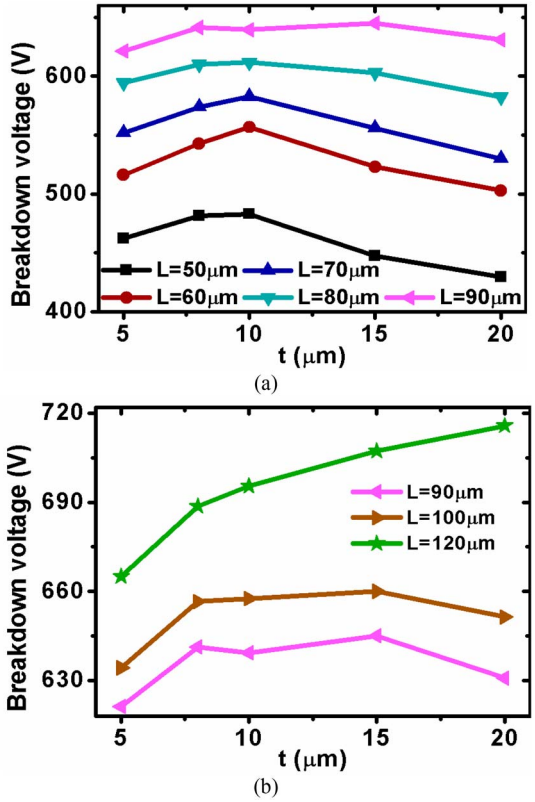

FIGURE 7. ***BV*$_{max}$ versus *t* for PSOI LDMOS with various *L*.**

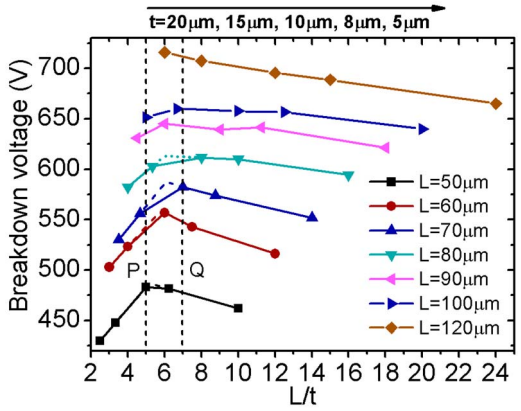

FIGURE 8. **Dependences of *BV*$_{max}$ on *L/t* for PSOI LDMOS with various *L*.**

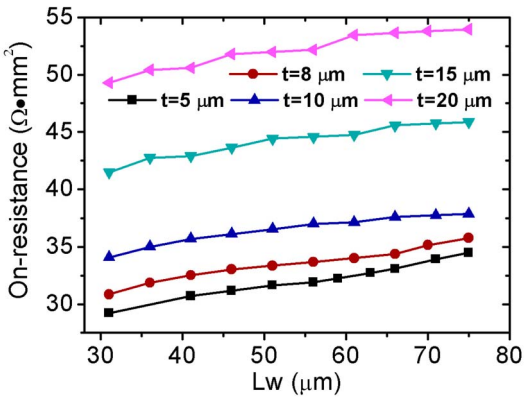

FIGURE 9. **Dependences of on-resistance on *L*$_{W}$ for PSOI at *BV*$_{max,Lw}$ with various *t*.**

Fig. 6, and the corresponding t is denoted as t_{best} for each peak point.

When $t < t_{best}$, the RESURF effect improves and thus $L_{W,op}$ increases with increasing t. When $t > t_{best}$, however, the RESURF effect degrades and thus $L_{W,op}$ decreases with increasing t. For the former, a larger $L_{W,op}$ results in a deeper depletion in the substrate while a smaller N_{dr} reduces the depletion in the substrate with a larger t. Consequently, the depletion varies little in the substrate and V_{Sub} almost keeps unchanged, due to the fact that the two effects counteract each other. For the latter, similarly, a smaller $L_{W,op}$ and a smaller N_{dr} both weaken the depletion effect in the substrate with a larger t, which reduces V_{Sub}. This is consistent with the description in Fig. 5.

In Fig. 6, it can also be seen that, as L decreases, the corresponding t_{best} decreases gradually (e.g., $t_{best} = 15$ μm for point E, $t_{best} = 10$ μm for point D), which is further illustrated in Fig. 7. Fig. 7 shows BV_{max} versus t for PSOI LDMOS with various L. In Fig. 7, one can observe that t_{best} is, respectively, 15 μm, 15 μm and 20 μm when $L = 90$ μm, 100 μm and 120 μm, whereas t_{best} becomes 10 μm as L is less than 90 μm. According to the trend in Fig. 7, it can be expected that t_{best} would be smaller than 10 μm as L decreases below 50 μm. This implies that dimensions L and t of the rectangular SOI film is important for achieving the highest BV for PSOI LDMOS.

In addition, as shown in Fig. 7, the breakdown voltage is a stronger function of L by comparison to t, since L decides the BV_{max} region that the device can achieve. However, when L is fixed, the specific largest value of BV_{max} is determined by t. Consequently, in order to achieve the highest BV, t also needs to be selected carefully. Thus, the ratio L/t is considered as a key design parameter.

Fig. 8 shows the dependences of BV_{max} on L/t for PSOI LDMOS with various L. In Fig. 8, it can be observed that the curves shift down and become sharper and narrower when L decreases. For all the curves, the highest BV_{max} is achieved between the ratio $L/t = 5$ and 7. From the intersection point of the dotted line for the curves, the best ratio L/t can be considered to be 6 for achieving the highest BV_{max}. During the practical fabrication, the SOI film thickness can be rounded off to the closest manufacture nominal one. For example, when $L = 70$ μm and $L/t = 6$, t_{best} is about 11.67 μm. For the convenience of fabrication, $t = 10$ μm may be a good choice.

For PSOI at $BV_{max,Lw}$ with various t, Fig. 9 plots the dependences of the on-resistance on L_w ($V_{GS} = 5$ V), whereas Fig. 10 depicts $N_{dr,Lw}$ versus L_w. For all the cases of $t = 10$ μm, when L_w increases, R_{on} increases as shown in Fig. 9, mainly due to the reducing $N_{dr,Lw}$ as shown in Fig. 10. For all the cases of $t > 10$ μm, when L_w increases, R_{on} still evidently increases as shown in Fig. 9, while $N_{dr,Lw}$

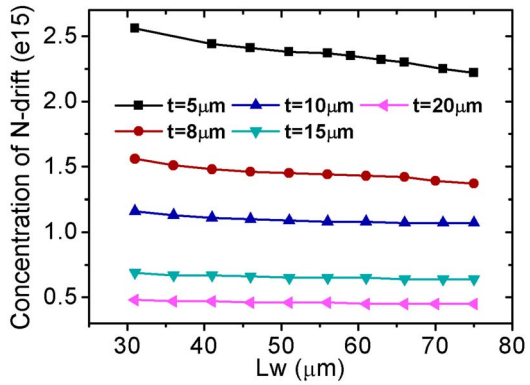

FIGURE 10. $N_{dr,Lw}$ versus L_w for PSOI at $BV_{max,Lw}$ with various t.

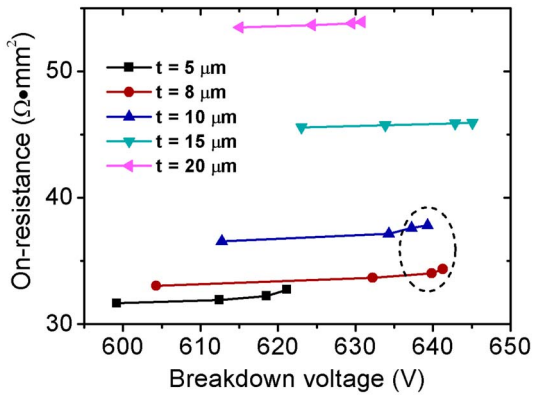

FIGURE 11. Trade-off between $BV_{max,Lw}$ and On-resistance for the PSOI LDMOS with various t. ($L = 90$ μm).

almost keeps unchanged as shown in Fig. 10. This implies that a larger L_w may degrade the drain current since a larger L_w leads a larger leakage current into the substrate and thus reduces the drain current.

The reason on why $N_{dr,Lw}$ almost keeps unchanged as L_w increases for the cases of $t > 10$ μm can be explained as follows. As illustrated in Fig. 5, when t increases, N_{dr} decreases for PSOI LDMOS with a fixed L according to the REUSRF theory, which is also clearly shown in Fig. 10. When t is large (e.g., $t > 10$ μm), $N_{dr,Lw}$ is small (e.g., $\sim 10^{14}\text{cm}^{-3}$). As L_w increases, a small variation in $N_{dr,Lw}$ (e.g., $\delta N_{dr,Lw} = 10^{13} \sim 10^{14}\text{cm}^{-3}$) can be large enough, in relative to $N_{dr,Lw}$, to significantly impact the RESURF effect and thus a slight adjustment in $N_{dr,Lw}$ can be sufficient for maintaining the RESURF to achieve fairly good BV. The minuscule change in $N_{dr,Lw}$ is hardly detectable, and thus $N_{dr,Lw}$ seems to be almost unchanged.

Fig. 11 depicts the trade-off between $BV_{max,Lw}$ and on-resistance for the PSOI LDMOS with various t under $L = 90$ μm. It can be found that, when t is between 8 and 10 μm, the PSOI LDMOS can achieve higher BV and smaller on-resistance. The PSOI LDMOS with $t = 15$μm can achieve the highest BV of all the cases, but figure of merit (i.e., FOM $= BV^2/R_{on}$) degrades significantly. Thus, $t = 15$ μm cannot be considered as a good choice for the design of device with $L = 90$ μm. In general, in order to achieve the best performance, both L and t need to be taken into consideration in a combinational way.

IV. CONCLUSION

PSOI LDMOS transistor has been comprehensively studied with various dimension settings (i.e., L and t). Firstly, it was found that, for a fixed L, BV_{max} changes as t increases. Generally, too thick or too thin SOI film is not the optimal choice. Thus, for achieving the highest BV, a combinational pair of L and t should be considered carefully. Furthermore, it has been shown that, when L is fixed, $L_{w,op}$ does not monotonously vary along with t. When the highest BV is achieved with a certain t (i.e., t_{best}), the corresponding $L_{w,op}$ is usually the largest one among all $L_{w,op}$ for PSOI LDMOS with different t. Secondly, it was shown that the ratio $L/t = 6$ is the optimal value for attaining higher BV of PSOI LDMOS. Considering the restrictions of the practical device fabrication processes, the ratio L/t between 5 and 7 may be acceptable for facilitating the device design margin. Finally, the trade-off between $BV_{max,Lw}$ and on-resistance was studied for the PSOI LDMOS with various t. It was shown that, when $L = 90$ μm, PSOI LDMOS with t between 8 μm and 10 μm can achieve the optimal deice performance with the optimal figure of merit (i.e., FOM $= BV^2/R_{on}$).

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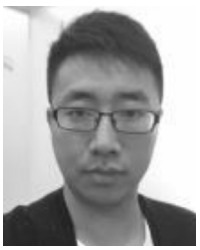

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