Received 2 December 2016; accepted 5 January 2017. Date of publication 9 January 2017; date of current version 22 February 2017.
The review of this paper was arranged by Editor M. K. Radhakrishnan.

Digital Object Identifier 10.1109/JEDS.2017.2649605

A Novel Sealing Redistribution Layer Approach for Through-Glass via Fabrication

SHIH-WEI LEE, GENG-MING CHANG, CHING-YUN CHANG, AND KUAN-NENG CHEN (Senior Member, IEEE)

Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan

CORRESPONDING AUTHOR: K.-N. CHEN (e-mail: knchen@mail.nctu.edu.tw)

This work was supported in part by the Ministry of Science and Technology under Grant MOST 103-2221-E-009-193-MY3 and Grant MOST103-2221-E-009-173-MY3, in part by the Ministry of Education, Taiwan, through the Aiming for the Top University Program, and in part by the National Chiao Tung University–University of California, Berkeley I-RiCE Program under Grant MOST 104-2911-I-009-301.

ABSTRACT A sealing redistribution layer (RDL) approach for the interposer fabrication is developed to simplify the conventional bottom-up process flow. By using this approach, bottom-up plating can achieve the integration of Cu-filler plating and its bottom RDL simultaneously. In this paper, through-glass via in glass interposer or 3-D integration is fabricated using the proposed approach. The electrical measurement and reliability tests indicate that the proposed approach can be an attractive candidate for interposer fabrication with great performance.

INDEX TERMS Through-Glass via (TGV), redistribution layer, glass interposer, 3D integration.

I. INTRODUCTION

With the miniaturization of IC, physics limitation and expensive extreme ultraviolet (EUV) lithography instrument induce the difficulty of Moore's law extension. 3D/2.5D integration that utilizes vertical electrical connection in stacked dies is considered as one of the most promising technologies to extend Moore's law [1]. Nowadays, it has been widely researched to promote the functional density of electronic system. Though-silicon via (TSV), which is a key technology in 3D/2.5D IC, can provide shorter interconnection length and shorter electrical delay. Furthermore, when compared with TSV, through-glass via (TGV) has attracted attention in recent years since glass substrate has a high resistivity, low insertion loss, and adjustable coefficient of thermal expansion. In addition, TGV has been proven to have better high frequency characteristic than TSV [2], [3].

The key technologies in TGV or TSV fabrication can be roughly divided into via formation, barrier and seed deposition, Cu electrochemical deposition (ECD), temporary bonding technology, and Cu chemical mechanical polishing (CMP). Among these technologies, ECD and CMP are regarded as the technologies with the highest cost in 3D integration [4]. They are used for the formation of Cu filler and removal of Cu overburden. In improving the cost efficiency, plating method plays an important role.

Intrinsically, top-down and bottom-up approaches can achieve the formation of Cu-filler plating in Cu-filler fabrication. By using blind via plating, top-down approach can complete the plating process without handling wafer and offer the flexibility of integration flow. However, many issues in the process cause the difficulty to obtain conformal plating without void formation, such as the ability of sputtering smooth Ti/Cu layer on the sidewalls, well-controlled plating chemistry, and the need of feature wetting [5]. On the other hand, the advantages of bottom-up approach can overcome these concerns and reduce the overburden on Cu during Cu plating [6]. In addition, this approach can be easily applied without expensive plating tool and electrolyte. However, temporary bonding or attaching technology is needed for bottom metal layer [7]. Although sealing bump with the bottom-up approach can provide a solution without the attachment of the metal layer requirement, the ability to control the size of the bottom metal is still a challenge [8]. In this letter, a novel sealing RDL method is proposed to improve the concerns mentioned here. To investigate the process feasibility, TGV is fabricated by using the proposed approach. With the well-fabricated TGV, electrical characteristic and reliability tests are investigated and discussed.

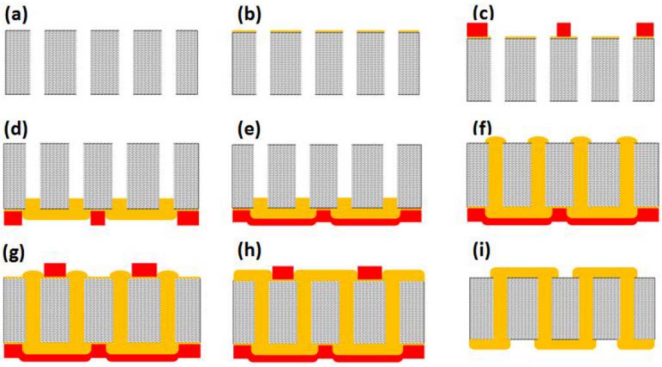

FIGURE 1. Process flow of proposed sealing RDL approach.

II. PROCESS AND FABRICATION RESULTS WITH ITS IMPROVEMENT

The process flow of glass interposer using sealing RDL shown in Fig. 1 includes:

1) Via of 50-μm diameter with 250-μm depth is formed byusing laser-drilling process.
2) Barrier/adhesion layer and Cu seed layer are sequentially sputtered on the top surface of glass.
3) Positive resist is coated on the substrate with glass via followed by lithography process to define the RDL pattern.
4) RDL sealing formation by electroplating.
5) Resist as protection layer is coated on the Cu to stop the growth of RDL during the next step of plating.
6) Bottom-up Cu TSV plating;
7) After completing the fabrication of TGV filler with bottom RDL, Ti and Cu are deposited on the other side followed by lithography process.
8) RDL Cu plating;
9) Removal of photo-resist and barrier/seed layer on both sides using wet etching to complete TGV with RDL.

In the proposed process, the RDL fabrication is similar to conventional RDL process, but process of TGV combined with RDL is quite different from other processes. For the conventional TSV/TGV fabrication, there are two approaches to complete the filler electro-plating: top-down and bottom-up. When using these two plating approaches, a thick Cu residual film on the top side (top-down approach) or on the bottom side (bottom-up approach) is formed since blanked Cu seed layer is grown together with Cu filler. To complete the RDL fabrication, this thick Cu film has to be removed with high cost of Cu CMP. In our proposed method, TGV and RDL are fabricated at the same time. Therefore, by using this proposed approach, the issue can be resolved.

After TGV with RDL fabrication is completed, scanning electron microscopy (SEM) is adopted to inspect the fabrication results of different plating currents. As shown in Fig. 2(a), the current of 15.8 A per TGV induces a fast growth of Cu seed layer, resulting in non-uniform plating. On the other hand, small current of 1.58 μA per TGV for plating can avoid the strong growth toward via. The

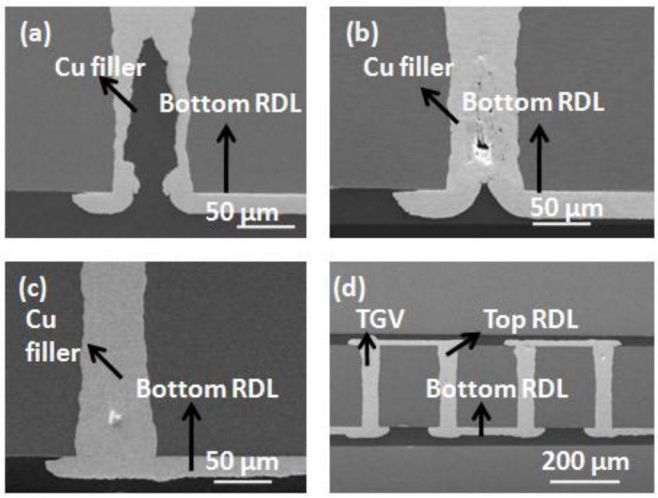

FIGURE 2. (a) Nonuniform plating of Cu filler by using a current of 15.8 μA per TGV; (b) nonuniform plating with a current of 1.58 μA per TGV; (c) uniform TGV and RDL plating with a current of 0.79 μA per TGV; (d) fabrication results of TGV chain.

results of Fig. 2(b) show that the depression structure is largely minimized. To explain the cause of the structure, [9] indicates that low plating rate can improve the uniformity of electroplating in TSV. Therefore, current for RDL sealing (step_e) of 0.79 μA can achieve filler plating without depression, as shown in Fig. 2(c). Fig. 2(d) shows the fabrication results of TGV chains without void and depression. In this study, TGV with uniform growth is used to investigate its characteristic.

The physical mechanism is explained in detail, as shown in the figure below. In Fig. 3(a), since the current is crowded at the corner, the current density at the corner is higher thus the growth rate of Cu at region A is higher than B. When high current (voltage) is applied for plating, most of Cu ions are deposited at region C instead of D in Fig. 3(b) due to shorter path between Cu block and bottom Cu layer. By using the IV-concept for simple explanation, assuming R in electrolyte is between Cu block and location C, while R+ΔR is between Cu block and location D. Then the current difference is $\frac{V}{R^2}\Delta R$, which is proportional to applied voltage (current), leading to large difference in growth rate at larger applied voltage (current). In Fig. 3(c), once the via is almost "sealed" by the bottom Cu, Cu ion is harder to reach region F due to a small opening and high Cu ion consumption at region E, leading to high growth rate of top side Cu. When Cu sealing is almost completed, the growth rate of bottom side Cu stops due to the lack of Cu ions, as shown in Fig. 3(d).

III. ELECTRICAL CHARACTERISTIC OF TGV

Fabrication of 50-μm diameter with 250-μm depth TGV on the bare glass substrate (dielectric constant = 5.27 (F/m)) by using sealing RDL method is performed with Kelvin, comb, and daisy chain structures. As shown in Fig. 4(a), a four-point Kelvin structure is adopted to investigate the characteristic of single TGV. Under current stressing, Fig. 4(b) represents

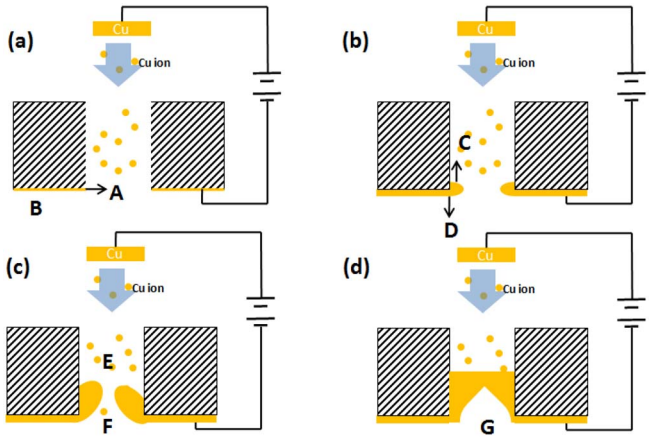

FIGURE 3. **(a) High Cu growth rate at the via corner; (b) high growth rate at C; (c) small opening; (d) bottom sealing.**

that the single TGV has a resistance of 3 mΩ, which almost matches the theoretical value [10]. On the other hand, the structure of daisy chain with multiple TSVs and metal lines is fabricated, as shown in Fig. 4(c). To inspect the quality of electrical connection, the measured result of different number of TGVs is plotted. Theoretically, the resistance of nTGVs chain can be roughly expressed in (1). Herein, n is the number of TGV chain, $\boldsymbol{R_{top\_RDL}/R_{bottom\_RDL}}$ is top/bottom metallization, $\boldsymbol{R_{contact}}$ is interface between RDL and TGV, and $\boldsymbol{R_{offset}}$ is the resistance caused by the contacts between the measured probe and the measured pad. The slope in n-R plot can be the combination of one TGV resistance, average resistance of RDL, and the interface resistance between RDL and TGV. Therefore, in this study, the linear slope of 6.9 mΩ can be obtained within 5% deviation, indicating great integration performance, as shown in Fig. 4(d).

$$R = n\left(R_{TGV} + \frac{R_{top\_RDL} + R_{bottom\_RDL}}{2} + R_{contact}\right) + R_{offset} \tag{1}$$

To inspect the insulating capability, comb structures with 120 TGVs of 200-μm pitch are designed to investigate leakage current and capacitance, as shown in Fig. 4(e). To decrease the impact of metal lines coupling, the adjacent RDLs are placed on the opposite of the glass substrate. By applying the voltages between 10 and -10 V, the leakage and capacitance can be obtained, as shown in Fig. 4(f). Similar to through-silicon via (TSV), the leakage characteristic $\boldsymbol{I_{leak}}$ of TGV is followed by Fowler-Nordheim tunneling, as described in (2) and (3) [11]. $\boldsymbol{I_{leak}}$ of TGV is strongly affected by electric field ξ, which is related to the voltage $\boldsymbol{V_{cross}}$ across the insulator, such as oxide and its thickness $\boldsymbol{d}$. Therefore, in the part of TSV, $\boldsymbol{I_{leak}}$ relies on the thickness and quality of thin oxide liner. However, TGV depends on via spacing due to insulated substrate, which greatly reduces the leakage when compared with TSV. As shown in Fig. 4(f), the leakage of 120 TGVs is less than nA, which is the typical leakage order of one TSV [12]. On the other hand, the capacitance behavior of TGV is also different from TSV.

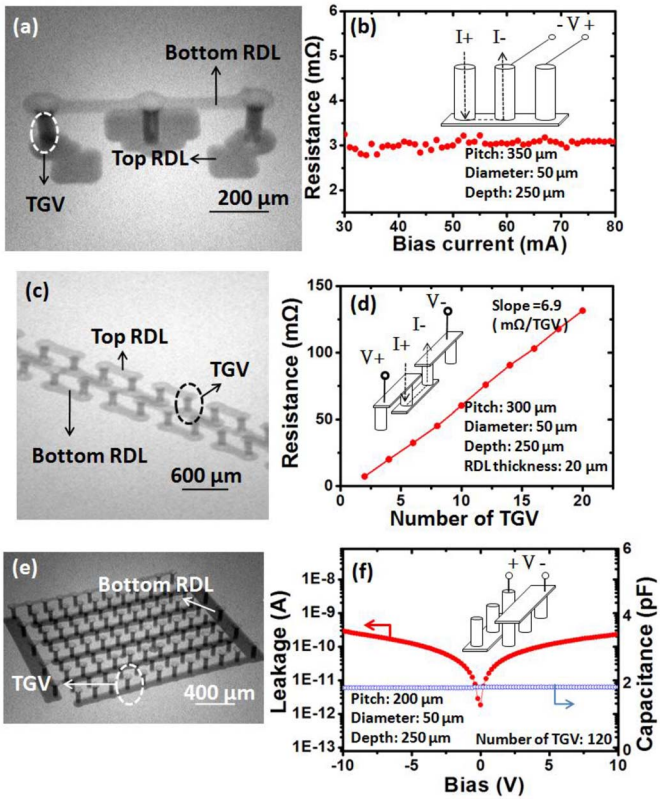

FIGURE 4. **(a) X-ray image of Kelvin TGV structure, and (b) its measurement results. (c) X-ray image of daisy chain structure, and (d) its measured resistance. (e) X-ray image of 120 TGV comb structure, and (f) its leakage and capacitance measurement.**

The capacitance of TSV is related to surface charge in silicon and changes with frequency and voltage. As shown in Fig. 4(f), the C-V curve of TGV behaves as a metal plate capacitance and has a stable 2 pF under voltage bias.

$$\boldsymbol{I}_{leak} \propto \xi^2 \exp\left(\frac{-C}{\xi}\right) \tag{2}$$

$$\xi = \frac{-V_{Cross}}{d}. \tag{3}$$

IV. QUALITY INVESTIGATION

Reliability tests including commonly used humidity test (HAST) and thermal cycle test (TCT) are performed to inspect the quality of this structure [13], [14]. JESD22-A104G and JEITA-ED-4701/100 method 103 are adopted for TCT and HAST, respectively. Electrical characterization results demonstrate excellent performance of TGV by using sealing RDL method. Fig. 5(a) shows the result of 130℃ and 85% humidity test for 48 h. The n-R graph shows daisy chain remains linear characteristic. There is only 0.12 mΩ/TGV increment in slope. It might come from the resistance change of the RDL after humidity test. On the other hand, the n-R graph has an improvement after TCT tests under conditions of -40∼125℃ for 500 loops, as shown in Fig. 5(b). The linearity of the graph increases with a reduction in its gradient. This improvement might come from metal grain

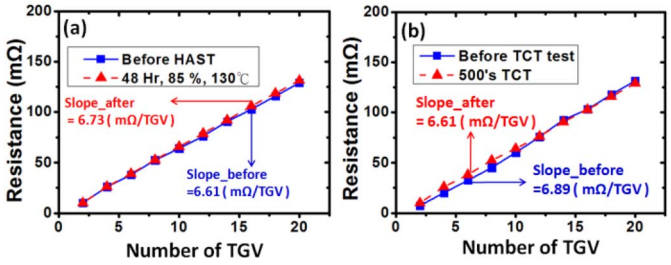

FIGURE 5. Electrical performances of TGV structures after (a) HAST test and (b) TCT test.

growth and metal diffusion at the interface between TGV and RDL. Overall, the satisfying results of the reliability tests imply that the structure has the ability to resist humidity and corrosion, as well as good temperature variation endurance, thus applicable on ready-to-market devices.

V. CONCLUSION

In this letter, a novel sealing RDL approach is proposed to achieve Cu bottom-up TGV plating process without temporary bonding. This approach can control the thickness of RDL and obtain the simultaneous fabrication of bottom RDL and filler deposition. TGV is fabricated and investigated by using this approach. Different structures are designed to investigate single TGV resistance, TGV chains resistance, leakage, and capacitance. In addition, TGV structures are inspected by HAST and TCT reliability tests. With great performances, this sealing RDL approach can provide a good solution for low-cost glass interposer or 3D integration without the usage of plating additives and a handling wafer.

REFERENCES

[1] A. W. Topol *et al.*, "Three-dimensional integrated circuits," *IBM J. Res. Develop.*, vol. 50, nos. 4–5, pp. 491–506, Jul. 2006, doi: 10.1147/rd.504.0491.

[2] J.-Y. Lee, S.-W. Lee, S.-K. Lee, and J.-H. Park, "Through-glass copper via using the glass reflow and seedless electroplating processes for wafer-level RF MEMS packaging," *J. Micromech. Microeng.*, vol. 23, no. 8, p. 085012, Aug. 2013, doi: 10.1109/TCPMT.2015.2511067.

[3] J. Kim *et al.*, "Electrical characteristics analysis and comparison between through silicon via (TSV) and through glass via (TGV)," in *Proc. Elect. Design Adv. Packag. Syst. Symp. (EDAPS)*, Seoul, South Korea, Dec. 2015, pp. 93–96, doi: 10.1109/EDAPS.2015.7383676.

[4] D. Velenis, M. Stucchi, E. J. Marinissen, B. Swinnen, and E. Beyne, "Impact of 3D design choices on manufacturing cost," in *Proc. IEEE Int. Conf. 3D Syst. Integr.*, Sep. 2009, pp. 1–5, doi: 10.1109/3DIC.2009.5306575.

[5] B. Wu, A. Kumar, and S. Ramaswami, *3D IC Stacking Technology*. New York, NY, USA: McGraw-Hill, 2011.

[6] E. Delbos, L. Omnès, and A. Etcheberry, "Bottom-up filling optimization for efficient TSV metallization," *Microelectron. Eng.*, vol. 87, no. 3, pp. 514–516, Mar. 2010, doi: 10.1016/j.mee.2009.06.008.

[7] H. H. Chang *et al.*, "TSV process using bottom-up Cu electroplating and its reliability test," in *Proc. 2nd Electron. Syst. Integr. Technol. Conf.*, Sep. 2008, pp. 645–650, doi: 10.1109/ESTC.2008.4684427.

[8] C.-H. Chiang *et al.*, "Sealing bump with bottom-up Cu TSV plating fabrication in 3-D integration scheme," *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 671–673, May 2013, doi: 10.1109/LED.2013.2250249.

[9] J. W. Choi *et al.*, "TSV Cu filling failure modes and mechanisms causing the failures," *IEEE Trans. Compon. Packag. Technol.*, vol. 4, no. 4, pp. 581–587, Apr. 2014, doi: 10.1109/TCPMT.2014.2298031.

[10] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1873–1881, Sep. 2009, doi: 10.1109/TED.2009.2026200.

[11] M. Lenzlinger and E. H. Snow, "Fowler–Nordheim tunneling into thermally grown SiO2," *J. Appl. Phys.*, vol. 40, no. 1, pp. 278–283, 1969, doi: 10.1063/1.1657043.

[12] T. Nakamura *et al.*, "Comparative study of side-wall roughness effects on leakage currents in through-silicon via interconnects," in *Proc. IEEE Int. 3D Syst. Integr. Conf.*, Jan./Feb. 2011, pp. 1–4, doi: 10.1109/3DIC.2012.6262948.

[13] S. W. Yoon, J. H. Ku, N. Suthiwongsunthorn, P. C. Marimuthu, and F. Carson, "Fabrication and packaging of microbump interconnections for 3D TSV," in *Proc. IEEE Int. Conf. 3D Syst. Integr.*, 2009, pp. 1–5, doi: 10.1109/3DIC.2009.5306554.

[14] A. Kamto, Y. Liu, L. Schaper, and S. L. Burkett, "Reliability study of through-silicon via (TSV) copper filled interconnects," *Thin Solid Films*, vol. 518, no. 5, pp. 1614–1619, Dec. 2009, doi: 10.1016/j.tsf.2009.07.151.

SHIH-WEI LEE received the B.S. degree in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan. He is currently pursuing the Ph.D. degree with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan. The focus of his research studies includes through silicon via, bump-less integration, heterogeneous integration, and 3-D IC technologies.

GENG-MING CHANG received the M.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2016.

CHING-YUN CHANG received the M.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2016.

KUAN-NENG CHEN (M'05–SM'11) received the M.S. degree in materials science and engineering and the Ph.D. degree in electrical engineering and computer science from the Massachusetts Institute of Technology. He was a Research Staff Member with the IBM Thomas J. Watson Research Center. He is currently a Professor of the Department of Electronics Engineering, National Chiao Tung University.

He was a recipient of the NCTU Distinguished Faculty Award four times, the NCTU Outstanding Industry-Academia Cooperation Achievement Award three times, the CIEE Outstanding Professor Award, the Adventech Young Professor Award, and the EDMA Outstanding Service Award. He also holds five IBM Invention Plateau Invention Achievement Awards.

Dr. Chen has authored over 250 publications and holds 77 patents. He has given over 70 invited talks in industries, research institutes, and universities worldwide. He is currently the Committee Member of the IEEE 3DIC, IEEE SSDM, IEEE VLSI-TSA, IMAPS 3-D Packaging, and DPS. He is a member of Phi Tau Phi Scholastic Honor Society. His current research interests are three-dimensional integrated circuits, through-silicon via technology, wafer bonding technology, and heterogeneous integration.