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Investigation of Dynamic Threshold Voltage Behavior in Semi-Floating Gate Transistor for Normally-Off AlGaN/GaN HEMT

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ABSTRACT In this paper, an inverter composed of semi-floating gate (SFG) transistor and a load resistor was analyzed. Varying threshold voltage (V_{th}) during switching was observed. This dynamic V_{th} behavior of SFG device is because of the special device structure of SFG transistors. Based on the V_{th}-programmable behavior of the SFG transistor, a SFG-based GaN high electron mobility transistor was proposed and enhancement-mode was realized with writing-0 into the transistor during every switching operation by simulation.

INDEX TERMS Semi-floating gate, dynamic threshold voltage, enhancement-mode GaN HEMT.

I. INTRODUCTION

Semi-floating gate (SFG) is a device concept utilizing a quasi-floating gate inside a transistor [1]. As the quasi-floating gate is charged or discharged, the threshold voltage (V_{th}) is changed. The SFG region can be coupled to the drain or source electrode via diode, tunneling field-effect transistor, or resistor. As a result, SFG transistor can be applied in different applications such as memory and sensor [1]–[6]. In this paper, the switching operation of an inverter consisting of a SFG transistor is analyzed and dynamic V_{th} is observed. Moreover, the threshold voltage of the SFG transistor can be programmed by writing-0 operation. Based on this device behavior, enhancement-mode GaN high electron mobility transistor (HEMT) utilizing SFG concept is proposed and studied by simulation.

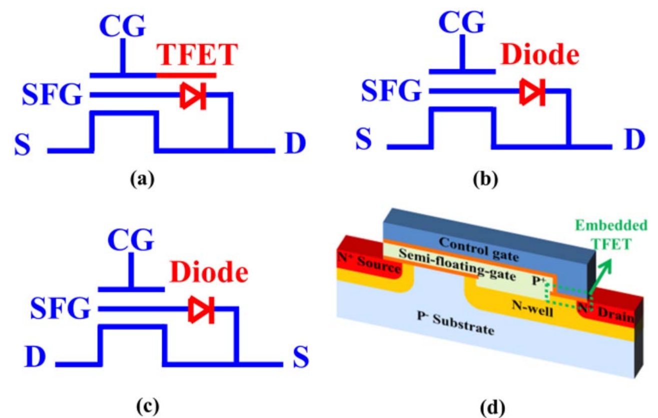

FIGURE 1. **Equivalent circuits of SFG devices with: (a) an integrated TFET, (b) a diode coupled to drain, and (c) a diode coupled to source. (d) Schematic view of the SFG transistor with an embedded TFET.**

II. DEVICE CONCEPTS AND DEVICE STRUCTURES

Fig. 1 shows the equivalent circuits of the SFG device concept. When a tunneling field effect transistor (TFET) is integrated with a floating gate, a SFG memory cell can be obtained [1]–[3]. The threshold voltage of SFG memory cell shown in Fig. 1(a) is controlled by the current through the TFET. If a diode is integrated between the drain electrode and the SFG region as shown in Fig. 1(b), this SFG device can work as a sensor [4]. For example, a simplified dosimeter structure has been proposed based on this device structure [5]. Light sensor can be formed when the integrated diode is optimized toward the photo-diode [4]. In Fig. 1(c), the cathode of the integrated diode is coupled to the source electrode. This configuration is suitable for

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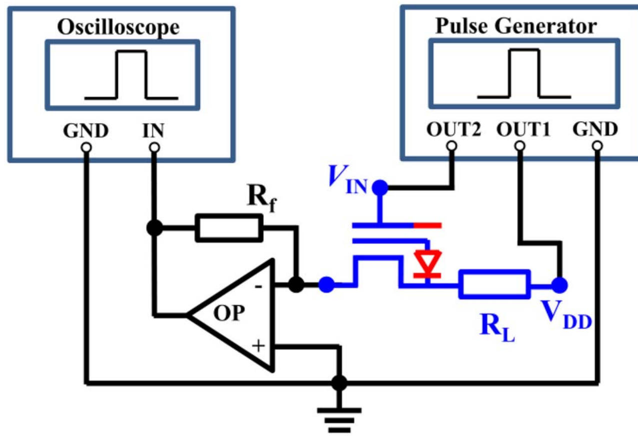

FIGURE 2. The diagram of the method of the SFG transistor measurement.

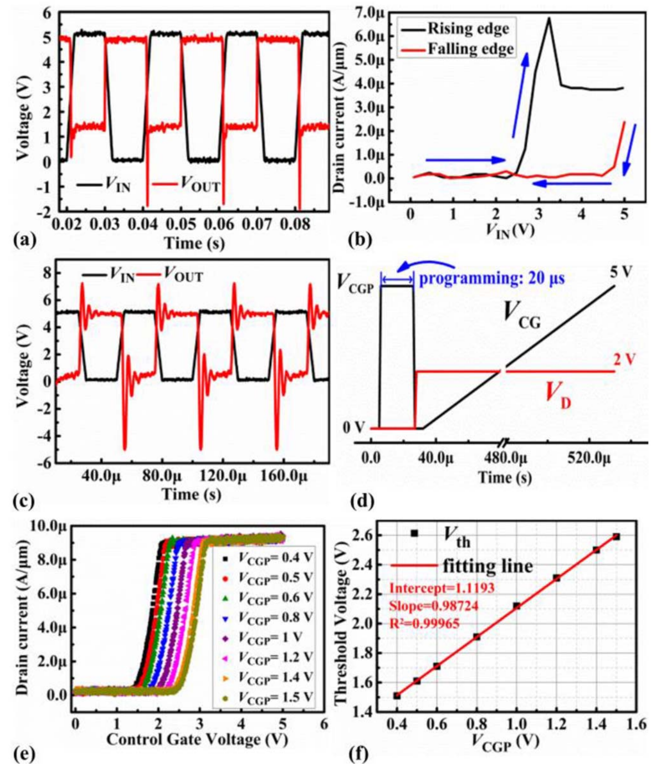

FIGURE 3. (a) Input and output voltage waveforms of the 20-ms period of the switching circuit. (b) Curves of drain current versus input voltage during the rising edge and falling edge of the switching operation. (c) Input and output voltage waveforms of the 50-us period of the switching circuit. (d) The operating sequence of a SFG transistor to program and measure the threshold voltage. (e) Measured transfer characteristics of the Si-based SFG transistor with different V_{CGP}. (f) Dependence of the threshold voltage extracted from Fig. 3(e) on V_{CGP}.

realizing enhancement-mode GaN HEMT. In this case, the threshold voltage of the device is increased if logic "0" is stored in the transistor. Then, a positive control-gate voltage is needed to turn on the channel of GaN HEMT. In this work, switching properties of the SFG transistor based on dynamic V_{th} and enhancement-mode SFG GaN HEMT are investigated.

III. EXPERIMENTAL, SIMULATION AND DISCUSSIONS

A. ELECTRICAL BEHAVIORS OF SFG TRANSISTOR

In the experiments, the silicon-based SFG transistor with the integrated TFET is measured and its schematic view is shown in Fig. 1(d). The fabrication process flow was described in [2]. The SFG region is connected to drain terminal via the embedded TFET. An inverter circuit is configured to investigate the switching behavior of SFG transistor. As shown in Fig. 2, the drain terminal of the SFG transistor is connected with a load resistor while the source terminal is connected to the cathode of the operational amplifier. The anode of the operational amplifier is grounded so that the source terminal of the SFG transistor is also grounded because of the virtual short concept of the operational amplifier. The input signal (V_{in}) generated by the pulse generator is applied to the control gate electrode of the SFG transistor while the power supply voltage (V_{DD}) is set to 5 V. The output current of the SFG transistor is converted into the voltage by the resistor (R_f), which is monitored by the oscilloscope. After the output current is measured, the output voltage signal (V_{out}) at the drain terminal of the SFG transistor can be calculated out by the load resistor. The input pulse and output voltage waveform of 20-ms period are shown in Fig. 3(a). When the input voltage increases from 0 V to 5 V, the output voltage firstly decreases from 4.9 V to a lowest value and then increases from the lowest value to 1.3 V. When V_{in} decreases from 5 V to 0 V, V_{out} increases from 1.3 V to 4.9 V. During the rising edge and falling edge, curves of drain current of the SFG transistor versus input voltage are shown in Fig. 3(b). The SFG transistor during the rising edge is turned on earlier than the turn-off point at the falling edge. During the rising edge, the drain current of the SFG transistor firstly increases to a peak value and then is reduced to a stable value. During the turn-on period, V_{in} increases and the tunneling current of the TFET charges the SFG node. The SFG potential is gradually increased and V_{th} of the SFG transistor is decreased. When V_{in} continues to increase and V_{out} decreases to the lowest value, the forward-biased diode in the SFG transistor will discharge the SFG node so that the SFG potential is lowered and V_{th} of the SFG transistor is increased. Hence, the drain current is reduced and the output voltage is increased. This electrical behavior proves dynamic V_{th} of the SFG transistor during switching. The increased drain current caused by lowered V_{th} can lead to faster switching of the SFG transistor during the rising edge. In Fig. 3(c), the cycle time of switching waveform is reduced to 50 μs. Some oscillations are generated in the output voltage because of the measurement equipments and the output signal tends to be stable after oscillations. During the rising edge, the output voltage decreases from 5 V to about 0 V when the input voltage increases from 0 V to 5 V. In Fig. 3(c), the output voltage V_{out} (red-line) is slightly rising from 0 V when V_{in} is kept at 5 V. The SFG potential changes slowly because the switching frequency is increased

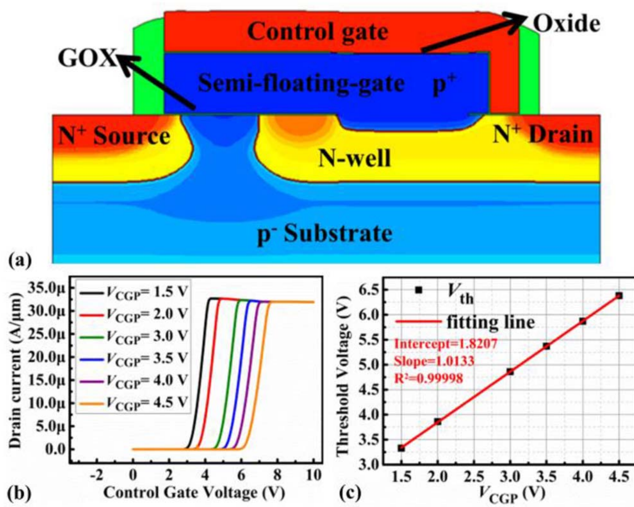

FIGURE 4. **(a) The simulated device structure of the SFG transistor. (b) Simulated transfer characteristics of the SFG transistor with different V_{CGP}. (c) Dependence of the threshold voltage extracted from Fig. 4(b) on V_{CGP}.**

and the cycle time is shorter than the retention time of the charge stored in the SFG region. In this case, dynamic V_{th} will acclerate the switching operation. Hence, the full-swing switching operation of the SFG transistor can be realized and accelerated.

Moreover, the threshold voltage of SFG transistor can be programmed utilizing writing-0 operation. The measurement method is the same as that shown in Fig. 2 but the load resistor is removed. The operating sequence in Fig. 3(d) is applied to the SFG transistor. In the first 32 μs, the control gate voltage (V_{CG}) is increased to a positive peak voltage (V_{CGP}) and drain voltage (V_D) is fixed to 0 V so that electron carriers flow into the SFG region and increase the threshold voltage of the device. The operating sequence of the last 500 μs in Fig. 3(d) is set to measure the transfer characteristics of SFG transistor with different V_{CGP}. The result is shown in Fig. 3(e) where V_{th} is extracted. The plot of V_{th} versus V_{CGP} in Fig. 3(f) shows that the change of V_{th} is almost equal to that of V_{CGP}. Hence, V_{th} of SFG transistor can be programmed by adjusting V_{CGP}. This V_{th}-programmable behavior of the SFG transistor can be verified by simulation. The simulated device structure of the SFG transistor is shown in Fig. 4(a). The p-type doping SFG region is connected to the drain terminal. The gate-oxide layer and the dielectric layer between SFG and the control gate are 6-nm-thick SiO_2 layers. The operating sequence applied to the simulated SFG transistor is similar to that shown in Fig. 3(d). In the first 27 μs, V_{th} of the device is programmed and the transfer characteristics with different V_{CGP} are simulated in the last 200 μs. The dependence of V_{th} on V_{CGP} in Fig. 4(c) is extracted from the transfer characteristics in Fig. 4(b). It also shows that V_{th} of the device can be programmed to increase linearly with V_{CGP}.

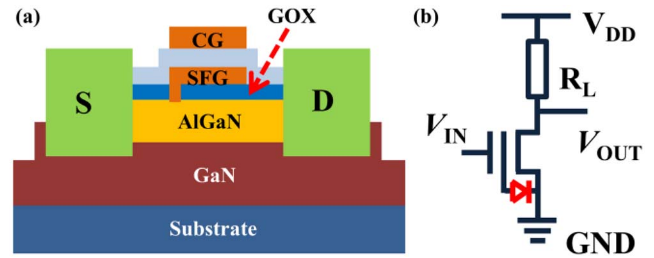

FIGURE 5. **(a) The simulated device structure of the enhancement-mode GaN HEMT based on the SFG concept. (b) The switching circuit diagram applying the SFG GaN HEMT.**

B. APPLICATION OF V_{TH}-PROGRAMMABLE BEHAVIOR IN GAN HEMT

AlGaN/GaN HEMT has been widely investigated for its promising power electronics applications but its normally-on behavior makes the circuit design complex. The normally-off AlGaN/GaN HEMT is strongly expected and many techniques have been reported such as gate recess [7]–[9], p-type gate [10]–[12] fluorine plasma ion implantation [13], [14], and floating-gate device structure [15], [16]. In this work, based on the V_{th}-programmable SFG transistor mentioned above, a SFG GaN HEMT device is proposed and simulated to realize enhancement-mode device by TCAD software. As shown in Fig. 5(a), the simulated enhancement-mode SFG GaN HEMT structure is composed of a GaN HEMT and a semi-floating gate. In the simulation, a 2-μm-thick GaN layer is stacked on the oxide substrate and a 25-nm-thick $Al_{0.25}Ga_{0.75}N$ layer is stacked on the GaN layer. A 2-dimensional electron gas (2DEG) is formed at the interface of AlGaN and GaN. The gate-oxide layer and the dielectric layer between SFG and the control gate are 10-nm-thick SiN layers. The SFG region and control gate are formed by gold. A Schottky diode is formed between metal SFG and AlGaN with a 100-nm-wide hole of the gate-oxide layer. The gate length is 1.1 μm. The gate-source and gate-drain distances are 1 and 5 μm, respectively. The equivalent circuit of the device is shown as Fig. 1(c) where the Schottky diode is put in between source electrode and SFG region.

At the initial stage, the SFG GaN HEMT is a normally-on device. However, its V_{th} can be programmed to be a positive value so that the device becomes enhancement-mode. As shown in Fig. 6(a), the first 3 μs is the programing stage. During the programming operation, V_{CG} is increased to V_{CGP} and V_D is dropped to 0 V. In Fig. 6(a), the period from 3 μs to 6 μs is added to investigate the transfer characteristics of the SFG GaN HEMT. V_{CG} decreases from V_{CGP} to 0 V while V_D is fixed to 10 V. The simulated transfer characteristics of the SFG GaN HEMT with different V_{CGP} are shown in Fig. 6(b). It can be seen that V_{th} of the SFG GaN HEMT increases from a negative value to a positive value with the increasing V_{CGP}. Hence, enhancement-mode SFG GaN HEMT is realized. The SFG potential (V_{SFG}) of

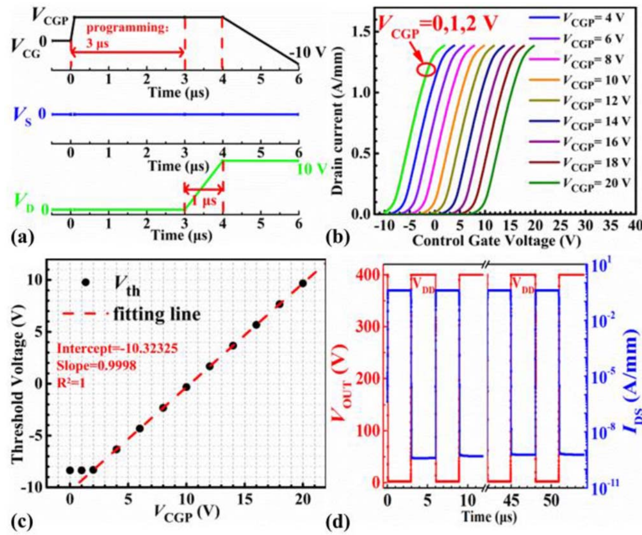

FIGURE 6. **(a) The simulated operating sequence of a SFG GaN HEMT to program and measure the threshold voltage. (b) The simulated transfer characteristics of the SFG GaN HEMT with different V_{CGP}. (c) Dependence of the threshold voltage of the device extracted from Fig. 6(b) on V_{CGP}. (d) The simulated output voltage and drain current of the SFG GaN HEMT during the switching operation.**

the device can be calculated by the following equation:

$$V_{SFG} = (V_{CG}C_{IPD} + Q)/C_{tot} \quad (1)$$

where C_{tot} is total SFG capacitance, C_{IPD} is capacitance between control gate electrode and SFG region, and Q is the accumulated electron charge in the SFG region. During the programing cycle, the SFG GaN HEMT is operated with writing-0. When V_{CGP} is large enough, the Schottky diode of the SFG-AlGaN junction is turned on so that electron carriers flow into the SFG region. Although larger V_{CGP} should lead to larger V_{SFG} according to (1), injected electron charge lowers V_{SFG} so that the Schottky diode is gradually turned off. Hence, the SFG potential of the device after writing-0 operation ($V_{SFG_0_W}$) is almost equal to the source voltage (V_S) of writing-0 plus the turn-on voltage of the Schottky diode (V_{on}), which is shown as follows:

$$V_{SFG_0_W} \approx V_S + V_{on} = V_{on} \quad (2)$$

where the source voltage is fixed to 0 V. Combing (1) and (2), we can deduce that the injected electron charge Q is equal to ($C_{tot}V_{on}$- $C_{IPD}V_{CGP}$) after the device is programmed. The relationship between V_{th} of the device and Q is

$$V_{th} = V_{th0} - Q/C_{IPD},$$
$$V_{th} = V_{th0} - C_{tot}V_{on}/C_{IPD} + V_{CGP} \quad (3)$$

where V_{th0} is initial threshold voltage of the device without accumulated electron charge in the SFG region. According to (3), V_{th} of the device increases linearly with V_{CGP} shown in Fig. 6(c) so that V_{th} can be programmed and the enhancement-mode SFG GaN HEMT can be realized.

The switching properties of the SFG GaN HEMT are further studied by simulation and the switching circuit is shown in Fig. 5(b). The drain terminal of the device is connected with a load resistor. The power supply voltage V_{DD} is set to 400 V. The control gate voltage of the SFG GaN HEMT is applied with the input voltage pulse which varies between 0 V and 20 V. During the rising edge of the input voltage, the SFG potential increases with increasing control gate voltage according to (1). When the input voltage is large enough, the Schottky diode is turned on so that electrons flow into the SFG region and V_{th} of the SFG GaN HEMT is increased with increasing input voltage. According to (3), V_{th} of the device can reach the maximum value with maximum V_{in}. Hence, V_{th} of the device can be programmed to be a positive value by adjusting maximum V_{in}. When input voltage is decreased to 0 V in the falling period, the positive-V_{th} SFG GaN HEMT is turned off so that the switching operation is realized. The Schottky diode will be reverse biased because of the accumulated electrons in the SFG region according to (1) when the input voltage is small enough in the falling period. The reverse current of the diode charges the SFG region and V_{th} of the SFG GaN HEMT decreases very slowly. Moreover, V_{th} of the SFG GaN HEMT can be refreshed during the rising edge in every switching pulse so that the positive V_{th} can be maintained during the whole switching period. It is shown in Fig. 6(d) that the output voltage of the switching circuit changes between 0 V and 400 V and the full-swing switching behavior is realized. That means the SFG GaN HEMT has been programmed to be enhancement-mode.

IV. CONCLUSION

In this paper, the dynamic threshold voltage of the SFG concept is investigated in an inverter circuit. The mechanism of dynamic V_{th} behavior in SFG transistor is studied. Based on the dynamic V_{th} behavior, the threshold voltage of SFG transistor can be programmed and then an enhancement-mode SFG GaN HEMT is proposed by writing-0 into the SFG region during every switching cycle. Its switching behavior in a switching circuit using 400-V supply voltage is also proven by simulation.

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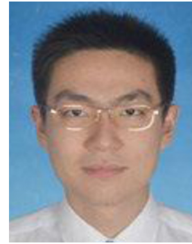

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