Received 20 September 2016; revised 27 November 2016 and 16 December 2016; accepted 21 December 2016. Date of publication 23 December 2016; date of current version 22 February 2017. The review of this paper was arranged by Editor M. Chan.

Digital Object Identifier 10.1109/JEDS.2016.2644724

Reliability-Tolerant Design for Ultra-Thin-Body GeOI 6T SRAM Cell and Sense Amplifier

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This work was supported by the Ministry of Science and Technology, Taiwan, under Contract MOST 104-2221-E-008-124 and Contract MOST 105-2628-E-008-006-MY3.

ABSTRACT This paper investigates the reliability-tolerant design for ultra-thin-body (UTB) GeOI 6T SRAM cell and sense amplifiers. For UTB GeOI 6T SRAM cells, using high threshold voltage design significantly mitigates the read and hold static noise margin degradations due to NBTI and PBTI. Due to worse PBTI degradations, as stress (aging) time increases, GeOI current and voltage latch sense amplifiers show larger degradation in word-line to sense amplifier enable (SAE) delay (T_{WS}) and sense amplifier sensing delay (T_{SA}) compared with the SOI counterparts. Using WL to SAE self-timed sensing scheme mitigates the BTI induced delay degradation. A new reliability-tolerant sense amplifier with speed-up design is proposed for the first time to improve the PBTI dominated sensing delay for UTB GeOI sense amplifier.

INDEX TERMS Reliability-tolerant, ultra-thin-body (UTB), GeOI, NBTI, PBTI, SRAM, sense amplifier.

I. INTRODUCTION

Germanium (Ge) has been proposed as an alternative channel material to enhance mobility and current drive [1], [2]. However, Germanium-channel device with high permittivity and low band-gap suffers from short-channel effects (SCEs) and severe band-to-band tunneling leakage current. Ultra-thin-body (UTB) Germanium-on-Insulator (GeOI) MOSFET has been proposed as a promising device architecture [3], [4] due to its better control of SCEs.

Negative and positive bias temperature Instabilities (NBTI for PFET, and PBTI for NFET) have become major reliability concerns as they weaken MOSFETs over time [5], resulting in temporal degradations in the stability and performance of the SRAM cells [6], [7]. Several studies [8], [9] have investigated the BTI reliability in Ge MOSFETs. The Si-passivated Ge devices with HfO_2/SiO_2 gate stack show less NBTI degradation than the Si counterparts because there is less hole trapping in the dielectric of the Ge device due to its larger valence band offset. The PBTI degradation of the Ge devices is more severe than the Si counterparts. This may attribute to the lower processing temperature during device fabrication, which results in larger amount of electron traps in the dielectric for the high-k Ge MOSFETs. Therefore, for UTB GeOI SRAM cells, PBTI dominates the degradations in read static noise margin (RSNM), hold static noise margin (HSNM), cell read access time, and time-to-write, while for UTB SOI SRAM cells, NBTI dominates the degradations in RSNM, HSNM, and time-to-write [10], [11]. In this paper, we focus on the reliability-tolerant design for mitigating the stability and delay degradations due to NBTI and PBTI in UTB GeOI SRAM cell and sense amplifier. This paper is organized as follows. Section II describes TCAD simulation methodology. Section III compares the stability and performance degradations due to NBTI and PBTI for GeOI and SOI SRAM cells. Threshold voltage (Vth) design and word-line underdrive (WLUD) read-assist circuit techniques are analyzed and compared to mitigate/compensate the SRAM stability degradation due to NBTI/PBTI. Section IV compares the delay degradations for the current latch sense amplifier (CLSA) and voltage latch sense amplifier (VLSA) for UTB GeOI and SOI MOSFETs. Two sense amplifier enable (SAE) timing control circuits using inverter buffers and self-timed sensing scheme are analyzed and compared under BTI stress. A new reliability-tolerant sense amplifier with speed-up design is also proposed to mitigate the delay degradation for UTB GeOI sense amplifier. Section V concludes the paper.

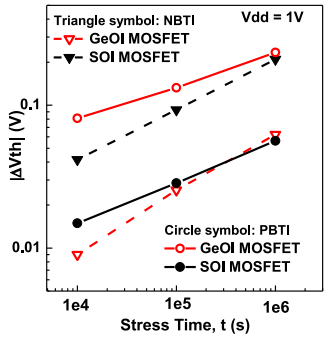

FIGURE 1. NBTI and PBTI induced Vth shift for UTB GeOI and SOI MOSFETs. UTB GeOI MOSFETs show larger PBTI and smaller NBTI degradations than the SOI MOSFETs.

II. DEVICE DESIGN AND TCAD SIMULATION METHODOLOGY

The UTB GeOI and SOI MOSFETs designed with 25nm gate length are used in this study [10]. Ge MOSFET with smaller bandgap exhibits larger band-to-band tunneling. In the TCAD simulations, the band-to-band tunneling and mobility model are calibrated with experimental data [3], [4] to accurately assess the power-performance of UTB GeOI and SOI devices. Reaction-diffusion (R-D) model [12] is used to calibrate the experimental data [8] of Vth drift due to NBTI/PBTI in Ge MOSFETs [10]. Based on the calibrated R-D model, Fig. 1 shows the time-dependent threshold voltage increase (|ΔVth|) due to NBTI and PBTI for UTB GeOI and SOI MOSFETs. As can be seen, UTB GeOI MOSFETs show larger PBTI and smaller NBTI degradations than the UTB SOI MOSFETs. The UTB GeOI and SOI MOSFETs are designed to have the same regular Vth (= 0.2V, RVt), and the 6T SRAM cells and sense amplifiers are analyzed using TCAD mixed-mode simulations [12].

III. ULTRA-THIN-BODY GEOI SRAM CELLS

A. IMPACTS OF NBTI/PBTI ON UTB GEOI SRAM CELL

The degradation in SRAM stability with time under worst case static stress pattern/condition (extreme asymmetry condition, only PR with NBTI and NL with PBTI) is considered as shown in Fig. 2. For worst-case aging, the SRAM cell stores the same data for a long period of time. The read static noise margin (RSNM) depends on the ability of the pull-down device (NL) to maintain the node VL storing '0' below the trip point of the opposite inverter (PR-NR). Under the worst case scenario for read stability, the threshold voltages of NL and PR are increased due to PBTI and NBTI, which increases the read disturb voltage on the VL node, and reduces the trip voltage of the PR-NR inverter, making it easier for the cell to flip during read operation, thus reducing the RSNM.

Fig. 3(a) shows the RSNM degradations due to NBTI and PBTI for GeOI and SOI SRAM cells. NBTI weakens

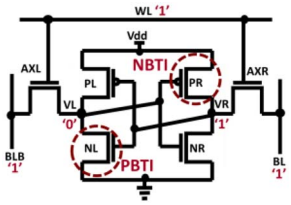

FIGURE 2. Worst stress scenario for SRAM. Only PR and NL suffer from NBTI and PBTI, respectively.

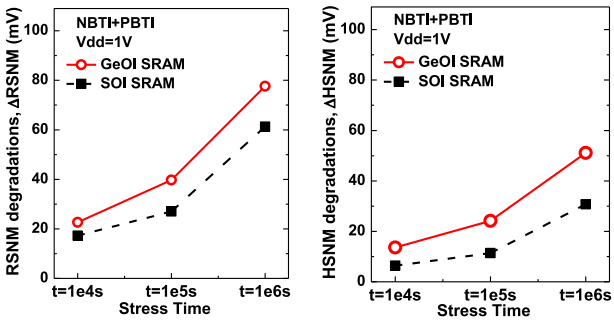

FIGURE 3. (a) RSNM degradations due to BTI stress for GeOI and SOI SRAM cells. (b) HSNM degradations due to BTI stress for GeOI and SOI SRAM cells.

the pull-up device (PR), thus reducing the trip voltage and RSNM. The weakening of pull-down device (NL) due to PBTI results in the increase of read disturb voltage and reduces RSNM. For UTB GeOI MOSFETs, PBTI degradation is more severe than NBTI degradation. PBTI dominates the RSNM degradation compared with the NBTI for the UTB GeOI SRAM cells. Besides, RSNM is more sensitive to the Vth increase due to PBTI compared with NBTI [6]. For SOI SRAM cells, NBTI dominates the RSNM degradation compared with PBTI. GeOI SRAM cell considering both NBTI and PBTI shows larger RSNM degradations than the SOI counterpart as shown in Fig. 3(a). In contrast with the significant RSNM degradation due to NBTI/PBTI, WSNM only degrades slightly due to BTI stress [10]. Fig. 3(b) shows the HSNM degradations due to NBTI and PBTI for GeOI and SOI SRAM cells. PBTI dominates the HSNM degradations for UTB GeOI SRAM cell, while NBTI dominates the HSNM degradations for UTB SOI SRAM cell. UTB GeOI SRAM cell considering both NBTI and PBTI shows larger HSNM degradations (Δ HSNM) than the UTB SOI counterpart. BTI stress is more critical for RSNM than HSNM, and NBTI and PBTI stress introduce more RSNM degradations than HSNM degradations.

Fig. 4 shows the cell read-access time and time-to-write degradations due to BTI for UTB GeOI and SOI SRAM cells. Cell read-access time and time-to-write are analyzed for 64 cells per bit-line. A capacitive load is added onto each bit-line to account for the capacitance of wires and the connected devices. Pull-down device with PBTI degrades the

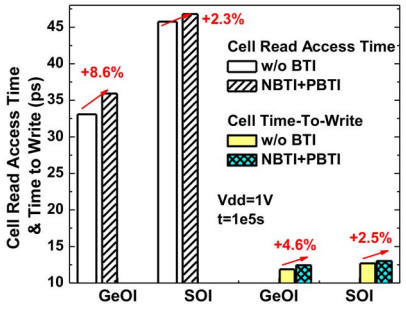

FIGURE 4. Cell read-access time and time-to-write comparisons for UTB GeOI and SOI SRAM cells under BTI stress.

read current and cell read-access time, and PBTI has dominant effect on cell read-access time. UTB GeOI SRAM cells with worse PBTI degradation show larger cell read-access time degradation (8.6%) than the UTB SOI SRAM cells (2.3%). Cell time-to-write is defined as the time from the 50% activation of the WL to the time when the voltages of two cell storage nodes cross each other. Pull-down device (NL) with PBTI and pull-up (PR) device with NBTI degrade the cell time-to-write. UTB GeOI SRAM cells show larger time-to-write degradation (4.6%) due to NBTI/PBTI than the UTB SOI SRAM cells (2.5%).

B. RELIABILITY-TOLERANT DESIGN FOR UTB GEOI SRAM CELL

Due to worse PBTI degradation in UTB GeOI MOSFETs, the UTB GeOI SRAM cells show larger RSNM and HSNM degradations compared to UTB SOI SRAM cells. In this section, high Vth design and read-assist circuit (word-line under-drive, WLUD [13]) techniques are analyzed and compared for UTB GeOI SRAM cells to mitigate/compensate the RSNM degradation due to NBTI/PBTI. Fig. 5 shows the RSNM, WSNM, HSNM, cell read-access time, and cell time-to-write comparisons among nominal SOI and GeOI with regular Vth ($|Vth| = 0.2V$, RVt), high Vth GeOI ($|Vth| = 0.4V$, HVt), and GeOI SRAM cells with WLUD (RVt_WLUD) considering both NBTI and PBTI. Vth shift ($|\Delta Vth|$) due to BTI is proportional to $[(Vdd - Vth) \times t^n]$ [14]. At Vdd = 1V, UTB GeOI MOSFET with HVt design shows smaller NBTI/PBTI degradation ($|\Delta Vth| = 13mV/106mV$) than the UTB GeOI MOSFET with RVt design ($|\Delta Vth| = 29mV/132mV$). Compared with the RVt UTB GeOI SRAM cell, UTB GeOI SRAM cell with HVt design shows significant improvement in RSNM (152%) and HSNM (27%) due to less BTI degradation and higher Vth design. At Vdd = 1V, SRAM cell with high Vth design increases the RSNM compared with the lower Vth design [15]. UTB GeOI SRAM cells with WLUD shows 65% improvement in RSNM, while exhibiting 17% degradation in WSNM. UTB GeOI SRAM cells with HVt design show larger degradation in cell read-access time and time-to-write compared with the UTB GeOI SRAM cells with WLUD, while the HVt UTB GeOI SRAM cell still shows

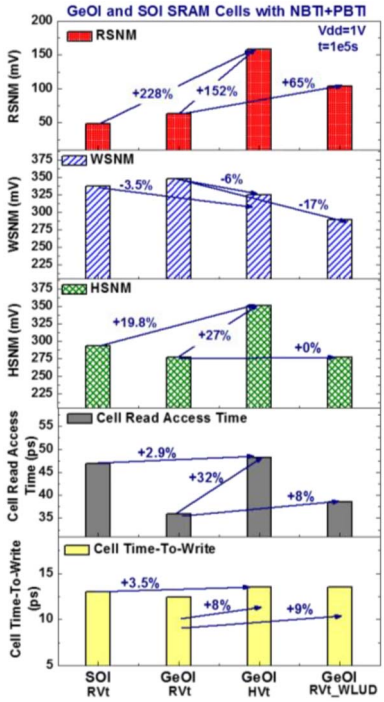

FIGURE 5. RSNM, WSNM, HSNM, cell read-access time, and cell time-to-write comparisons among nominal SOI and GeOI ($|Vth| = 0.2V$, RVt), high Vth GeOI ($|Vth| = 0.4V$, HVt), and GeOI ($|Vth| = 0.2V$, RVt_WLUD) with read-assist WLUD SRAM cells considering NBTI and PBTI.

comparable cell read-access time and time-to-write compared to the UTB SOI SRAM cells.

IV. ULTRA-THIN-BODY GEOI SENSE AMPLIFIERS

A. RELIABILITY-TOLERANT SELF-TIMED SENSING SCHEME

Two types of sense amplifiers including current latch sense amplifier (CLSA) and voltage latch sense amplifier (VLSA) are analyzed as shown in Fig. 6(a) and 6(b). Both CLSA and VLSA have the inputs connected to BL and BLB. The sense amplifier is enabled once the required differential voltage (ΔV_{BL}) is developed on the bit-lines. Fig. 6(c) shows the timing scheme of world-line (WL) to sense amplifier enable (SAE) delay (T_{WS}) and sense amplifier sensing delay (T_{SA}). WL to SAE delay (T_{WS}) is defined as the time between the activation of WL (0.5Vdd) and SAE enable (0.5Vdd). In this work, two types of timing control circuits for SAE are analyzed and compared as shown in Fig. 6(d). One is inverter timing buffers, and the other one is self-timed sensing scheme [16]. For inverter buffers at t = 0s (without BTI stress), T_{WS_INV} determined by the inverter chains corresponds to the time for bit-line differential voltage to reach 200mV (20% of Vdd). For the self-timed sensing scheme, when sufficient voltage (more than sense amplifier offset) is developed across BL and BLB, SAE goes high via a skewed NAND gate. The NAND gate is designed to be triggered with trip voltage close to Vdd.

Fig. 7(a) and 7(b) show the WL to SAE inverter buffer delay (T_{WS_INV}) and self-timed sensing delay (T_{WS_NAND}) for GeOI and SOI MOSFETs respectively. As can be seen,

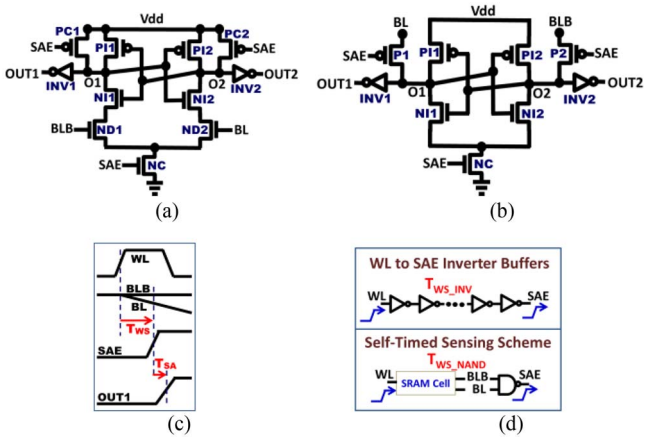

FIGURE 6. **(a) Current latch sense amplifier (CLSA), (b) Voltage latch sense amplifier (VLSA), (c) Timing scheme of word-line (WL) to sense amplifier enable (SAE) delay (T_{WS}) and sense amplifier sensing delay (T_{SA}). (d) Two types of timing control circuits SAE are analyzed and compared including inverter buffers and self-timed sensing scheme.**

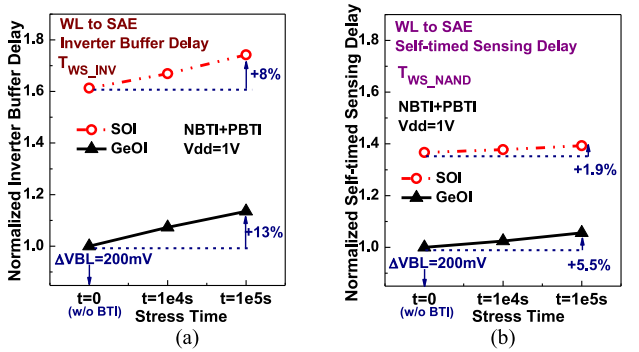

FIGURE 7. **(a) WL to SAE inverter buffer delay (T_{WS_INV}) and (b) WL to SAE self-timed sensing delay (T_{WS_NAND}) for GeOI and SOI MOSFETs.**

GeOI shows both smaller T_{WS_INV} and T_{WS_NAND} than the SOI due to its higher drive current. For WL to SAE inverter buffers, both NFETs and PFETs suffer from BTI stress, and the duty cycle is 0.5. Duty cycle is defined as the percentage of a period that devices are under stress (|Vgs|= Vdd) [17]. As stress (aging) time increases to 1e5s, GeOI shows 13% degradation in T_{WS_INV}, which is larger than the SOI counterpart because GeOI suffer from larger PBTI stress. WL to SAE self-timed sensing delay (T_{WS_NAND}) is determined by the combinations of cell read-access time and NAND delay. With BTI stress, the cell read-access time degrades due to the weaken pull-down devices, while the NAND delay is improved because the weaken bottom NFET of NAND suffering from BTI results in faster low to high signal in SAE. Besides, the WL to SAE self-timed sensing scheme exhibits less BTI degradations than the inverter timing buffers as shown in Fig. 7(b).

B. RELIABILITY-TOLERANT SENSE AMPLIFIER DESIGN

The sense amplifier sensing delay (T_{SA}) is defined as the difference between the time SAE is turned on (0.5Vdd) to the time OUT1 of CLSA and VLSA reaches 0.5Vdd as shown

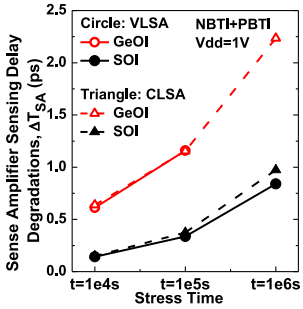

FIGURE 8. **Sense amplifier sensing delay (T_{SA}) degradations for GeOI and SOI sense amplifiers considering NBTI and PBTI. Sense amplifier is enabled when bit-line differential voltage (ΔV_{BL}) reaches 200mV.**

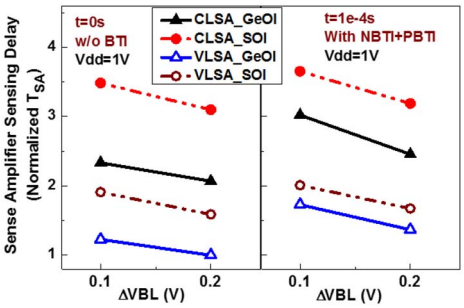

FIGURE 9. **Impact of bit-line differential voltage (ΔV_{BL}) on sense amplifier sensing delay (T_{SA}) for GeOI and SOI sense amplifiers considering NBTI and PBTI.**

in Fig. 6(c). The worst case stress scenario is considered for CLSA and VLSA, in other words, the sense amplifier is consistently reading the same data which induces the most threshold voltage shift due to BTI. For GeOI CLSA (VLSA), N1, ND1, and NC (NI1 and NC) suffer from larger PBTI, and thus exhibiting larger T_{SA} degradations as aging time increases (Fig. 8). Fig. 9 shows sense amplifier sensing delay (T_{SA}) influenced by bit-line differential voltage (ΔV_{BL}). The minimal bit-line differential voltage is a factor in defining the read-access time and the speed of SRAM. A larger bit-line differential is beneficial for more reliable sensing. As bit-line differential voltage (ΔV_{BL}) increases, T_{SA} decreases. At t = 0s (without BTI stress), GeOI CLSA and VLSA show smaller T_{SA} than the SOI counterparts. As t increases from 0s to 1e4s, both GeOI CLSA and VLSA exhibit larger T_{SA} degradations than the SOI ones, while the GeOI sense amplifiers still show smaller T_{SA} than the SOI ones. For more realistic analysis, recovery must be considered for sense amplifiers [17].

Fig. 10 shows the proposed variation-tolerant speed-up design for UTB GeOI VLSA. In Fig. 11(a), the operation waveform shows that the sense amplifier sensing delay degrades as aging time increases. This is mainly due to the PBTI degradations in transistors NI1 and NC which are used for discharging node O1. Compared with the original VLSA shown in Fig. 6(b), the proposed variation-tolerant speed-up design (Fig. 10) adds two skewed inverters (INVskew1, INVskew2) and two speed-up transistors (Nsp1, Nsp2). As O1 discharges from 1V to 0.8V, the high-skew inverter

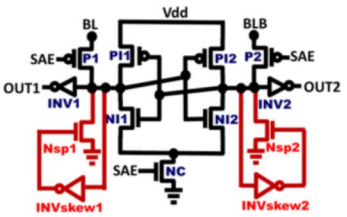

FIGURE 10. **Reliability-tolerant voltage latch sense amplifier with speed-up design. The skewed inverters (INVskew1 and INVskew2) and speed-up transistors (Nsp1 and Nsp2) are used to mitigate the sensing delay degradations due to BTI.**

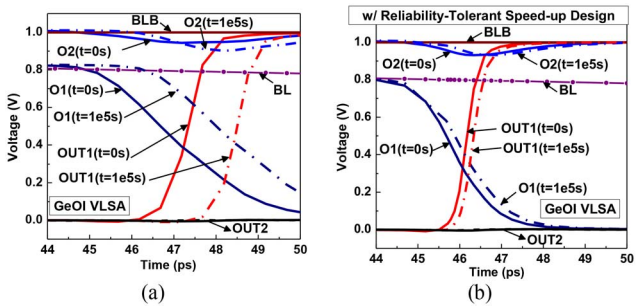

FIGURE 11. **Operation waveform comparisons for UTB GeOI VLSA (a) w/o speed-up design (Fig. 6(b)), and (b) with variation-tolerant speed-up design (Fig. 10). (ΔV_{BL} = 200mV).**

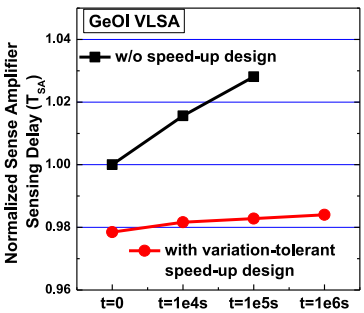

FIGURE 12. **Sense amplifier sensing delay comparisons for UTB GeOI VLSA with and without variation-tolerant speed-up design. (ΔV_{BL} = 200mV).**

(INVskew1) turns on the speed-up transistor (Nsp1), and therefore GeOI VLSA with speed-up design exhibits smaller T_{SA}. Besides, the proposed reliability-tolerant sense amplifier also exhibits smaller sense amplifier delay degradations as aging time increases as shown in Fig. 12.

V. CONCLUSION

The reliability-tolerant design for improving the stability and delay degradations due to NBTI and PBTI are investigated for UTB GeOI SRAM cell and sense amplifier. PBTI dominates the RSNM and HSNM degradations (ΔRSNM, ΔHSNM) for UTB GeOI SRAM cell, and ΔRSNM/ΔHSNM can be mitigated/compensated by high threshold voltage design. For SAE timing control, self-timed sensing scheme with a skewed NAND gate exhibits more tolerance to BTI stress than the inverter timing buffers. The proposed variation-tolerant speed-up design for UTB GeOI sense amplifier mitigates the BTI induced delay degradations, and exhibits smaller T_{SA} and ΔT_{SA} compared with the original VLSA design.

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