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A New Figure of Merit, $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$, to Characterize Short-Channel Performance of a Bulk-Si n-Channel FinFET Device

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ABSTRACT This paper aims to investigate the device parameters, including drain-induced barrier lowering (DIBL), subthreshold swing (SS), and saturation drive current, $I_{\mathrm{d,sat}}$, of bulk-Si n-channel FinFET devices (bulk n-FinFETs). The impact of lightly doped drain (LDD) process on the performance of bulk n-FinFETs is also examined in this paper. According to our measured data, excluding LDD in bulk n-FinFETs not only reduces mask costs but it also enables slightly better short-channel control compared to the inclusion of LDD. A new figure of merit, $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$, is introduced for monitoring short-channel performance of bulk n-FinFETs, where $\Delta V_{\mathrm{DIBLSS}}$ accounts for the DIBL and SS, and $I_{\mathrm{sd,leak}}$ is the source/drain subthreshold off-state leakage current.

INDEX TERMS Logic figures of merit (FoMs), bulk n–FinFETs, lightly doped drain (LDD), short–channel control, $\Delta V_{\mathrm{DIBLSS}}$, $I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}}$, short–channel performance.

I. INTRODUCTION

As the physical gate length, L_{g}, scales down to below 20 nm, planar metal–oxide–semiconductor field–effect transistor (MOSFET) devices reach the bottleneck in terms of gate controllability. The ultrathin–body and buried oxide (UTBB) silicon–on–insulator (SOI) MOSFET has been one of the candidates to extend the lifetime of planar MOSFETs to the 10 nm regime [1]–[4]. However, from the viewpoint of mass production of nanoscale MOSFETs, bulk–Si FinFETs are preferred over planar MOSFETs. The better gate controllability over the channel and lower leakage current render FinFET devices inherently superior to planar devices [5]–[7].

In this work we present a bulk–Si n–channel FinFET device (bulk n–FinFET) that has desirable transistor characteristics and competitive short–channel performance. Simultaneously, we compare the performance between including and excluding the lightly doped drain (LDD) process. We find that the short–channel performance is comparable, if not slightly improved, when we exclude the LDD process. It is also worth mentioning that excluding the LDD process significantly reduces the cost for masks. We introduce a new figure of merit (FoM), $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$, for the purpose of monitoring the electrical characteristics of bulk n–FinFETs. This FoM can be described as the short–channel performance factor representing the controllability of the gate voltage over the channel potential. The important parameters in bulk n–FinFETs, including drain–induced barrier lowering (DIBL), subthreshold swing (SS), saturation drive current, $I_{\mathrm{d,sat}}$, and source/drain (S/D) subthreshold off–state leakage current $I_{\mathrm{sd,leak}}$, are combined to reflect the overall performance of a device and to provide a criterion for the design of innovative devices.

II. DEVICE FABRICATION

Silicon wafer was used as the starting material in the manufacturing of n–FinFET devices. The major steps in the fabrication process are described as follows. After fin definition, ion implantation was carried out in order to adjust the threshold voltage, V_{t}, of bulk n–FinFETs. The resultant concentration of the channel dopant, BF_2, is 1.25×10^{19} cm^{-3} $\sim 2\times10^{19}$ cm^3. Then the polysilicon gate process took place,

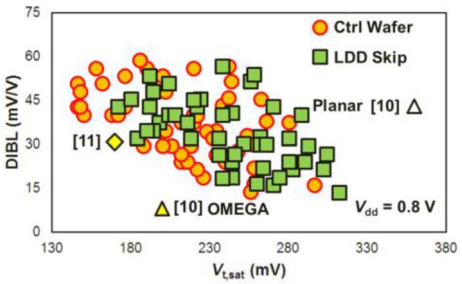

FIGURE 1. **DIBL versus $V_{t,sat}$ of bulk n–FinFETs with and without LDD. Reduction of charge sharing is observed in bulk n–FinFETs without LDD. This means that excluding LDD is more beneficial for further MOSFET L_g scaling.**

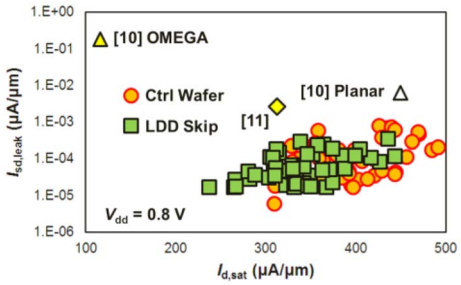

FIGURE 2. **$I_{sd,leak}$ versus $I_{d,sat}$ of bulk n–FinFETs with and without LDD. It is seen that the device excluding LDD results in higher $I_{d,sat}/I_{sd,leak}$ ratio. This can be attributed to the improved electrostatic gate control over the conduction channel.**

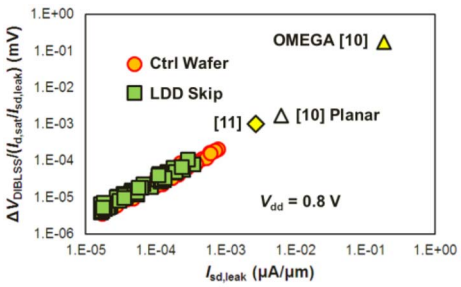

FIGURE 3. **$\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$ (short–channel performance factor) versus $I_{\mathrm{sd,leak}}$ of bulk n–FinFETs with and without LDD. As predicted, excellent short–channel device performance is exhibited in devices without LDD. Additionally, the short–channel factor is useful for demonstrating the importance of the characteristics of short–channel devices.**

followed by LDD implantation. The LDD width, W_{LDD}, is physically equal to the sidewall spacer width of between 2.7 nm and 3 nm, and the LDD As concentration is 3.5×10^{20} cm^{-3} $\sim 4.2\times10^{20}$ cm^{-3}. For the epitaxial S/D growth process, the sacrificial nitride layers were first deposited onto the silicon surface. The lithography and etching processes were then used to define the in–situ phosphorous doped silicon (SiP) recess structure in n–type devices. Subsequently the epitaxial growth of the SiP layer was performed, followed by S/D implantation. Next, rapid thermal processing was utilized to electrically activate the dopants. The subsequent processes were done using conventional high–k complementary MOS (CMOS) processes.

We also fabricated the bulk n–FinFET without LDD for comparison. The value of L_{g} is between 16 nm and 20 nm. The gate insulator thickness, T_{ox}, is between 1.97 nm and 2 nm. The fin width, W_{fin}, is between 6 nm and 8 nm, and the fin height, H_{fin}, is between 40 nm and 42 nm.

III. RESULTS AND DISCUSSION

Fig. 1 shows the graph of DIBL versus saturation V_{t}, $V_{\mathrm{t,sat}}$, for our bulk n–FinFETs including and excluding the LDD process. A slight improvement of DIBL has been observed with the exclusion of LDD. It should be noted that skipping LDD slightly increases the effective gate length, L_{eff}, reducing the influence of the electric field from the drain to the channel region. Furthermore, increasing the L_{eff} leads to the increase in total volume of the depletion region, υ_{tot}, and thus the increase in effective depletion charges controlled by the gate, Q_{eff}, according to the relationship [8]

$$Q_{\mathrm{eff}} = Q_{\mathrm{dep}}\left[1-\left(\upsilon_{\mathrm{s}}+\upsilon_{\mathrm{d}}\right)/\upsilon_{\mathrm{tot}}\right] \tag{1}$$

where υ_{s} is the total encroachment volumes controlled by the source; υ_{d} is the total encroachment volumes controlled by the drain. The increase in Q_{eff} implies better gate controllability over the channel charges. Thus, for bulk n–FinFETs without LDD, we can expect to see reduced DIBL and improved SS compared to bulk n–FinFETs with LDD. It is also found that the device performance remains similar with and without the LDD process as shown in Fig. 2. The slight negative shift in $I_{\mathrm{d,sat}}$ is attributed to the positive shift in $V_{\mathrm{t,sat}}$ shown in Fig. 1 due to the removal of the LDD process and can be readjusted via modifying the dosage of the channel implant.

Fig. 3 shows our newly introduced FoM, $\Delta V_{\mathrm{DIBLSS}}/(I_{\mathrm{d,sat}}/I_{\mathrm{sd,leak}})$ or the short–channel performance factor, plotted against $I_{\mathrm{sd,leak}}$. This FoM consists of the aforementioned important device parameters, namely DIBL, SS, $I_{\mathrm{d,sat}}$, and $I_{\mathrm{sd,leak}}$. The denominator simply consists of the ratio of the device's on–state current and its off–state current, which translates to its performance. The numerator accounts for DIBL and SS:

$$\Delta V_{\mathrm{DIBLSS}} = \Delta V_{\mathrm{DIBL}} + \Delta V_{\mathrm{SS}} \tag{2}$$

where ΔV_{DIBL} is the difference of the linear V_{t}, $V_{\mathrm{t,lin}}$, and $V_{\mathrm{t,sat}}$ and ΔV_{SS} is the change in gate voltage, V_{g}, required for the current to increase tenfold, which is the definition of SS. Fig. 4 graphically illustrates the meaning of the numerator. Although different organizations and institutions extract SS from different portions of the $I_{\mathrm{d}}-V_{\mathrm{g}}$ curve, the result of ΔV_{ss} remains the same regardless of the location of extraction. Thus, for the purpose of introduction of the new FoM, we define SS as ΔV_{g1} in Fig. 4, over which I_{d} increases tenfold to I_0. This way, it is easy to see in Fig. 4 that $\Delta V_{\mathrm{DIBLSS}}$ is simply the sum of $\Delta V_{\mathrm{g1}}(=\Delta V_{\mathrm{ss}})$ and $V_{\mathrm{t,lin}}-V_{\mathrm{t,sat}}(=\Delta V_{\mathrm{DIBL}})$.

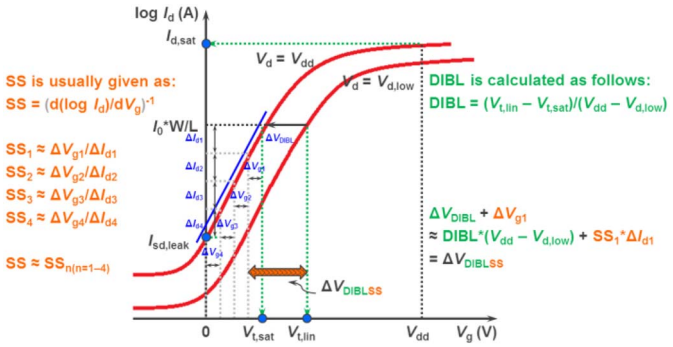

FIGURE 4. A physical explanation of the newly introduced FoM. It consists of the combination of DIBL and SS divided by the on/off ratio, and reflects the overall performance of FinFETs. Smaller SS results in improved on/off ratio and smaller DIBL results in smaller $I_{sd,leak}$. Hence, a small value of the FoM is desirable. I_0 is the current at which we define the V_t [9].

Since small values of both DIBL and SS and large values of the ratio of the on– and off–current are desired, a small value of the short–channel performance factor is favored. This is once again confirmed in the graph in Fig. 3, where $I_{sd,leak}$ has a positive relationship with the short–channel performance factor. Hence, lower values of short–channel performance factor indicate better short–channel behavior, which means that improvement of gate control over the depletion layer is obtained. This new FoM helps us quickly figure out the overall device performance metrics and can be used to monitor the charge sharing effect in nanoscale MOSFETs. Fig. 3 shows that the device without LDD has reduced charge sharing compared to the device with LDD. These benefits are attributed to the fact that the absence of LDD helps to both reduce the V_t roll–off and improve the SS.

Finally, we compare our electrical results with that of n–MOSFETs with different architectures to further demonstrate the universality of our new FOM. It is shown in Fig. 1 that the smaller $V_{t,sat}$ of the Ω n–MOSFET compared to the planar n–MOSFET results in a larger $I_{sd,leak}$. Also, the higher S/D parasitic resistance and the degraded mobility of the Ω n–MOSFET result in a smaller $I_{d,sat}$ [10]. From these observations, it is expected that the Ω n–MOSFET has larger short–channel performance factor compared to the planar n–MOSFET. This is indeed the case as shown in Fig. 3. In addition, it is seen from Fig. 3 that the bulk FinFET [11] shows a smaller value of short–channel performance factor compared to the planar n–MOSFET [10]. This is due to smaller values of DIBL and SS of FinFETs in comparison to planer MOSFETs. Furthermore, a clear linear trend of the short–channel performance factor is observed in Fig. 3. Thus, the FOM is useful for monitoring short–channel performance of nanoscale devices.

IV. CONCLUSION

We have demonstrated the performance of a bulk–Si n–channel FinFET device. We have also introduced a new FoM that reflects the overall device performance, and used it to show the influence of LDD on the device performance. We have shown that excluding the LDD process results in better short–channel performance of bulk n–FinFETs and hence is more beneficial for further MOSFET L_g scaling. Reduction in mask cost is also achieved as a result.

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REFERENCES

[1] A. Kranti, S. Burignat, J.-P. Raskin, and G. A. Armstrong, "Underlap channel UTBB MOSFETs for low-Power analog/RF applications," in *Proc. 10th Int. Conf.* Ultimate *Integr. Silicon*, Aachen, Germany, 2009, pp. 173–176.
[2] Q. Liu *et al.*, "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22nm node and beyond," in *VLSI Symp. Tech. Dig.*, Honolulu, HI, USA, 2010, pp. 61–62.
[3] Q. Liu *et al.*, "Impact of back bias on ultra-thin body and BOX (UTBB) devices," in *VLSI Symp. Tech. Dig.*, Kyoto, Japan, 2011, pp. 160–161.
[4] J.-P. Noel *et al.*, "Multi-VT UTBB FDSOI device architectures for low-power CMOS circuit," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2473–2482, Aug. 2011.
[5] X. Huang *et al.*, "Sub 50-nm FinFET: PMOS," in *IEDM Tech. Dig.*, Washington, DC, USA, 1999, pp. 67–70.
[6] D. Hisamoto *et al.*, "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.
[7] S.-Y. Kim and J. H. Lee, "Hot carrier-induced degradation in bulk FinFETs," *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 566–568, Aug. 2005.
[8] Y.-C. Eng *et al.*, "Numerical study of a highly scaled bulk MOSFET with block oxide and source/drain-tied structure," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1381–1387, May 2011.
[9] H.-G. Lee, S.-Y. Oh, and G. Fuller, "A simple and accurate method to measure the threshold voltage of an enhancement-mode MOSFET," *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 346–348, Feb. 1982.
[10] T.-S. Park *et al.*, "Threshold voltage behavior of body-tied FinFET (OMEGA MOSFET) with respect to ion implantation conditions," *Jpn. J. Appl. Phys.*, vol. 43, no. 4B, pp. 2180–2184, Apr. 2004.
[11] K.-R. Han *et al.*, "Device design consideration for 50nm dynamic random access memory using bulk FinFET," *Jpn. J. Appl. Phys.*, vol. 44, no. 4B, pp. 2176–2179, Apr. 2005.

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