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TFET-Based Power Management Circuit for RF Energy Harvesting

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ABSTRACT This paper proposes a Tunnel FET (TFET)-based power management circuit (PMC) for ultra-low power RF energy harvesting applications. In contrast with conventional thermionic devices, the band-to-band tunneling mechanism of TFETs allows a better switching performance at sub-0.2 V operation. As a result, improved efficiencies in RF-powered circuits are achieved, thanks to increased rectification performance at low power levels and to the reduced energy required for a proper PMC operation. It is shown by simulations that heterojunction TFET devices designed with III–V materials can improve the rectification process at received power levels below −20 dBm (915 MHz) when compared to the application of homojunction III–V TFETs and Si FinFETs. For an available power of −25 dBm, the proposed converter is able to deliver 1.1 μW of average power (with 0.5 V) to the output load with a boost efficiency of 86%.

INDEX TERMS Energy harvesting, power management, radio-frequency, tunnel FET, UHF, ultra-low power.

I. INTRODUCTION

With the fast progression in the development of low power embedded systems, the design of efficient circuits at reduced voltage operation has gained momentum in recent years [1], [2]. Such low voltage and power systems, like biomedical implants or wearable devices, could benefit from harvesting surrounding electromagnetic radiation, thus reducing battery size and extending its lifetime. Several works have already demonstrated wireless powering of a load at short distances with UHF radiation at legally transmitted power levels [3]–[11]. However, the received radiation power attenuates with distance, and low power conversion efficiency (PCE) demonstrated by front-end rectifiers at low RF power levels (<-20 dBm) constrains the operation distance of RF energy harvesters.

Low power levels of electromagnetic radiation produce low output voltage values in the receiving antenna and therefore, efficient rectifiers are required for a proper system operation. Under extreme low-power/voltage scenarios (sub −20 dBm) conventional CMOS technologies cannot perform efficiently in RF rectifiers. In contrast, the Tunnel Field-Effect Transistor (TFET) appears as an interesting alternative. Due to the band-to-band tunneling (BTBT) carrier injection mechanism, the TFET device presents a sub-threshold swing (SS) below 60 mV/dec (room temperature) and low leakage current [12]–[14]. These characteristics make this technology attractive for ultra-low voltage/power front-end rectifiers and switched capacitors, as shown by recent works [15]–[17]. The decrease of energy per switch also allows the design of more efficient digital cells when compared to conventional CMOS [18]–[20].

In this work, a TFET-based power management circuit (PMC) for RF energy harvesting is designed and simulated showing promising results at RF available power levels below −20 dBm. The PMC adapts its input impedance to the output of the rectifier in order to allow the maximum power transfer to the input of the boost converter. Once the output of the boost converter reaches 0.5 V, a load is enabled. In Section II, the structure and electrical characteristics of

the TFET device are explained; Section III addresses the problems in RF systems associated with ultra-low power levels; Section IV explains the proposed TFET-based PMC; Section V presents the simulation results and Section VI presents the conclusions.

II. TUNNEL FET VS. FINFET DEVICE

A. PHYSICAL CHARACTERISTICS

Unlike thermionic devices such as FinFETs [21], see Fig. 1 (a), the TFET is designed as a reverse biased *p-i-n* diode. As shown in Fig. 1 (b), for both *n* and *p*-type TFETs the source region is characterized by a higher doping concentration than that of the drain. For an *n*-type TFET, under forward bias conditions the drain (*n* doped) is at a higher potential level than that of the source. In contrast, the *p*-type TFET is forward biased when the source (*n* doped) is at a higher potential than that of the drain.

As it will be explained in the following sub-section, TFETs designed with different source and drain materials present improved electrical characteristics compared to homojunction structures. Therefore, vertical TFET structures such as the one shown in Fig. 1 (c) are currently under investigation in order to reduce the device footprint area and due to the feasibility of the heterojunction structure implementation [22], [23]. In this work, TFETs with double-gate structures as the one presented in Fig. 1 are considered for simulation purposes.

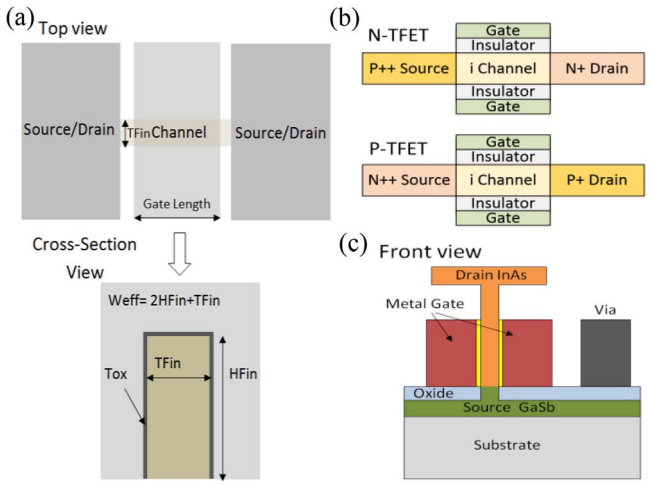

FIGURE 1. (a) FinFET structure, adapted from [21]; (b) double-gate TFET doping structure and (c) vertical TFET structure, adapted from [23].

B. BAND-TO-BAND TUNNELING MECHANISM

Due to the different doping structure of TFETs (*p-i-n*) the main carrier injection mechanism is characterized by Band-to-Band Tunneling (BTBT). In Fig. 2 (a), the energy band diagram of an *n*-TFET is presented. During the off-state condition shown by the dashed curves (V_{GS}=0V, V_{DS} > 0V) both the valence band in the source region and conduction band in the channel region are aligned, thus setting a large channel resistance and consequent lower leakage current when compared to thermionic devices. Once the V_{GS} of the TFET device increases (solid curves), the conduction band in the channel moves below the valence band of the source region thus increasing the probability of electrons in the source region to tunnel through the channel to the empty states of the drain region.

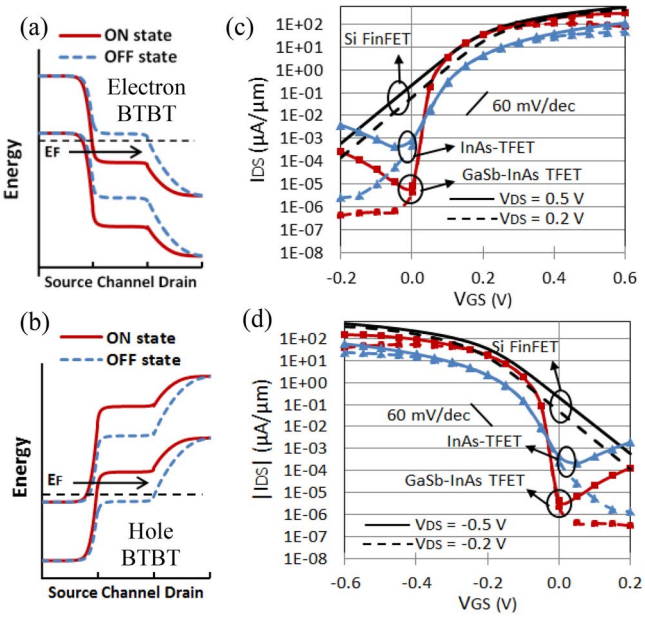

FIGURE 2. (a) n-TFET and (b) p-TFET Energy band diagram. Input characteristic for (c) n-type and (d) p-type devices. Homo-TFET: Lg20 nm, P+ InAs Source NA=4x1019 cm-3; N+ InAs Drain ND=6x1017 cm-3, TCH=5 nm, Tox=5 nm, HiK (HfO2), EOT=1 nm, ΦM=4.78 ev. Hetero-TFET: Lg=40 nm, P+ GaSb Source NA=4x1019 cm-3; N+ InAs Drain ND=2x1017 cm-3, TCH=5 nm, Tox=2.5 nm, HiK (HfO2), EOT=1nm, ΦM=4 ev.

As shown in Fig. 2 (b), in a *p*-TFET, a negative bias applied to both channel and drain regions (respective to the source) increases the energy levels in the channel, thus increasing the probability of holes in the source region to tunnel through the channel to the empty states of the drain.

In [13], the progress toward the development of TFETs is reviewed, showing the improved performance of staggered and broken gap TFETs designed with low energy band gap materials. Group III-V materials such as InAs and GaSb allow for an increase of carrier transmission probability and hence larger drive current at low voltage due to their lower band gap. In contrast, TFETs designed with group IV materials such as Silicon (Si) and Germanium (Ge) exhibit smaller drive-currents resulting from their indirect band gaps and lower tunnel probability. Similar to *n*-TFETs, *p*-TFETs designed with III-V materials exhibit improved performance when compared to all Si-*p*-TFETs. However, the performance of *p*-TFETs is limited due to the low conduction-band density-of-states of the *p*-channel. In [14] the authors show that despite the degraded SS of *p*-TFETs, they can have

a comparable drive-current to *n*-TFETs (approx. 0.5x) for a similar off-current target.

C. CURRENT-VOLTAGE AND CAPACITANCE-VOLTAGE CHARACTERISTICS

In this sub-section, the current-voltage characteristics of a state-of-the-art Silicon FinFET and two different III-V TFET structures (homojunction and heterojunction) are presented. The behavior of both TFETs at a device-level is simulated with a Verilog-A model using look-up tables describing the main electrical characteristics of the device. Both current-voltage and capacitance-voltage characteristics were obtained from TCAD Sentaurus device simulator by the NDCL group at PSU. The Verilog-A model describes the behavior of a 40 nm double-gate GaSb-InAs TFET and 20 nm double-gate InAs TFET calibrated through full-band atomistic simulations with a dynamic non-local band-to-band tunneling model. The Si FinFET is simulated with a triple-gate configuration, fin height of 28 nm, fin width of 15 nm and gate length of 20 nm. More information about these models can be found in [21] and [24].

In Fig. 2 (c) and (d) the input-characteristic of both technologies is compared. It is shown that both TFETs present lower leakage current compared to the FinFET counterpart and a sub-60 mV/dec of SS. It is also shown that considering a low V_{DS} of |0.2 V| both *n* and *p*-type heterojunction TFETs present a larger drive-current than that of the FinFET in the V_{GS} range of |50-250| mV. In Fig. 3 (a) the output-characteristics of the *n*-type heterojunction III-V TFET shows a larger drive-current when compared to both homojunction TFET and FinFET at a V_{GS}=0.2 V for a V_{DS} range of 50 mV to 0.5 V. With a gate length of 20 nm, one can see the important effect of the channel length modulation in the current behavior of the FinFET. In contrast, the current of both TFETs is shown saturated due to the BTBT carrier injection mechanism. An important consequence of the different TFET structure is the reverse bias behavior. Under reverse bias conditions (negative V_{DS} for *n*-type and positive V_{DS} for *p*-type TFET), the intrinsic *p-i-n* diode of the device is forward biased and the resulting reverse current is characterized by two different carrier injection mechanisms.

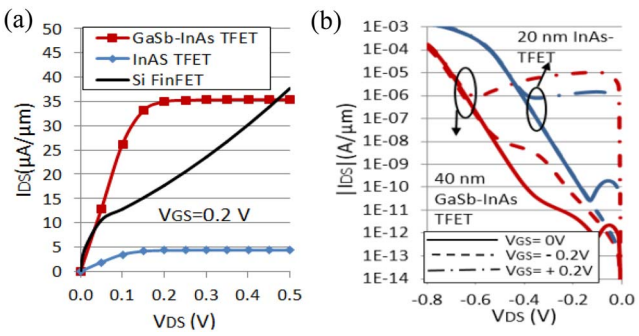

FIGURE 3. (a) Output characteristics of Si FinFET, Homojunction TFET and Heterojunction TFET. (b) Current of n-TFETs under reverse bias conditions.

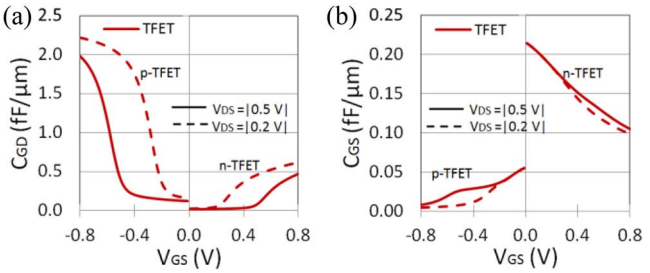

FIGURE 4. (a) Gate-to-drain and (b) gate-to-source intrinsic capacitance of TFET.

For an *n*-TFET, a low reverse bias results in a reverse current characterized by BTBT carrier mechanism occurring at the channel-drain interface. As long as reverse bias increases ($V_{DS} \ll 0$ V) the BTBT mechanism is suppressed due to the increase of energy bands in the drain region, and the drift-diffusion (DD) mechanism characterizes the current. The transition between the two mechanisms results in a negative differential resistance (NDR) as shown in Fig. 3 (b). When a negative V_{GS} is applied to a reverse biased TFET, the NDR is not observed and DD characterizes the reverse current. However, in the case of GaSb-InAs heterojunction TFET, a V_{GS}=0 V applied to a reverse biased TFET can reduce the reverse current for a significant range of V_{DS} (−0.1 V to −0.6 V). This characteristic is important in the design of TFET-based circuits (e.g., boost converters) as it allows the reduction of unwanted reverse current and consequent reverse power.

In TFET devices, the intrinsic gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances as a function of the gate bias present a different behavior when compared to conventional thermionic devices. As shown in Fig. 4, the total gate capacitance of the heterojunction TFET is dominated by C_{GD}. As the TFET current is dependent on the barrier shrinking in the source-channel interface, the resulting C_{GS} is shown much lower than C_{GD} when the transistor is active. Compared to conventional CMOS-circuits, this characteristic can enable the design of TFET-based circuits with lower switching losses.

III. RF POWER TRANSPORT

In Fig. 5, the structure of the RF power transport system considered in this work is presented. The receiver comprises a receiving antenna with 50 Ω standard impedance followed by a lumped matching network between the antenna and the rectifier. The power management circuit (PMC) boosts the rectifier output voltage to a higher stable voltage in order to power a load/sensor.

The main challenge in the receiver of the RF power system is to overcome the power-density attenuation due to long distances between the transmitter and receiver part. Friis equation expressed by (1) shows that the power received at the input of the rectifier is dependent on the transmitted power P_t, transmitter and receiver antenna gain G_t and

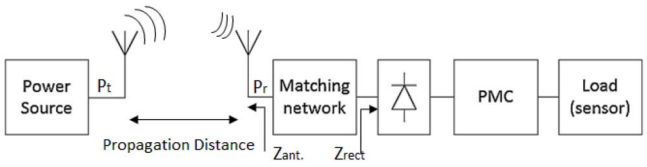

FIGURE 5. RF Power Transport System.

G_r respectively, wavelength λ_o of the transmitter signal and propagation distance R [1]. If the receiver antenna is well matched with the rectifier, the relation between the output of the antenna V_A and the received power can be expressed as (2), with R_A representing the real part of the antenna impedance.

$$P_r = P_t G_t G_r \left(\frac{\lambda_o}{4\pi R}\right)^2 \quad (1)$$

$$V_A = \sqrt{8 R_A P_r} \quad (2)$$

In Table 1, the license-free Industry-Science-Medical (ISM) frequency bands for different regions are indicated [1]. Considering two different frequency bands (915 MHz and 2.4 GHz), a maximum regulated transmitter power of 4 W and taking into account expressions (1) and (2), one can calculate the received power and the output of the antenna as a function of the propagation distance R as shown in Fig. 6 (assuming antenna gains of 1). The power density attenuation at the input of the rectifier as a function of the propagation distance constrains the operation of RF systems to short distances.

TABLE 1. Frequency band allocations and maximum transmitter power [1].

Freq. Band (MHz)	Transmitter Power	Region
2446-2454	500 mW-4 W (EIRP)	Europe
867.6-868	500 mW (ERP)	Europe
902-928	4 W (EIRP)	USA/Canada
2400-2483.5	4 W (EIRP)	USA/Canada
2400-2483.5	10 mW (EIRP)	Japan/Korea

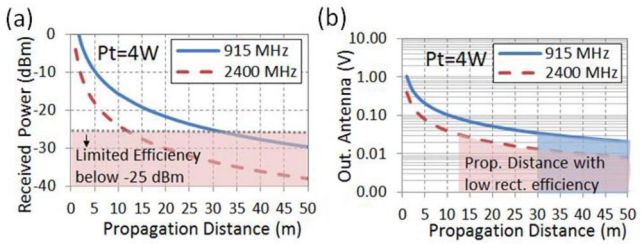

FIGURE 6. (a) Received power and (b) output of the antenna as a function of propagation distance for transmitter power = 4 W.

As an example and according to Fig. 6 (a) the receiving antenna is sensing -25 dBm at a propagation distance of 30 m from the transmitter (915 MHz, 4 W). As shown in Fig. 6 (b), at 30 m the receiving antenna produces an output voltage of 36 mV. At such low voltage levels, there is a clear difficulty of rectification as shown by the recent results from the state-of the-art CMOS rectifiers shown in Fig. 7.

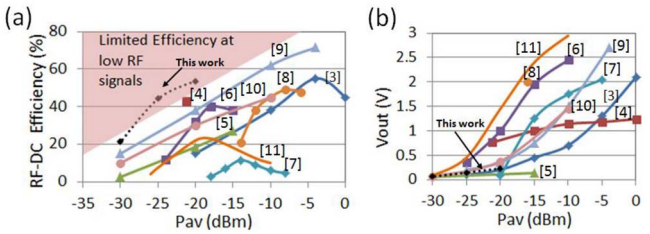

FIGURE 7. State-of-the-art CMOS rectifier PCE (a) and output voltage (b) as a function of available power.

In order to increase the input voltage of the rectifier, a resonating LC network [1], [6] optimized for a desired input power level can be inserted at the output of the antenna as shown in Fig. 8 (a). In this work, the gate cross-coupled rectifier (GCCR) shown in Fig 8 (b) is considered for simulation purposes and matched with a 50 Ω antenna.

In Fig. 9 (a), the efficiency of one-stage GCCR designed with different technologies is presented. Each one of the four transistors is simulated with a channel width of 10 μm. The matching network with L and C elements is optimized for each rectifier considering an available power of −20 dBm. The results show that the heterojunction III-V TFET-based rectifier presents higher rectification efficiencies in the range of -30 to -25 dBm when compared to the FinFET-based rectifier. At these low power levels the homojunction TFET-based GCCR presents the lowest efficiency values. Compared to the FinFET-based rectifier, the higher efficiency shown by the heterojunction TFET-based counterpart is explained due to the better switching performance of individual TFET transistors at sub-0.2 V operation.

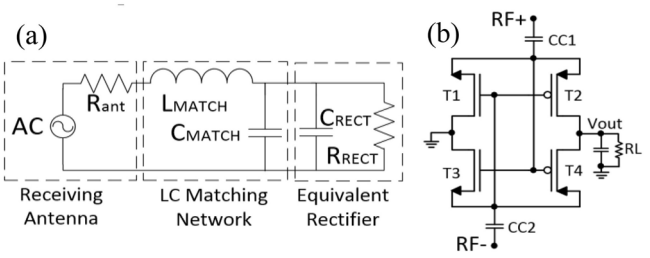

FIGURE 8. (a) Eq. circuit of antenna-matching-rectifier; (b) GCCR topology.

As shown by the authors in [15] and compared to conventional CMOS, the larger drive current, lower leakage current and lower parasitic capacitances of TFETs enable this technology as a good candidate for ultra-low power rectification.

Focusing on the heterojunction TFET-based rectifier, Fig. 9 (b) shows that at different power levels, the range

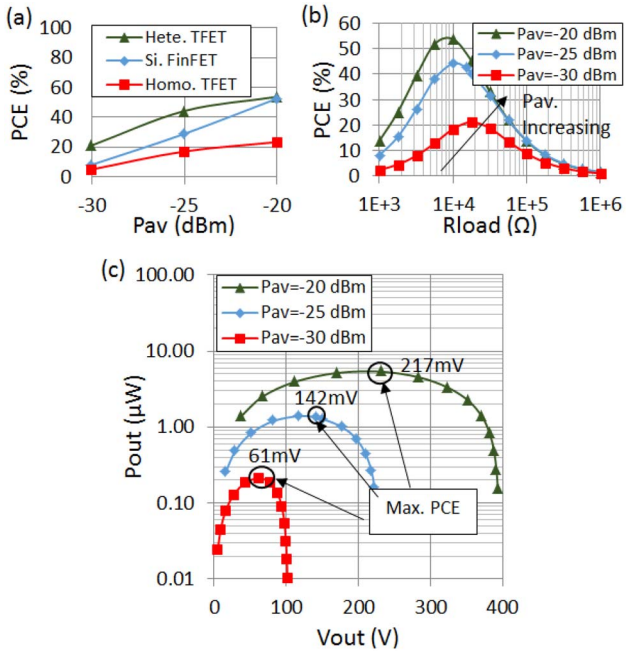

FIGURE 9. **(a) Rectifier efficiency as a function of available power for different devices; (b) Hetero. TFET-based rectifier PCE as a function of output load, (c) Output power as a function of output voltage for hetero. TFET-based rectifier.**

of optimum loads for maximum efficiency changes. One can see that as long as the available power increases the optimum load value for maximum efficiency decreases. This behavior results in an increase of the optimum rectifier output voltage as shown in Fig. 9 (c). For a good PMC design, knowing the load range that maximizes the rectifier efficiency is mandatory in order to allow maximum transfer of power from the rectifier to the input of the boost converter.

IV. POWER MANAGEMENT CIRCUIT AND DESCRIPTION

In Fig. 10 (a), the building blocks of the proposed TFET-based PMC are presented. The RF source is considered as a port with 915 MHz and 50 Ω impedance. After matching and rectification the PMC is required to boost the output of the rectifier to 0.5 V and then enable a load. The PMC is divided in three distinct modules: startup, controller and boost circuit.

A. STARTUP CIRCUIT

In this work we propose a startup circuit that avoids the use of any external power source for proper PMC functioning. As shown in Fig. 10 (a) a ring oscillator powered by the output of the rectifier is required for generating two non-overlapped clock signals that are applied to a multi-stage gate cross-coupled charge pump (GCCCP). In [16] it was shown by simulations that a TFET-based GCCCP can double its input voltage with magnitudes as low as 80 mV. In this work, the charge pump is required to charge the capacitor connected to the node *Vddstartup*. This capacitor is used to power all the analog and digital circuitry of the startup module.

A voltage monitor is used to trigger a signal *setboost* whenever the node *Vddstartup* reaches 200 mV. This signal is required to enable the boost conversion. A voltage reference circuit is designed, providing a fixed 50 mV signal to the comparator of the voltage monitor block. Before enabling the boost conversion, the input *Cboost* and output *Cout* capacitors of the boost converter are pre-charged to

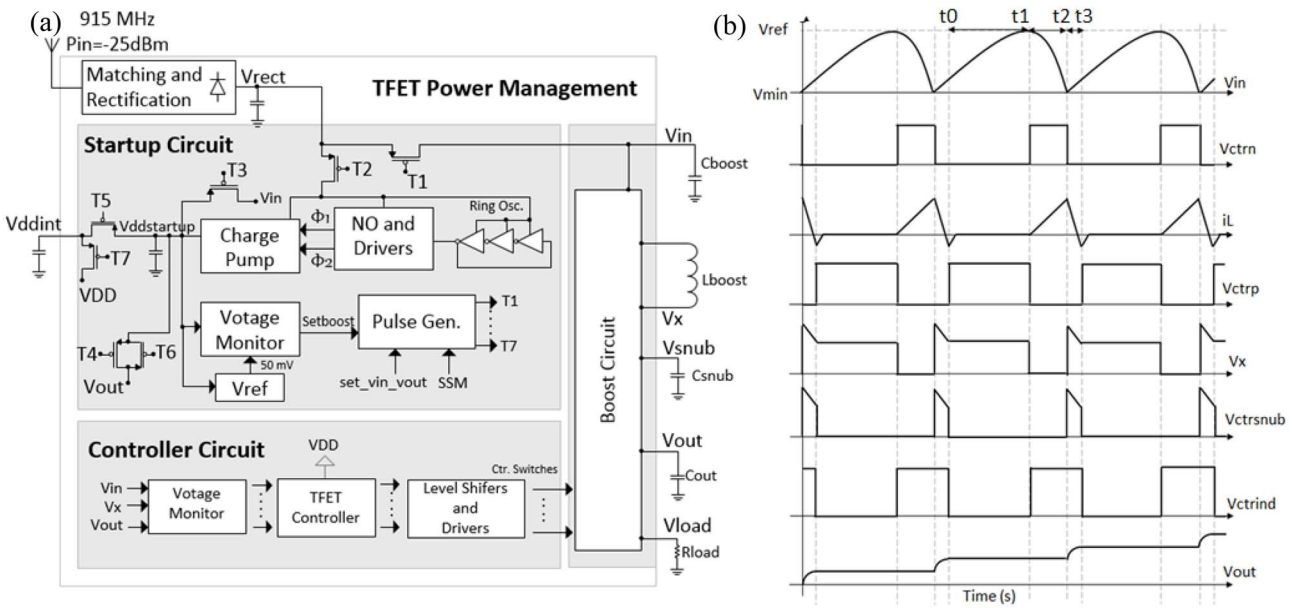

FIGURE 10. **(a) Proposed RF TFET-based Power Management Circuit, (b) Operation sequence of main electrical signals when the boost controller is enabled.**

200 mV (from node *Vddstartup*) by the TFET switches controlled by T3 and T4. Once charged, a signal *set_vin_vout* is enabled and the boost operation takes place.

The TFET switch controlled by T1 is required to allow the charging of the capacitor connected to the input of the boost converter. The output of the rectifier is responsible for this charging whenever the signal *setboost* is active. The TFET switch controlled by T5 is required to allow the charging of the capacitor at node *Vddint* to the same voltage level of node *Vddstartup*, i.e., 200 mV and the switch controlled by T7 to enable this capacitor as the power source of the digital and analog circuitry in the controller module. Once the output load of the system is enabled, i.e., node *Vload* goes from low-to-high state, a signal *SSM* (Self-Sustaining Mode) is triggered.

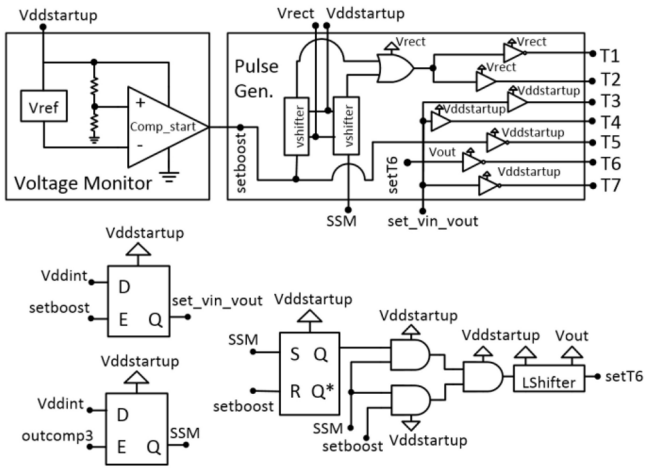

FIGURE 11. Digital and analog circuitry of the startup module.

Once *SSM* is enabled, the TFET switch T2 deactivates the ring oscillator, clock signals and the charge pump circuit. At this time, the output capacitor *Cout* is responsible for charging the capacitor connected to the node *Vddstartup* through the TFET switch controlled by T6.

The digital and analog circuitry of the voltage monitor and pulse generator are shown in Fig. 11. In the voltage monitor, the differential-pair of the two-stage comparator is biased with 50 mV coming from the voltage reference. The signal *outcomp3* is responsible for triggering the *SSM* signal, coming from the controller as shown in Section IV-C. Inside the startup module, two level shifter circuits are required to match the voltage of both the input and power source of digital cells. The importance of level shifters in TFET-based circuits is explained in Section IV-C.

B. BOOST CIRCUIT

In order to increase the output voltage of the rectifier to voltage values suitable to the output load, a boost converter is required. In Fig. 12 an inductor-based boost converter topology for TFET devices is proposed. The sequence of operation for the gate controls of each TFET device is shown in Fig. 10 (b). After a proper startup operation and *setboost* signal enabled, the input capacitor *Cboost* is charged and discharged maintaining an average voltage adequate for maximum rectifier efficiency. This matching technique is used by several works [25]–[27], allowing a maximum transfer of power to the boost converter.

The suitable matching voltage depends on the received power. According to the power-voltage relationship displayed in Fig. 9 (c), the optimum reference input voltage (*Vin* between *Vref* and *Vmin* in Fig. 10 (b)) is 142 mV for a received power of -25 dBm. If the received power changes, these reference values have to change accordingly. Therefore, during the time interval t0 to t1 the input capacitor *Cboost* is charged by the rectifier up to *Vref*. During this time interval, no current should flow through the inductor. Therefore, the TFET device S1 in Fig. 12 is closed and only a small current flows through the inductor.

The absence of body diode in reverse biased TFETs (due to a different doping structure than that of MOSFETs) requires a change in the conventional boost converter topology. While the output transistor S4 is reverse-biased during the time interval t0 to t1, a snubber circuit (designed with TFET device S3 and a capacitor C_{snub}) is required in order to provide a path for the inductor current.

During t1 to t2 the TFET device S2 is closed in order to charge the inductor from the input capacitor, until the latter is discharged to a minimum reference value. During this time interval the remaining transistors are open.

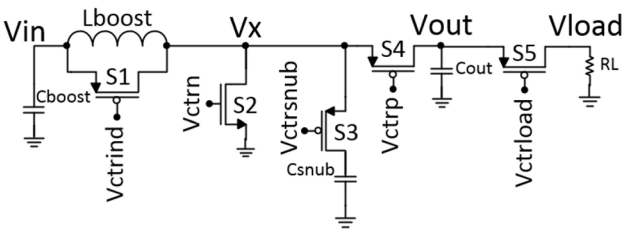

FIGURE 12. Proposed boost converter topology for TFET devices.

During the time interval t2 to t3 TFET S4 is closed so that the stored energy in the inductor is transferred to the output capacitor *Cout*, increasing its voltage. Only when the output of the boost converter achieves a reference value of 510 mV the TFET device S5 is closed. An external load is then enabled until the output capacitor is discharged to 490 mV.

B.1. CHALLENGES IN TFET-BASED BOOST CONVERTER DESIGN

In order to increase the boost conversion efficiency, it is mandatory to keep a low reverse current conduction from the output transistor S4 during the time interval t0 to t2, i.e., when the device is reverse biased ($V_{DS} > 0$ V), see Fig. 13 (a). The larger the voltage difference between nodes

Vout and *Vx*, the larger the reverse current conducted by S4 will be, and the faster the output capacitor will discharge.

Fig. 13 (b) shows the reverse current magnitude of the three technologies under study as a function of reverse V_{DS}. The V_{GS} of TFETs is set to 0 V in order to reduce the reverse current (as explained in Section II-C), while a V_{GS}=V_{DS} is considered for the reverse biased FinFET.

During the time interval t0 to t1, the source node of the output transistor S4 equals *Vin* (assuming that no current is flowing in the inductor) and therefore V_{DS} of S4 is *Vout*-*Vin*. As an example, if the input voltage of the boost converter is 0.2 V and the required output voltage is 0.5 V (V_{DS}=0.3 V), then during this time interval the reverse current conducted by the GaSb-InAs TFET device S4 is more than 2 orders of magnitude higher than the FinFET device S4 for a similar channel width. Since the time interval t0 to t1 dominates the period of the boost operation, an increase of boost frequency can reduce the discharge of the output capacitor *Cout*.

During the time interval t1 to t2, the source node of the output transistor S4 is at 0 V and its V_{DS} equals *Vout*. Considering the previous example, if one requires a *Vout*=0.5 V then the reverse current conducted by the heterojunction TFET device S4 is more than 6 orders of magnitude higher than a FinFET S4 device for a similar channel width. During this time interval, an inductor current larger than the reverse current of S4 is required in order to allow the storage of energy in the inductor. In order to reduce the discharge rate of *Cout* and consequently improve the boost efficiency, several solutions can be adopted: decrease the boost frequency, decrease the size of S4 or increase the size of the output capacitor.

During the time interval t2 to t3, S4 is forward biased conducting current from the inductor to the output capacitor.

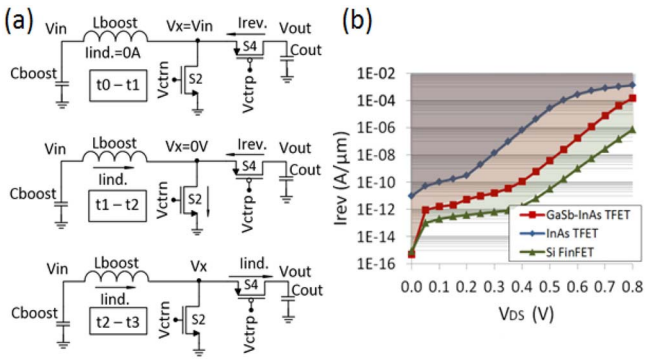

FIGURE 13. (a) Top: Cboost charging from rectifier; Middle: Inductor charging from Cboost; Bottom: Inductor discharging to Cout; (b) Reverse current for different technologies as a function of V_{DS}.

Therefore, in order to increase the boost efficiency (decreasing S4 losses during its forward bias interval) it is preferable to have an output transistor with a large size. Therefore, there is a trade-off between choosing a large transistor S4 to reduce forward conduction losses, or a small

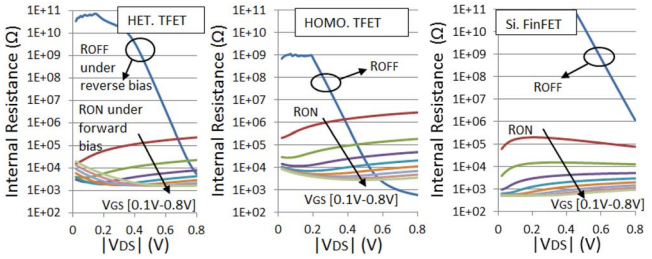

FIGURE 14. Internal resistance under reverse (V_{DS} < 0V) and forward (V_{DS} > 0V) bias. For FinFETs under reverse bias V_{GS}=V_{DS}, whereas for TFET V_{GS}=0V.

transistor to attenuate the reverse current. A boost operation with large frequencies can decrease the losses of S4 during the time interval t0 to t1. However, larger frequencies of operation result in larger average reverse power of S4 during the time interval t1 to t2.

B.2. ADVANTAGES OF TFETS IN BOOST CONVERTERS

The analysis of the device internal resistance as a function of $|V_{DS}|$ is useful to evaluate the performance of the device in a boost converter. As shown in Fig. 14, the heterojunction TFET device presents the lowest internal resistance under forward bias conditions at sub-0.25 V. When compared to conventional MOSFETs, this characteristic allows for lower conduction losses in the input transistor S2 during the time interval t1 to t2, and lower conduction losses in the output transistor T4 during the charging time of the output capacitor. Furthermore, the lower static and dynamic power consumption of TFET-based circuits at 0.2 V allows for a minimization of energy required for a proper boost controller operation when compared to the use of conventional thermionic technologies. The larger current conducted by TFETs at sub-0.2 V operation allows a decrease of the transistor size compared to thermionic devices (for a similar drive current) and a consequent minimization of the buffer sizes.

C. TFET-BASED CONTROLLER CIRCUIT

The proposed TFET-based controller circuit shown in Fig. 15 is responsible for providing the control signals to the switches in the boost converter presented in Fig. 12. In order to reduce the reverse losses of the TFETs and improve the controller efficiency, the circuit imposes a V_{GS}=0 V to all the TFET devices under reverse bias state. The differential pairs of the two-stage comparators are biased with 50 mV coming from the voltage reference of the startup circuit. The first comparator is required to trigger the *Vctrn* signal, maintaining the voltage of the input capacitor *Cboost* between a minimum and a reference voltage. The second comparator is required to detect when the inductor current is negative, triggering a *Reset* signal that is applied to an RS latch. Depending on the state of *Vctrn* the output transistor S4 is conducting or blocking current according to the signal *Vctrp*. The third comparator

is required to control the device S5 when the node *Vout* is in the range between 490 mV and 510 mV. When both the input S2 and output S4 devices are operating in the off-state, the control signal *Vctrind* is triggered from an RS latch.

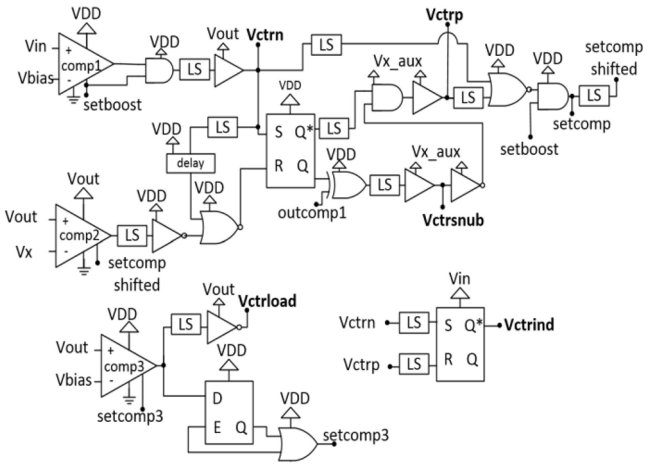

FIGURE 15. **Proposed TFET-based controller circuit for the boost converter.**

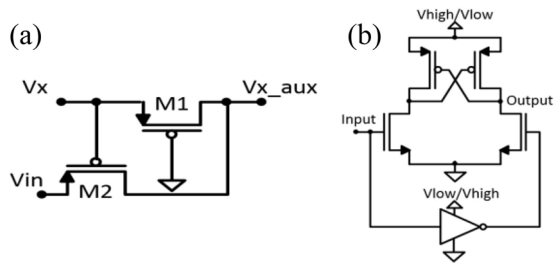

FIGURE 16. **(a) Vx_aux generator circuit and (b) Level shifter (LS) block.**

In order to maximize the controller efficiency, the three comparators only operate during the fraction of time when both *Vctrn* and *Vctrp* signals are at 0 V. This condition triggers the signal *setcomp*. The *Vctrp* and *Vctrsnub* signals are generated by buffers powered by *Vx_aux*. Since the node *Vx* in Fig. 12 is grounded during the operation time t1 to t2, the above mentioned buffers cannot be powered directly by *Vx*. Therefore, a different circuit is required. In Fig. 16 (a), the proposed circuit guarantees that during the time interval t1 to t2, the voltage node *Vx_aux* equals the voltage node *Vin* (M1 is open and M2 closed). During the time interval t2 to t3, the node *Vx* is at a higher voltage than that of the node *Vin* and therefore *Vx_aux* equals *Vx* (M1 is closed and M2 is open).

TFET-based digital gates are very sensitive to mismatch between digital levels and power supply. In order to improve the controller efficiency, level shifter (LS) blocks are required to match the voltage at the input of the various digital cells with the applied power supply voltages. In Fig. 16 (b) the topology of the TFET-based level shifter is presented.

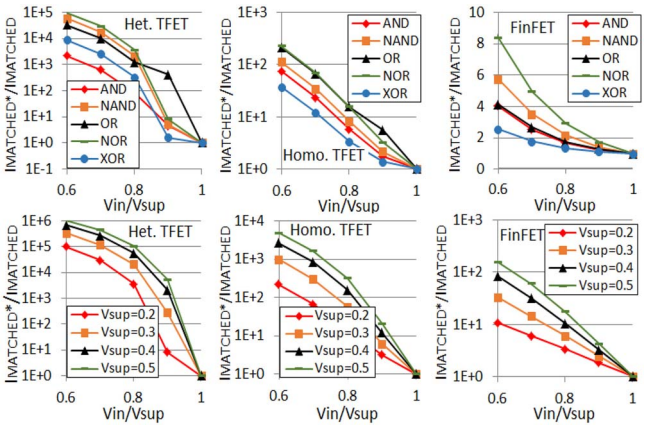

FIGURE 17. **Increase of power consumption in digital cells (top) with Vsup=0.2 V and inverters (bottom) as a function of different ratios between the input voltage and the power supply voltage for different technologies.**

A detailed study of TFET-based LS and the power consumption associated with the voltage conversion can be found in [28].

Fig. 17 shows the increase of power consumption in several digital cells used in the proposed PMC as a function of ratio between the input voltage of the cell and a power supply voltage of 0.2 V. In the *y* axis, "$I_{MATCHED}$" is the nominal current consumption of the cell when the magnitude of the input voltage of the cell equals the power supply voltage (0.2 V) and "$I_{MATCHED}$*" represents the increase of power consumption when the input voltage of the cell is lower than the power supply voltage. It can be seen that for heterojunction TFETs a voltage ratio of 0.6 between the input and power supply voltages can increase the power consumption of the cell by several orders of magnitude, so that the use of LS is mandatory.

V. SIMULATION RESULTS

This section presents simulation results to evaluate the performance of a TFET-based PMC designed with the heterojunction III-V TFET models described in Section II-C. The drive current of p-TFET devices is assumed to be half of that of the n-TFETs due to the p-TFET performance degradation. The C-V characteristics of both *n*-TFET and *p*-TFET devices are different [24]. In Fig. 18, the transient simulations of the circuit are presented for an available RF power of -25 dBm. It is shown that before the boost conversion operation, the input capacitor *Cboost* and output capacitor *Cout* of the boost converter are pre-charged to 200 mV. Once charged, the power supply node of the controller is enabled (*VDD*) and the boost converter enters in a synchronous mode of operation. The voltage at the input node of the boost converter (*Vin*) is regulated with an average voltage of ∼142 mV, thus allowing maximum transfer of power from the rectifier (1.28 μW) according to Fig. 9 (c).

In Fig. 19 the performance of the boost converter is presented, considering an output load of 166.7 kΩ. Once

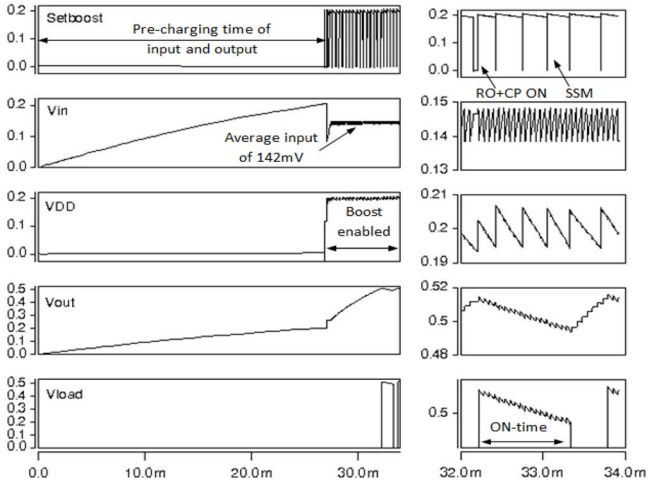

FIGURE 18. **Simulation results of the proposed TFET-based PMC for RF Pav=-25 dBm. L1=10 mH, Cboost=0.05 μF, Cout=0.05 μF, Csnub=2 nF, Rload=166.7 kΩ, WS1=10 μm, WS2,3,5=100 μm, WS4=25 μm.**

the load is enabled, an instantaneous output power of 1.5 μW is observed. When considering an input boost capacitor value of 0.05 μF, boost conversion efficiencies close to 90% are achieved for an inductor value of 10 mH.

According to [27] the inductor current and the boost frequency are proportional to the size of the input capacitor. Larger current values with larger capacitors require larger input and output transistors to reduce the conduction losses and increase the PCE of the boost conversion. However, the increase of the output transistor not only results in larger switching losses but also larger conduction of reverse current and consequent reverse losses. As shown in Fig. 19 and depending on the frequency of operation, there is an optimum size for the output transistor S4 that maximizes the efficiency of the boost conversion. Despite the consequent increase of the circuit die area, the choice of large boost inductors produces higher conversion efficiency values due to resultant reduction of the boost peak current, as shown in Fig. 19.

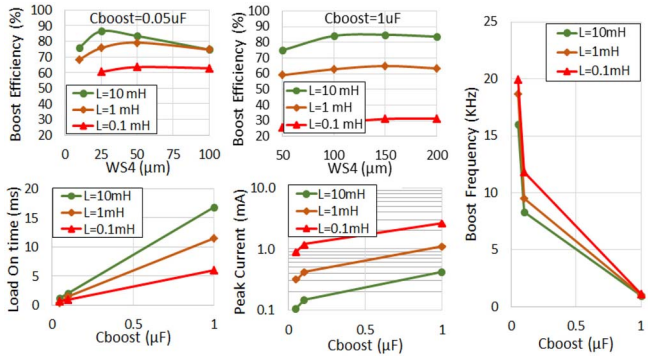

FIGURE 19. **Performance of TFET-based boost converter for RF Pav=-25 dBm. Cout=Cboost, Csnub=2 nF, Rload=166.7 kΩ, WS1=10 μm, WS2,3,5=100 μm.**

For an inductor of 10 mH, a parasitic series resistance of 30 Ω is considered. As the average inductor current is in the order of μA, the losses associated with this resistance value represent a small fraction of the total power losses in the boost converter.

Fig. 20 shows the distribution of the power losses for the TFET-based PMC where maximum boost conversion efficiency was achieved (86 %). The startup circuit is shown to consume 41.9 nW, controller circuit 11.88 nW and boost converter 116 nW, with a great part of these losses coming from the TFET switches present in the circuit. In Table 2, a comparison between the results presented in this work and RF-powered PMC from the literature is presented, showing the promising performance of TFET-based PMC at μW power level applications.

TABLE 2. **Comparison with state of the art rf pmc.**

	[25]	[26]	[27]	This work
RF Freq.	1.93 GHZ	2.45GHz	950 MHz	915 MHz
Tech.	350 nm	-	180 nm	40 nm TFET
Startup	Ext. Battery	Battery-less	Battery-less	Battery-less
Vout	1.4V	1V	1V	0.5 V
$\overline{\text{Pout}}$	0.52 μW	5 μW	13.1 μW	1.1 μW
PCE DC-DC	35.13%	50%	80%	86%
PCE RF-DC	0.87% @-12.26 dBm	52% @-15 dBm	13% @-10 dBm	41% @-25 dBm

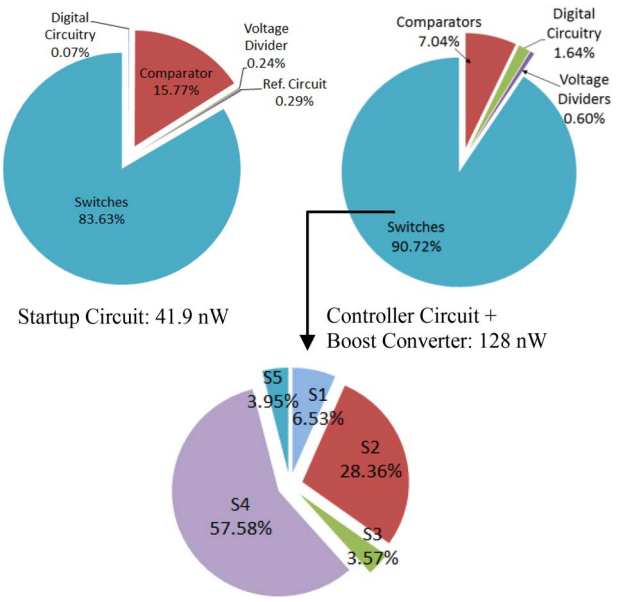

FIGURE 20. **Distribution of power losses in the PMC for RF Pav= -25 dBm. L1=10 mH, Cboost=0.05 μF, Cout=0.05 μF, Csnub=2 nF, Rload=166.7 kΩ, WS1=10 μm, WS2,3,5=100 μm, WS4=25 μm.**

VI. CONCLUSION

When compared to Si FinFETs, the better switching performance of TFETs at sub-0.25 V allows for an efficient rectification at received RF power levels below −20 dBm. It is shown by simulations that at -25 dBm of available RF power, a TFET-based PMC can boost the output voltage

of the rectifier (140 mV) to 500 mV with high efficiency. A TFET-based startup, controller circuit and boost converter are designed with power consumption values of 41.9 nW, 11.88 nW and 116 nW respectively. These values allow the design of an efficient energy-harvesting system, showing high conversion efficiencies at input power levels in the μW range.

Reverse current in reverse biased TFETs present a challenge in the design of TFET-based boost converters when compared to conventional thermionic technologies. Boost converters with larger output values require larger peak inductor currents to counteract the reverse current conducted by the TFET output transistor.

The reduction of the V_{GS} magnitude in reverse biased TFETs (intrinsic *p-i-n* diode forward biased) is shown as a good practice to attenuate the reverse power losses in TFET-based circuits. In order to increase the RF-powered system efficiency, the proposed PMC circuit imposes V_{GS}=0V for all the TFETs under reverse bias.

Although the presented results do not include pad connection losses and parasitics, the improved switching performance shown by the TFET models when compared to similar device models of thermionic transistors demonstrate the potential of using III-V TFET devices in RF energy harvesting applications at μW power levels.

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