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High-Temperature Bipolar-Mode Operation of Normally-Off Diamond JFET

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ABSTRACT High temperature characteristics of bipolar-mode operation of normally-off diamond junction field-effect transistors were investigated up to 573 K. As an important factor, the current gain depending on the gate current was analyzed with a theoretical model. We found that the experimental current gain decreased with the rise in the gate current, in agreement with the theoretical estimation considering the recombination at the end regions. We achieved 4–9 times higher drain currents in the bipolar-mode compared with the unipolar-mode operation at a DC current gain of 10. Furthermore, the bipolar-mode currents at the high temperatures of 473 and 573 K became two orders of magnitude larger than the unipolar-mode current at room temperature with a large DC current gain of 10^2.

INDEX TERMS Diamond, JFET, bipolar-mode operation, normally-off, high temperature.

I. INTRODUCTION

Diamond semiconductor is a promising material for next-generation low-loss power devices due to its wide band-gap, high breakdown field, and high thermal conductivity [1]. We have reported the fabrication of diamond junction field-effect transistors (JFETs) with selectively grown n^+-side gates [2], which can be operated at high temperatures up to 723 K [4] and at high voltages about 600 V [5]. However, the on-current is limited by the low activation of the boron acceptors in the p-type diamond. Especially, this problem is crucial for normally-off devices with lower doping concentrations and/or narrower channel widths [5], resulting in the significant reduction of the drain current. Recently, to increase the drain current, we have demonstrated current enhancement by bipolar-mode operation of diamond JFETs [6], in which the amount of the carriers in the p-channel was enhanced, and thus, the drain current increased compared with the unipolar-mode. Although this operation mode was also observed in devices based on other materials such as Si [7]–[9], 4H-SiC [10], and GaN [11], it is of special importance for diamond with the deep impurity levels.

Since power devices are required to work at high temperatures, investigation of the bipolar-mode characteristics over room temperature is essential. In this study, we report high temperature characteristics of the bipolar-mode operation in normally-off diamond JFET up to 573 K, and the device operation is analyzed by comparing with a theoretical model.

II. EXPERIMENTAL

Fig. 1 illustrates the device structure of the normally-off diamond JFET. The device consists of a boron-doped p-type channel, which is sandwiched by two n^+-gates fabricated by the selective growth method [12]. A high phosphorus concentration of 8×10^{19} cm^{-3} was obtained by promoting the growth of the (111) faces which efficiently incorporate impurities into the diamond lattice [13]. A boron concentration of about 3×10^{16} cm^{-3} and a channel width of 0.5 μm led to the normally-off operation. We formed p^+-contact layers with a boron concentration of $\sim 5 \times 10^{20}$ cm^{-3} below source and drain electrodes. Thus, from the source to the gates, the device consists of p^+-p-n^+ diodes which enhance the bipolar-mode operation. The profile of the boron concentration measured by secondary ion mass spectrometry (SIMS) is shown in Fig. 1c. The thickness of the p-channel and p^+-contact layer is about 1 μm and 0.15 μm, respectively. The contact electrodes consist of Ti/Pt/Au, fabricated by electron-beam evaporation.

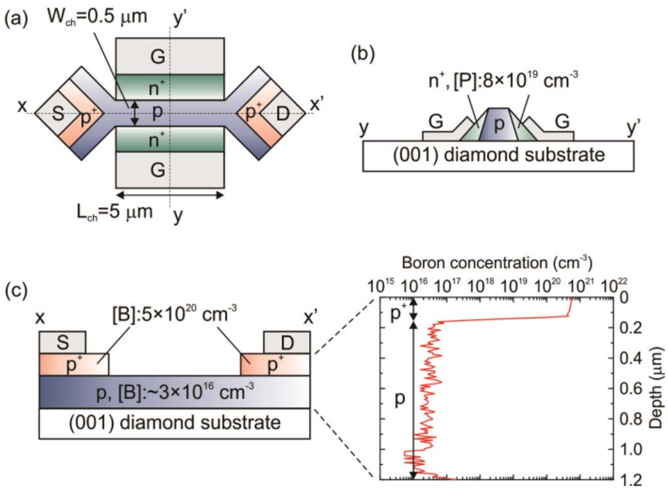

FIGURE 1. Structure of normally-off diamond JFET with p^+-contact layers. (a) Top-view and (b), (c) cross-sectional images along the dashed lines in the top-view. A SIMS profile of boron acceptors is also shown.

III. RESULTS AND DISCUSSION

First, we confirmed the normally-off operation of the fabricated diamond JFET with varying the temperature. Fig. 2a shows transfer curves of the diamond JFET from 300 to 573 K with the each gate current. The leakage currents are kept very low even at the high temperatures. The on-current increases as the temperature rises due to the activation of the boron acceptors [4]. The activation energy of the drain current is calculated to be around 2 eV. At high temperatures, the hole concentration is proportional to exp(-E_A/2kT), where E_A is the boron acceptor level (∼0.37 eV), k is the Boltzmann constant, and T is the temperature [14]. The obtained activation energy of 2 eV is in good agreement with the half of the boron acceptor level. Thus, the acceptor activation causes the increase in the on-current. At room temperature, the device works in the normally-off operation with a threshold voltage (V_{th}) of −1.2 V. The normally-off operation can be maintained even at 573 K.

The device works in the unipolar-mode before the gate diodes turn on in Fig. 2a. After the diodes turn on, the gate current flows, for example at a gate voltage over -3.5 V at 473 K, leading to the increase of the drain current by the bipolar-mode operation. In Fig. 2b, we can clearly see the rise in the drain current in the bipolar-mode compared with the unipolar-mode operation. With the flow of the gate current, the concentration of both the majority (holes) and minority (electrons) carriers in the p-channel increases. By extracting the enhanced holes to the drain contact, we obtain the enhancement of the drain current compared with the unipolar-mode operation.

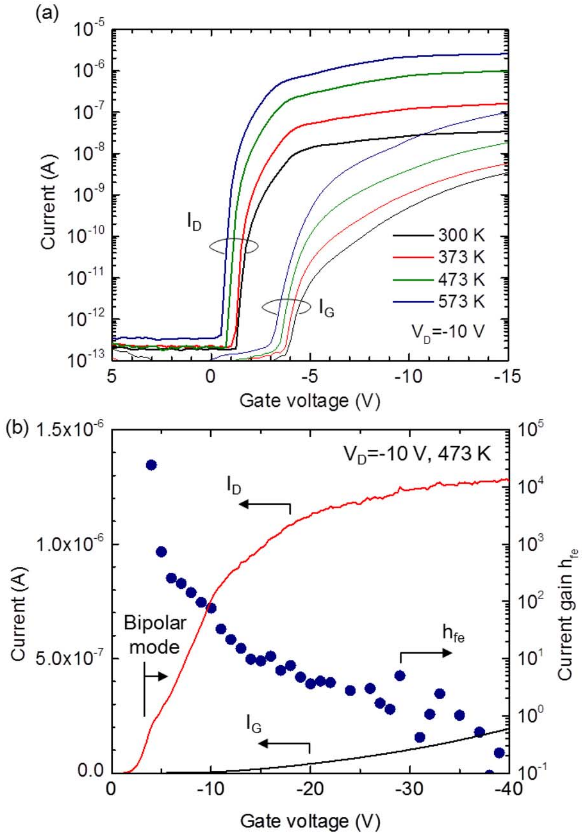

FIGURE 2. Transfer characteristics of normally-off diamond JFET. (a) Log-scale plots from 300 to 573 K. The gate currents are also shown. (b) Linear-scale plots and current gain h_{fe} at 473 K. Here, h_{fe} was calculated with a gate voltage step of 1 V.

The current gain $h_{fe} = \Delta I_D/\Delta I_G$ is an important factor for the bipolar-mode operation. The drain current keeps increasing with the gate current, while h_{fe} continuously decreases with a rise in the gate voltage (Fig. 2b). To analyze the decrease of the current gain, the relation of h_{fe} and I_G is plotted in Fig. 3. At the low gate currents, h_{fe} is higher than 10^3, but it continues to decrease with the gate current at all the temperatures. We compare this behavior with a theoretical model. With considering recombination at the ends (p^+-source and n^+-gate regions) at the high injection level, the gate current is giving by [7], [15]

$$I_G = \left(\frac{p_1}{n_{ip^+}}\right)^2 I_{sp^+} + \frac{q\overline{p}W_{ch}S_G}{\tau_{HL}} + \left(\frac{p_2}{n_{in^+}}\right)^2 I_{sn^+} \quad (1)$$

where p_1 (p_2) is the hole concentration at the p^+-p (n^+-p) junction. n_{ip^+}(n_{in^+}) is the effective intrinsic carrier concentration in the p^+ (n^+) regions. $\overline{p}$ is the average concentration in the p-layer. S_G is the gate area. τ_{HL} is the lifetime in the p-layer at the high level injection. q is the elementary charge. I_{sp^+} (I_{sn^+}) is the saturation current in the p^+ (n^+) region. The first and third terms in the right side of the equation (1) represent the recombination currents at the p^+

and n^+ regions, respectively. The middle term denotes the recombination in the p-channel. If the second term is negligible compared with the other two terms, h_{fe} is expressed as follows with assuming the homogeneous carrier distribution in the p-layer, i.e., $\bar{p}=p_1=p_2$ [7],

$$h_{\mathrm{fe}} = \frac{dI_D}{dI_G} \propto \frac{d\bar{p}}{dI_G} = \frac{1}{2\sqrt{I_G\left[\frac{I_{sp^+}}{\left(n_{ip^+}\right)^2} + \frac{I_{sn^+}}{\left(n_{in^+}\right)^2}\right]}} \quad (2)$$

h_{fe} is proportional to $I_G^{-1/2}$ irrespective of the temperature, which is shown as a dashed line in Fig. 3. The experimental values, especially at 473 and 573 K, follow this theoretical relationship. Thus, the recombination at the end regions strongly influences the behavior of h_{fe} in our device.

Next, we plot the DC current gain (I_D/I_G) against the gate current (Fig. 4). The DC gains also decrease with increasing the gate current. A DC current gain of 10 is obtained even at a high gate current, e.g., $I_G=1.2\times10^{-7}$ A at 473 K. Although h_{fe} goes down to the unity in this region as shown in Fig. 3, the high DC current gain can be maintained. It is worth noting that a slight difference in the slope of the current gains compared with the model (proportional to $I_G^{-1/2}$, eq (2) and [7], [8]) would be caused by the recombination of the carriers before the extraction at the drain contact. In addition, the rapid drops are observed at a higher gate current, for example, at $I_G=4\times10^{-9}$ A at 473 K. This is because the holes injected from the source preferentially flow to the gates rather than the drain at the high forward voltage of the gate diodes.

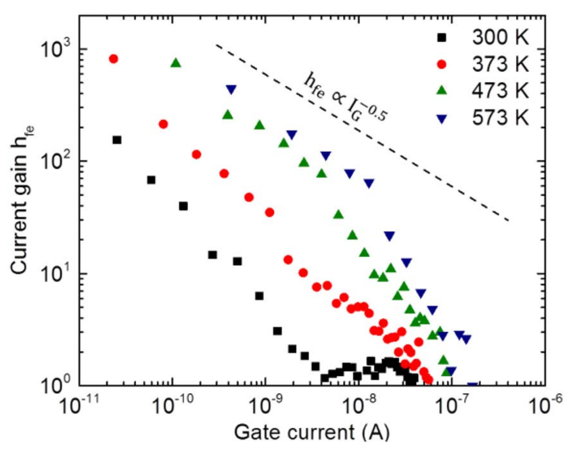

FIGURE 3. Dependence of the current gain on the gate current. The dashed line denotes the slope of the theoretical model described in the main text.

The current densities in the unipolar- and bipolar-modes are summarized in Fig. 5. Here, the drain currents were normalized with the channel cross-section. The bipolar-mode current was obtained at DC current gains of 10, 10^2, and 10^3 in Fig. 4. The bipolar-mode current rises with the temperature as well as the unipolar-mode current. At a DC current gain of 10, the bipolar-mode current increases from 6 A/cm^2 at 300 K to 458 A/cm^2 at 573 K. At 300 K, the bipolar-mode

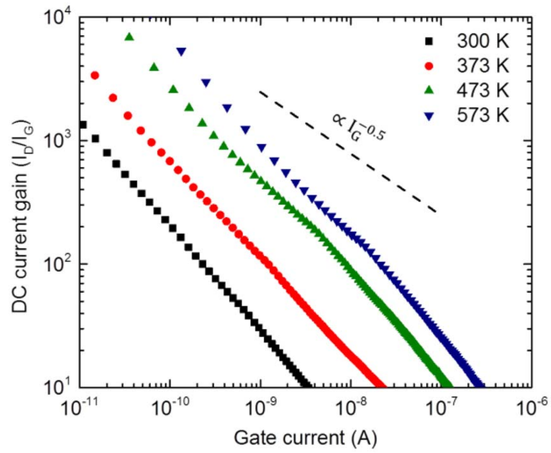

FIGURE 4. Dependence of the DC current gain (I_D/I_G) on the gate current.

current is 4 times higher than the unipolar-mode. Importantly, we obtained a high current enhancement over 8 even at 573 K. Compared with the unipolar-mode at 300 K, the current density in the bipolar-mode at 473 K becomes 110-160 times higher with the DC current gains of 10-10^2. Thus, the combined operation of the bipolar-mode and high-temperature is expected to lead to the construction of very low-loss power electronics.

It has been reported that the bipolar-mode drain current increases by a factor of 100 in Si JFET, compared with the unipolar-mode [7]. To quantitatively examine the theoretical model and estimate the maximum performance of the bipolar-mode diamond JFET, measurements of physical parameters such as carrier lifetime and diffusion coefficient are required. It is expected that such parameters for different doping types and concentrations will be revealed for the further device analysis and fabrications.

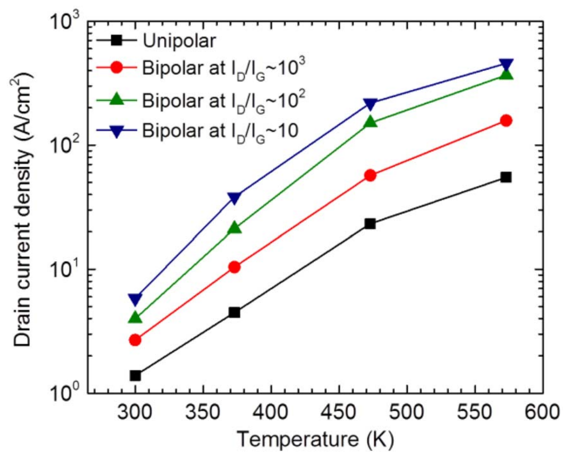

FIGURE 5. Drain currents in the unipolar- and bipolar-modes at various DC current gains (I_D/I_G) from 300 to 573 K.

IV. CONCLUSION

We fabricated the normally-off diamond JFET with a threshold voltage of -1.2 V. We confirmed that the normally-off operation was maintained even at 573 K. The bipolar-mode operation led to the increase of the drain current by a factor of 4-9 compared with the unipolar-mode from 300 to 573 K at a DC current gain of 10. By analyzing the current gain, we found that the reduction tendency of h_{fe} depending on the gate current was in agreement with the theoretical model based on the recombination at the p^+- and n^+-end regions.

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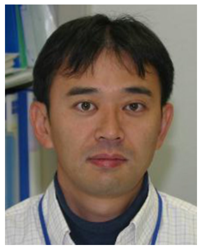

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