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Lithium-Intercalated Graphene Interconnects: Prospects for On-Chip Applications

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ABSTRACT This paper establishes the importance of the lithium (Li) intercalation in multilayer graphene nanoribbon (MLGNR) interconnects for obtaining superior performance than conventional copper (Cu) on-chip interconnects. For the first time, we report performance analysis of Li-intercalated MLGNRs for local interconnect applications. In that, interconnect thickness is optimized for obtaining lowest delay and energy-delay-product (EDP). At 12 μm interconnect length, our optimized Li-intercalated MLGNRs exhibit ($\approx$ 22.9 ps)1.9$\times$ and 4.1$\times$ lower delay and EDP, respectively, when compared to Cu. Even in presence of edge roughness, they exhibit ($\approx$ 31.8 ps)1.37$\times$ and 2.5$\times$ lower delay and EDP, respectively, when compared to Cu. Our analysis quantitatively proves the potential of Li-intercalated MLGNRs for local interconnect applications.

INDEX TERMS Delay, EDP, interconnects, intercalation, MLGNRs.

I. INTRODUCTION

Interconnect performance has become the main bottleneck in modern integrated circuits due to limitations of lower speed and higher power consumption. For lower technology nodes, the interconnect delay dominates the transistor delay while parasitic capacitance associated with interconnects leads to more than 50% of the total power consumption in modern ICs [1]–[3]. Currently, Copper (*Cu*) is the industry preferred interconnect material. However, due to various width dependent scattering mechanisms, *Cu* resistivity increases excessively. This happens largely due to size-effects as physical dimensions decrease beyond the mean free path of $Cu(\lambda_{Cu} \sim 40nm)$. As per the International Technology Roadmap for Semiconductors (ITRS) prediction, it will reach 16 $\mu\Omega.cm$ for local interconnect applications, at the end of the roadmap [4]. This necessitates the need for novel materials that can be used for next generation on-chip interconnects. In the recent past, Graphene has shown promising ability to exceed the performance of *Cu* interconnects [5]. Chen *et al.* [6] have shown the monolithic integration of Graphene with CMOS using conventional fabrication processes. High-frequency operation in Graphene strips with lengths as long as 80 μm has been observed, thereby promising future Graphene-based local and semi-global high-speed interconnects.

Due to higher resistance of single layer Graphene Nanoribbons (GNRs), a structure of multiple layers of GNRs stacked over each other, called multilayer GNRs (MLGNRs), is preferred. Based on their connection with surrounding devices and other interconnects, MLGNRs are classified as top contact MLGNRs (TC-MLGNRs) and side contact MLGNRs (SC-MLGNRs) [7]. All the GNR layers are physically connected to the contacts in case of SC-MLGNRs, which results in significant reduction in their effective resistance. On the other hand, in case of TC-MLGNRs, only topmost layer is physically connected to the contacts resulting in inferior performance as compared to that of SC-MLGNRs. However, fabrication of TC-MLGNRs is easier, while that of SC-MLGNRs is very difficult and has not yet been reported. Therefore, there is a need to improve and optimize the performance of TC-MLGNRs for practical applications. Due to technology scaling, interconnect width shrinks, which lowers the number of conduction channels and MFP in each GNR layer, thereby increasing the effective resistance of TC-MLGNRs. In other words, reduction in both in-plane and *c*-axis resistance of TC-MLGNRs is needed for better interconnect performance. Patterning graphene into narrow ribbons leads to edge roughness due to immature fabrication technology. The electron MFP further reduces significantly due to enhanced scatterings at the

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GNR edges [5], [8]. This is a one of the major drawbacks of GNRs and needs to be overcome before GNRs can be used for commercial applications. This happens to be the central theme of this present work.

Intercalation doping is a promising technique that can improve both the in-plane and *c*-axis resistances. Xu *et al.* [9] have proposed Arsenic Pentafluoride (*AsF5*) intercalation in MLGNRs and have observed significant improvements in MFP and Fermi level. In [10], Lithium (*Li*) intercalated ultrathin graphite structure is fabricated and improved in-plane conductivity and Fermi level have been experimentally observed. However, the effect of *AsF5* or *Li*-intercalation on practically possible TC-MLGNR interconnects has not been reported yet. In addition, performance comparison between these two intercalated interconnects is also needed to determine the potential candidate that can replace *Cu* for local interconnect applications.

In this paper, performance analysis of *Li*- and *AsF5*-intercalated TC-MLGNR interconnects with effect of edge roughness is presented and compared with pristine (undoped) TC-MLGNRs and *Cu* interconnects. For our analysis, typical performance metrics such as delay and energy-delay-product (EDP) are considered. Further, the interconnect thickness of *AsF5*- and *Li*-intercalated TC-MLGNRs has been optimized to obtain the lowest delay and EDP. In our analysis, it is found that even with presence of edge roughness, our optimized *Li*-intercalated TC-MLGNR is the fastest interconnect and exhibits lowest EDP among all configurations, irrespective of the practical lengths for local interconnects. At interconnect lengths of 100 gate pitch, our optimized *Li*-intercalated MLGNRs in presence of edge roughness, exhibit 1.37× and 2.5× lower delay and EDP as compared to *Cu* interconnects, respectively.

In the remainder of this paper; in Section II, a driver-interconnect-load (DIL) system is used to evaluate key performance matrices such as delay and EDP. Performance of pristine, *AsF5*-intercalated, *Li*-intercalated TC-MLGNRs and *Cu* interconnects are compared in Section III. Important findings are summarized in Section IV.

II. EQUIVALENT DRIVER INTERCONNECT LOAD SYSTEM

Fig. 1(a) represents a 3-line structure having three adjacent TC-MLGNR interconnect lines of width, *w*, height from ground, *h'*, thickness, *t*, and spacing, *s*. All interconnect dimensions are taken from ITRS and technology year 2026 has been considered for delay and EDP analysis in our paper. Fig. 1(b) shows the driver-interconnect-load system used to evaluate the performance of TC-MLGNR interconnects. The quantum resistance is taken as 12.9 $k\Omega$ per channel. The additional contact resistance R_{c1} and R_{c2} is assumed to be 4.3 $k\Omega$ per conduction channel. r, l_K, l_M, c_Q and c_E are the equivalent resistance, kinetic inductance, magnetic inductance, quantum capacitance and electrostatic capacitance per unit length of TC-MLGNR, respectively. The total number of GNR layers in TC-MLGNR interconnects is given by $N = Integ(t/\delta) + 1$, where δ represent average interlayer spacing. The driver resistance and capacitance, R_S and C_S, are 41 $k\Omega$ and 3.5 aF, respectively, which are considered to be equal to that of minimum size transistors. Table 1 summarizes experimental values for major TC-MLGNR properties.

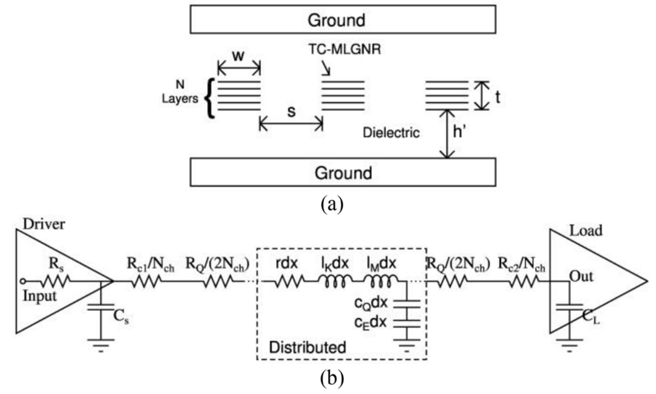

FIGURE 1. (a) Cross-section of TC-MLGNR interconnects embedded in a dielectric. $w = 6$ *nm*, $s = 6$ *nm*, $t = 13.2$ *nm* and $h' = 13.2$ *nm*. The dielectric constant is 1.87. (b) Driver-Interconnect-Load system. Power supply V_{DD} is taken as 0.57 V.

TABLE 1. Different properties of TC-MLGNRs [5], [9]–[12].

Properties	Pristine	AsF5-intercalated	*Li*-intercalated
In-plane conductivity $(\mu\Omega.cm)^{-1}$	0.026	0.63	$\frac{1}{3.1}$
c-axis conductivity $(\Omega.cm)^{-1}$	$\frac{1}{30}$	0.24	1.8×10^4
δ (nm)	0.34	0.575	0.37
E_F (eV)	0.2	0.6	1.5

The equivalent *p.u.l.* resistance, *r*, is calculated from [5]. The effective resistance of TC-MLGNR interconnect can be easily calculated using an accurate mathematical model that has been proposed by Kumar *et al.* [5], which is given by:

$$R_{eff} = \sum_{m=1}^{m=M} \sum_{m=1}^{m=M} [A_{11}] \left(\frac{[A_{11}]}{R_b} - [A_{21}] \right)^{-1} \tag{1}$$

where, $[A_{11}]$, $[A_{21}]$ matrices are of size $M \times M$, and depends on R_a and R_b. M represents the number of partitions along the interconnect length. R_a is the *c*-axis resistance, while R_b represent the distributed in-plane resistance, respectively. R_a and R_b can be calculated as:

$$R_a = \frac{\rho_c \delta}{w \triangle z} \tag{2}$$

$$R_b = \frac{R_Q \triangle z}{N_{ch} \lambda_{eff}} \tag{3}$$

where Δz is the differential element along the interconnect length. R_Q is the quantum resistance. In that, the distributed in-plane resistance, R_b, depends on the number of conduction channel, N_{ch}, and effective mean free path, λ_{eff}, of GNR layer, while the distributed perpendicular resistance,

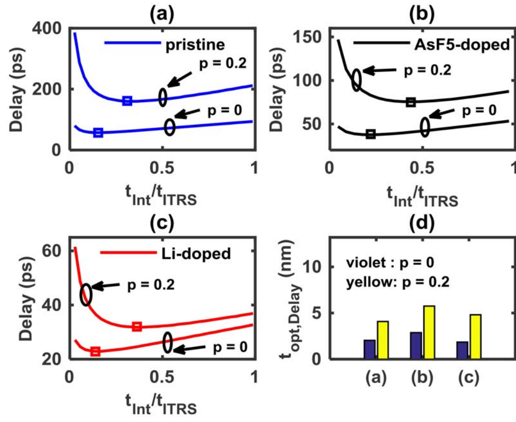

FIGURE 2. **Delay variation w.r.t. interconnect thickness for (a) pristine (b) *AsF5*-intercalated and (c) *Li*-intercalated MLGNRs. In (d), optimum interconnect thickness, t_{opt} is analyzed for (a) pristine, (b) *AsF5*-intercalated, and (c) *Li*-intercalated MLGNR interconnects at 100 gate pitch interconnect length. The analysis is done considering perfectly smooth edges ($p = 0$) and an edge-scattering probability of 20% ($p = 0.2$).**

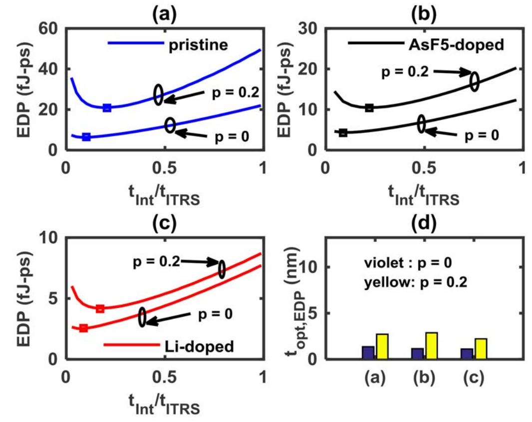

FIGURE 3. **EDP variation w.r.t. interconnect thickness for (a) pristine (b) *AsF5*-intercalated and (c) *Li*-intercalated MLGNRs. In (d), optimum interconnect thickness,t_{opt} is analyzed for (a) pristine, (b) *AsF5*-intercalated, and (c) *Li*-intercalated MLGNR interconnects at 100 gate pitch interconnect length. The analysis is done considering perfectly smooth edges ($p = 0$) and an edge-scattering probability of 20% ($p = 0.2$).**

R_a, between the GNR layers depends on c-axis resistivity, ρ_c, and interlayer spacing, δ. N_{ch} in GNRs is the function of Fermi level, E_F, and interconnect width, w [12]. The effective MFP of each GNR layer in TC-MLGNRs limited due to scattering from the edges and from substrate-induced scattering can be obtained using simple formulation reported in [5] and [8]. In that, the substrate-limited MFP, λ_{sub}, is taken as 300 *nm*. The electron MFP depends on subband index, m, interconnect width, w, and edge-scattering coefficient in GNR, p, where value of p is reported between 0.2 and 1 in [13] and [14]. Here, 0.2 represents least value of practically possible edge roughness while 1 means highly diffusive edges. l_K and c_Q are obtained from [9] and given as:

$$l_K = \frac{h/4e^2 v_F}{NN_{ch}} \quad (4)$$

$$c_Q = \frac{4e^2}{hv_F} NN_{ch} \quad (5)$$

where, e is electronic charge, h is Plank's constant. N represent the number of GNR layers. $v_F = (8 \times 10^5\ m/s)$ is the Fermi velocity. The c_E and l_M has been computed using *Synopsys Raphael*.

III. RESULTS AND DISCUSSION

In this section, delay and the EDP for various configurations of TC-MLGNR interconnects are evaluated and compared against those of *Cu*. Synopsys HSPICE is used to simulate the DIL system shown in Fig. 1(b).

Here, we have used 3-line interconnect systems. In HSPICE simulation setup, three DIL system is used to present 3-line interconnect system. The coupling capacitance and mutual inductance between interconnect lines, electrostatic capacitance and magnetic inductance of TC-MLGNR interconnects have been computed using *Synopsys Raphael*. Other required parameters are already defined in previous section. Based on these circuit parameters, delay has been computed using Synopsys HSPICE.

Fig. 2 gives the delay as a function of interconnect thickness for pristine, *AsF5*-intercalated and *Li*-intercalated TC-MLGNR interconnects. As the thickness of TC-MLGNR interconnects is increased, the effective resistance decreases, while the capacitance increases. Therefore, there is an optimal thickness where minimum delay and EDP occurs. Thicker interconnect leads to more number of GNR layers that provide more conduction path, thereby lesser resistance of that internconnect line. However, increasing GNR layers leads to higher sidewall capacitance. As shown in Fig. 2(d), the optimal thickness required for obtaining lowest delay in pristine, *AsF5*-intercalated and *Li*-intercalated TC-MLGNR interconnects is 2.04 *nm*, 2.875 *nm* and 1.85 *nm*, respectively for perfectly smooth edges while it is 4.08 *nm*, 5.75 *nm* and 4.81 *nm*, respectively for rough edges ($p = 0.2$) at 100 gate pitch lengths. These optimal thickness also exhibit lesser capacitance as compared to *Cu*. At these optimal thickness, capacitance ratio (c_{Cu}/c) is obtained as 2.059×, 1.893× and 2.06×, respectively for perfectly smooth edge while it is 1.724×, 1.521× and 1.614×, respectively for rough edges ($p = 0.2$) at 100 gate pitch lengths.

The energy dissipation of the system shown in Fig. 1(b) is given by $E = 0.5 \times (C_S + c.L + C_L)V_{DD}^2$, [5], where c, L and V_{DD} are *p.u.l.* equivalent capacitance, length and supply voltage, respectively of the TC-MLGNR interconnect. In Fig. 3, variation of EDP for all TC-MLGNR configurations is computed as a function of interconnect thickness. Fig. 3(d) shows the optimal thickness required for obtaining least EDP for pristine, *AsF5*-intercalated and *Li*-intercalated TC-MLGNR interconnect are 1.36 *nm*, 1.15 *nm* and 1.11 *nm*, respectively for perfectly smooth edges while 2.72 *nm*, 2.875 *nm*

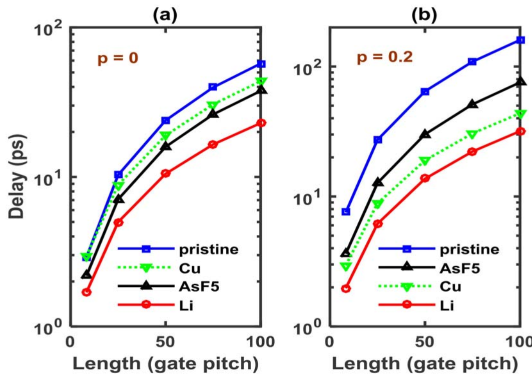

FIGURE 4. Variation of delay w.r.t. interconnect length for pristine, *AsF5*-intercalated, *Li*-intercalated TC-MLGNRs and *Cu*. Interconnect thickness, $t = t_{opt}$ is considered for TC-MLGNRs. The analysis is done considering perfectly smooth edges ($p = 0$) and an edge-scattering probability of 20% ($p = 0.2$).

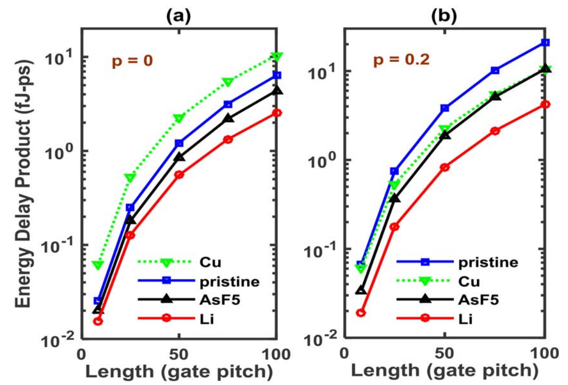

FIGURE 5. Variation of EDP w.r.t. interconnect length for pristine, *AsF5*-intercalated, *Li*-intercalated TC-MLGNRs and *Cu*. Interconnect thickness, $t = t_{opt}$ is considered for TC-MLGNRs. The analysis is done considering perfectly smooth edges ($p = 0$) and an edge-scattering probability of 20% ($p = 0.2$).

and 2.22 *nm*, respectively for rough edges ($p = 0.2$) at 100 gate pitch interconnect length. At these optimal thickness, capacitance (c_{Cu}/c) is obtained as 2.217×, 2.251× and 2.226×, respectively for perfectly smooth edge while it is 1.929×, 1.893× and 1.988×, respectively for rough edges ($p = 0.2$) lesser capacitance as compared to *Cu* at 100 gate pitch lengths. From Figs. 2 and 3, it can be concluded that the optimal thickness to minimize delay in TC-MLGNRs is greater than that needed to minimize EDP for all other cases. This is due to stronger impact of interconnect capacitance on EDP than on the delay.

Further, the delay and EDP of pristine, *AsF5*-intercalated and *Li*-intercalated TC-MLGNRs *w.r.t. Cu* interconnects is compared in Figs. 4 and 5, respectively. In that, respective optimal thickness is computed at each interconnect length for delay and EDP evaluation. Note that the delay of pristine TC-MLGNRs ($p = 0$ or 0.2) is worse than *Cu*. EDP of pristine TC-MLGNRs with perfectly smooth edges is lesser than Cu while it worsens in presence of edge roughness. In case of *AsF5*-intercalated TC-MLGNRs, lesser delay and EDP is achieved with consideration of perfectly smooth edges. In presence of edge roughness, its delay becomes worse while it exhibits similar EDP as compared to Cu. However, *Li*-intercalated TC-MLGNR interconnects ($p = 0$ and 0.2) show best performance in terms of both delay and EDP for all interconnect lengths when compared with *Cu*. At 100 gate pitch interconnect length, *Li*-intercalated TC-MLGNRs with ($p = 0$) exhibit 47.57% and with ($p = 0.2$) exhibit 27.2% lower delay while 75.7% and 59.6% lesser EDP for *Li*-intercalated MLGNR with ($p = 0$) and with ($p = 0.2$), respectively as compared to *Cu*. Significant increase in conductivity in intercalated MLGNRs results from injection of carrier from the intercalate layer, where the carriers have a lower mobility, to the GNR layers, where the mobility usually is high. This leads to an upward shift in Fermi level. Moreover, intercalation increases interlayer spacing that leads to higher MFP due to lower scattering phenomena. Our present analysis proves the potential benefits of *Li*-intercalated TC-MLGNRs for local interconnect applications.

IV. CONCLUSION

This paper analyzes the performance of *Li*-intercalated TC-MLGNRs as a potential candidate to replace *Cu* as local interconnects for advanced technology nodes. *Li*-intercalation improves both the Fermi-level and *c*-axis conductivity in TC-MLGNRs. Using a driver interconnect load system, various performance matrices, such as delay and EDP, are analyzed. The effect of edge roughness in *Li*-intercalated TC-MLGNRs is also considered in analysis for realistic comparison with *Cu* interconnects. The interconnect thickness of *Li*-intercalated TC-MLGNRs has been optimized to obtain lowest delay and EDP when compared with pristine, *AsF5*-intercalated and *Cu* interconnects for practical interconnect lengths.

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