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Characterization of RF Noise in UTBB FD-SOI MOSFET

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ABSTRACT In this paper, we report the noise measurements in the RF frequency range for ultrathin body and thin buried oxide fully depleted silicon on insulator (FD-SOI) transistors. We analyze the impact of back and front gate biases on the various noise parameters; along with discussions on the secondary effects in FD-SOI transistors which contribute to the thermal noise. Using calibrated TCAD simulations, we show that the noise figure changes with the substrate doping and buried oxide thickness.

INDEX TERMS Thermal noise, high frequency noise, device modeling, RF, FDSOI, MOSFET, electrical characterization.

I. INTRODUCTION

Ultra-thin body fully depleted (FD) silicon on insulator (SOI) transistors are being used at 28 nm and below due to their excellent electrostatic control [1]–[9]. Apart from digital applications, FD-SOI transistors are also getting a strong interest from RF circuit designers for high frequency applications [10], [11]. At RF frequencies, thermal noise becomes an important factor in design of circuits as it decides the noise floor for the signal. It is well known that thermal noise is a function of the temperature and the conductivity of the channel. FD-SOI transistors have higher thermal noise compared to bulk transistors due to high lattice temperature originating from poor thermal conductivity of the buried oxide (BOX) [12]. Hence, careful analysis and measurements of thermal noise in such devices is of utmost importance. Although RF noise characterization for thick BOX FD-SOI transistors has been presented [13]–[15]; there is no work reporting the same for thin BOX FDSOI transistors. In this work, we report the measured data for an FD-SOI transistor with 8 nm thin channel and 25 nm thin BOX, and discuss the impact of the drain and the front/back gate biases on the high frequency noise. Fig. 1 shows the UTBB FD-SOI structure used in this study. The dependence of noise on the back gate bias is especially important as the back gate bias is often used to tune the threshold voltage (V_{th}) in these devices. Also, the substrate below the thin BOX plays an important role at RF frequencies and shows significant impact on the thermal noise. Hence, we also present an analysis of the impact of substrate resistivity and BOX thickness on the thermal noise.

This paper is organized as follows: the measurement setup is described in Section II while the thermal noise and related parameters are defined and discussed in Section III. The secondary effects inherent with FDSOI transistors are discussed in Section IV and the results are presented in Section V. Finally, the conclusions are drawn in Section VI.

II. MEASUREMENT SETUP

Fig. 2 shows the noise measurement setup used in this work. It includes a vector network analyzer, a noise figure meter (NFM) to measure noise power, a source-pull tuner to vary the impedance seen by the DUT and a noise source. The measurement setup is controlled by Keysight's IC-CAP tool. The low noise amplifier (LNA) is used before the NFM to boost the weak noise signal, which increases the accuracy of the measurement [16]. In this work, we have measured the

Noise figure (defined later) keeping a fixed source impedance of 50 Ω. The DUTs belongs to the 28 nm technology node from CEA-LETI. We have performed the measurements on two channel lengths ($L_g = 50$ nm and 100 nm). Other device dimensions are: channel width $W_g = 1\mu$m, number of fingers NF = 40, effective oxide thickness $T_{ox} = 1.2$ nm, back gate oxide thickness $T_{box} = 25$ nm and silicon channel thickness $T_{si} = 8$ nm.

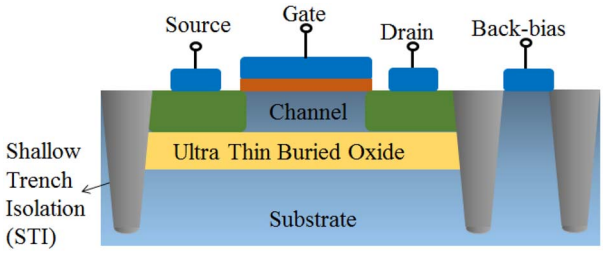

FIGURE 1. Schematic of ultra thin body and thin buried oxide fully depleted silicon on insulator (UTBB FD-SOI) transistor. The Device under test (DUT) is from 28 nm technology node fabricated at CEA-LETI.

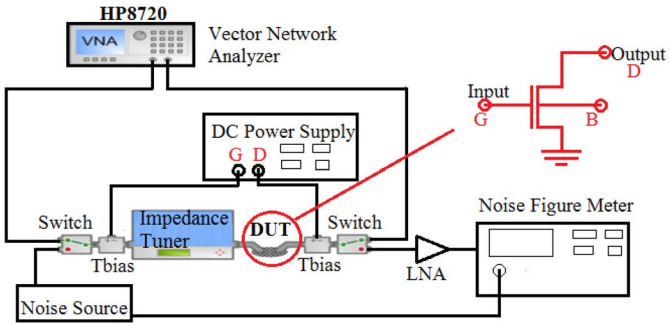

FIGURE 2. RF Noise Figure Measurement Setup. A separate DC power supply (not shown here) is used for applying back-gate bias through substrate.

III. THERMAL NOISE AND RELATED PARAMETERS

Since noise is a random event with zero average, it is measured and analyzed by means of specific parameters that highlight the device behavior accurately. One such parameter is the Noise figure (NF), which is the ratio of the signal to noise ratio at the input port to that at the output port. NF_{50} denotes the Noise Figure measurement performed with a source impedance of 50 Ω (see (1)), and NF_{min} denotes the minimum achievable noise figure (see (2)) for a device under fixed bias conditions. NF_{min} and NF_{50} are given as [17]

$$NF_{50} = 1 + R_n G_s + \left(\frac{f}{f_T}\right)^2 \frac{S_{id}^2}{16 k_B^2 T^2 g_m^2 R_n G_s} \tag{1}$$

$$NF_{min} = 1 + 2\Bigg[\left(\omega C_{gg}\right)^2 R_{gs}\left(R_n - R_{gs} + r - r\left(R_{gs}\omega C_{gs}\right)^2\right) + \omega C_{gg}\left(R_n\left(R_n - R_{gs} + r - r\left(R_{gs}\omega C_{gs}\right)^2\right) - \left(R_n - R_{gs} - r\left(R_{gs}\omega C_{gs}\right)^2\right)^2\right)^{1/2}\Bigg] \tag{2}$$

where $G_s = (1/50)\,\Omega^{-1}$ is the source admittance, k_B is the Boltzmann constant, T is the temperature, S_{id} is the noise power spectral density and $r = \frac{4}{15 g_m}$ with g_m denoting the trans-conductance. $R_{gs} = R_g + R_s$, where R_g and R_s are the gate and the source resistances, respectively. Gate capacitance $C_{gg} = C_{gs} + C_{gd}$, where C_{gs} is the gate-to-source capacitance and C_{gd} is the gate-to-drain capacitance; while $\omega(= 2\pi f)$ is the frequency of operation in rad/second and f_T is the cutoff frequency. It should be noted that the equations presented here for NF_{50} and NF_{min} do not take the induced gate noise into account because it is not as significant as the channel thermal noise for the frequency range under consideration [16]. The noise resistance (R_n) is an effective representation of the channel thermal noise which is extracted from NF_{50} as [17]

$$R_n = \frac{(NF_{50} - 1) - \left(\omega C_{gg}\right)^2\left(r - R_{gs} - r\left(R_{gs}\omega C_{gs}\right)^2\right)R_A}{\left(\omega C_{gg}\right)^2\left(2R_{gs} + \frac{1}{G_s}\right) + G_s} \tag{3}$$

where $R_A = (2R_{gs} + \frac{1}{G_s})$. Another important parameter is the source side reflection co-efficient, $\Gamma_{opt}(= \frac{Z_{opt} - Z_o}{Z_{opt} + Z_o})$. Z_o is the characteristic impedance of the system while $Z_{opt}(= \frac{1}{Y_{opt}})$ is the optimum source impedance and $Y_{opt}(= G_{opt} + \mathrm{j}B_{opt})$ is the optimum source admittance which results in minimum noise figure [16]. G_{opt} and B_{opt} are given as [16]

$$G_{opt} = \frac{\omega C_{gg}}{R_n}\left(R_n\left(R_n - R_{gs} + r - r\left(R_{gs}\omega C_{gs}\right)^2\right) - \left(R_n - R_{gs} - r\left(R_{gs}\omega C_{gs}\right)^2\right)^2\right)^{1/2} \tag{4}$$

$$B_{opt} = -\frac{\omega C_{gg}}{R_n}\left(R_n - R_{gs} - r\left(R_{gs}\omega C_{gs}\right)^2\right) \tag{5}$$

IV. SECONDARY NOISE SOURCES IN FD-SOI TRANSISTOR

FD-SOI transistors have secondary noise sources which get coupled with the channel thermal noise and result in higher NF_{min} than expected from the channel thermal noise alone. The majority carriers in the substrate also impact the device performance at high frequencies [18], as they dictate the substrate loss. The doping of the silicon substrate below the BOX plays a major role in increasing (or decreasing [19]) this substrate loss and the channel noise [20]. FDSOI transistors with the high substrate resistivity (or lightly doped substrate) are preferred for RF applications due to their high integration capabilities along with the advantages of lower noise and lower cross-talk [21], [22]. The depletion in the substrate and the substrate resistance act as extra noise sources (see Fig. 3). The substrate depletion and the substrate resistance R_{sub} induced thermal noises also contribute to the overall noise. Fig. 4(a) shows the calibration of current voltage characteristics from TCAD simulations against measured data for a transistor with $L_g = 100$ nm. Fig. 4(b) shows the NF_{min} vs. substrate doping obtained from calibrated TCAD simulations. We can see that NF_{min} changes with substrate

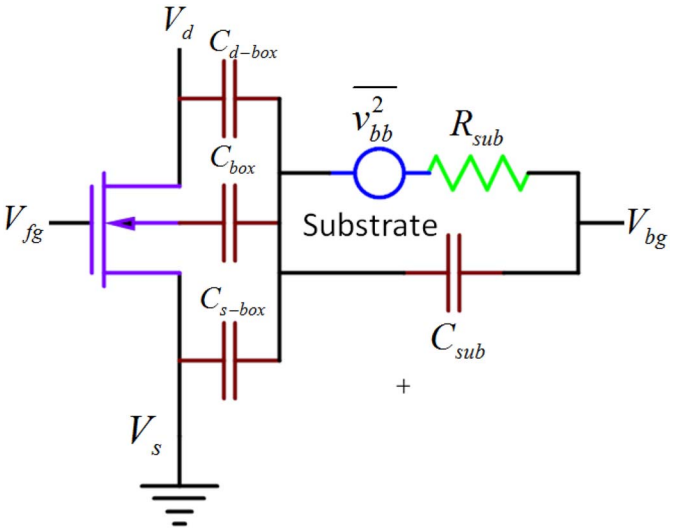

FIGURE 3. **Schematic of the substrate network showing substrate induced noise source in FDSOI transistor. R_{sub} is the equivalent substrate resistance while C_{sub} is the substrate capacitance. V_{fg}/V_{bg} are the applied front/back gate voltages and V_d/V_s are the drain/source voltages. The substrate coupling results in higher NF_{min} due to R_{sub} induced thermal noise at the drain [20].**

doping due to the substrate coupled thermal noise. Fig. 4(c) shows the NF_{min} variation with BOX thickness which indicates that as thickness decreases, the substrate coupling with the channel increases, resulting in increased thermal noise.

V. RESULTS AND DISCUSSION

Fig. 5 shows the frequency dependence of NF_{50} for different bias sweeps. The NF_{50} shown in Fig. 5(a) - Fig. 5(c) is more or less constant with frequency whereas (1) predicts a parabolic dependence [23], [24]. This is because the frequency dependent term, $(\frac{f}{f_T})^2 \frac{S_{id}^2}{16k_B^2T^2g_m^2R_nG_s}$, is smaller than $1 + R_nG_s$ for the measured device for the frequency range used here. Inset of Fig. 5(a) shows NF_{50} as a function of the front gate bias (V_{fg}). As V_{fg} increases, the total number of charge carriers in the device increases. This results in higher drain current and more carrier collisions in the channel which in turn increases the overall noise (i.e., higher NF_{min}) [25]. Fig. 4(a) shows that, with increase in positive back-gate bias (V_{bg}), the threshold voltage (V_{th}) decreases [26] which results in higher drain current and higher thermal noise. This increased thermal noise results in higher noise figure as shown in the inset of Fig. 5(b). To the best of our knowledge, the behavior of NF_{50} with changing back-gate bias for thin BOX FDSOI transistors is being reported for the first time. The inset of Fig. 5(c) shows that NF_{50} is nearly constant with drain bias (V_{ds}) as the noise does not change with V_{ds} in the saturation region due to the phenomenon of velocity saturation [27]. A similar trend has been reported by Adan *et al.* [28] for SOI MOSFETs.

It is well known that the accurate measurement of noise parameters is difficult (see measured data in Fig. 6(a) and Fig. 8(a)) for short channel devices [29]. Also, in our case, the channel width of the measured device is small, making measurements susceptible to other noise sources in the measurement setup. Hence, we have also measured the

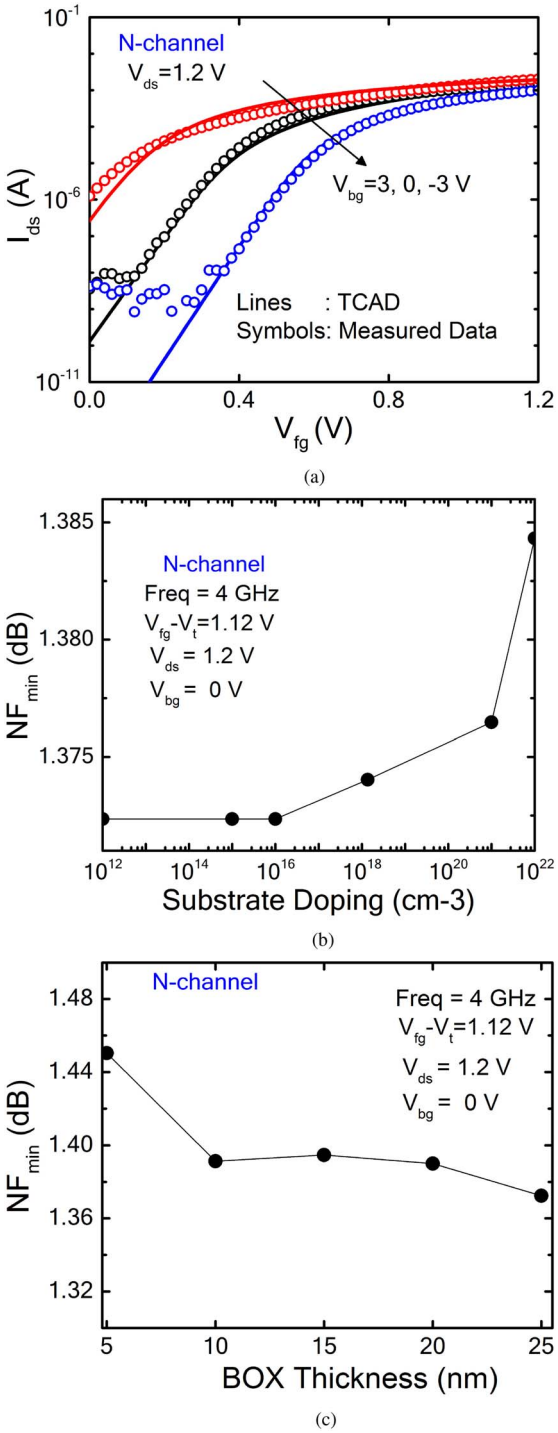

FIGURE 4. **(a) Drain current I_{ds} vs front gate bias V_{fg} characteristic for different back gate biases (V_{bg}) from the measurement as well as calibrated TCAD simulations. Lines: TCAD data, Symbols: Measured data. (b) NF_{min} vs substrate doping characteristic. The substrate depletion and the substrate resistance R_{sub} induced thermal noises also contribute to the overall noise, creating fluctuations in NF_{min}. (c) NF_{min} vs BOX thickness characteristic. NF_{min} increases further with BOX thinning due to an increase in the substrate coupled thermal noise.**

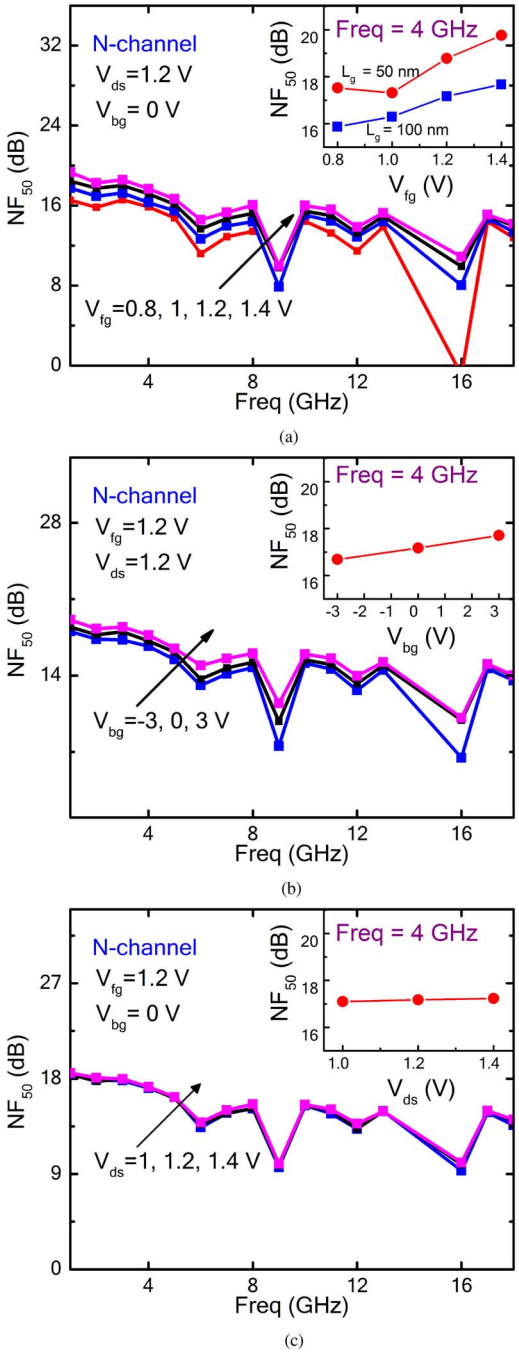

FIGURE 5. (a) Measured NF_{50} vs. frequency characteristics for different front-gate biases $V_{fg} = 0.8, 1, 1.2, 1.4$ V. Frequency is swept from 1 to 18 GHz with the step size of 1 GHz. Inset figure shows the NF_{50} vs V_{fg} characteristics for two channel lengths $L_g = 50$, 100 nm. (b) NF_{50} vs. frequency characteristics for different back-gate biases $V_{bg} = -3, 0, 3$ V. Inset figure shows the NF_{50} vs V_{bg} characteristic for $L_g = 100$ nm. (c) NF_{50} vs. frequency characteristics for different drain biases $V_{ds} = 1, 1.2, 1.4$ V. Inset figure shows the NF_{50} vs V_{ds} characteristic for $L_g = 100$ nm. Device dimensions are: $W_g = 1\mu$m, NF = 40, $T_{ox} = 1.2$ nm, $T_{box} = 25$ nm, $T_{si} = 8$ nm.

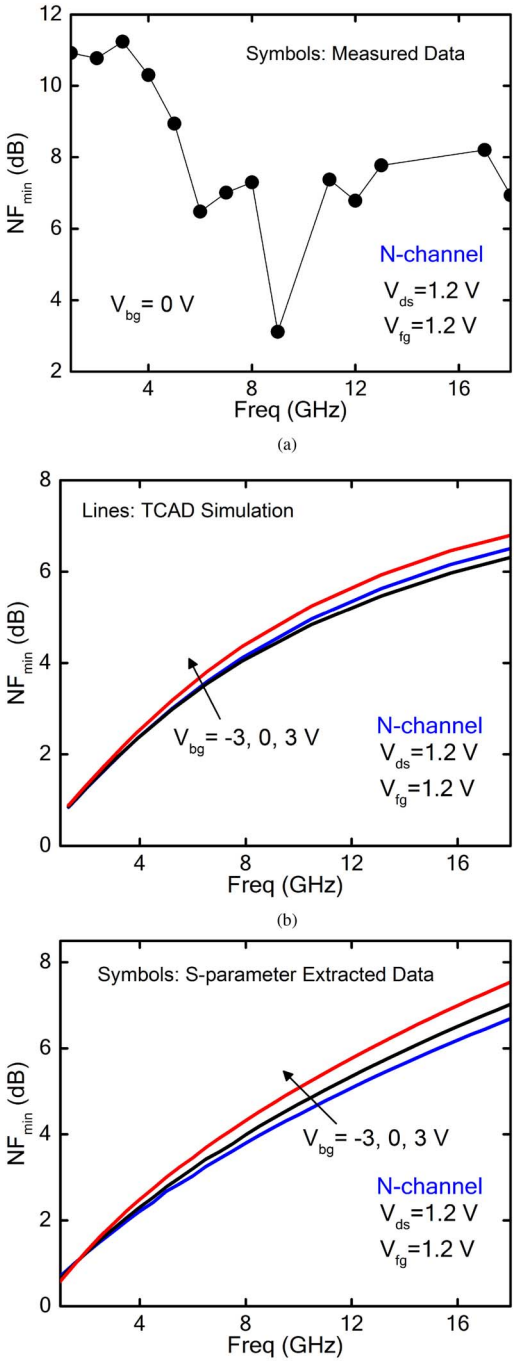

FIGURE 6. (a) Measured NF_{min} vs. frequency characteristics. (b) NF_{min} vs. frequency characteristics from TCAD simulations. (c) NF_{min} vs. frequency characteristics extracted from S-parameter measurement for an FDSOI transistor ($L_g = 100$ nm) with highly doped substrate below the BOX. Frequency is swept from 1 to 18 GHz with the step size of 0.5 GHz. Bias conditions are: $V_{fg} = 1.2$ V and $V_{ds} = 1.2$ V. Parameter values used to calculate NF_{min} for the device are: $R_{gs} = 37.47\ \Omega$ and $R_n = 1.7$, 2.02, 2.35 kΩ for $V_{bg} = -3$, 0, 3 V, respectively. $C_{gs} = C_{gg} - C_{gd}$, where C_{gg} and C_{gd} are shown in Fig. 10(b).

S-parameters and have used these, along with the NF_{50} measurements, to extract the noise parameters R_n, NF_{min}, B_{opt}, G_{opt} and Γ_{opt} as defined from (1) to (5). Fig. 6 shows the frequency dependence of the minimum noise figure for $V_{fg} = 1.2$ V and $V_{ds} = 1.2$ V for different back-gate biases $V_{bg} = -3, 0, 3$ V. Fig. 6(c) shows that the NF_{min} extracted

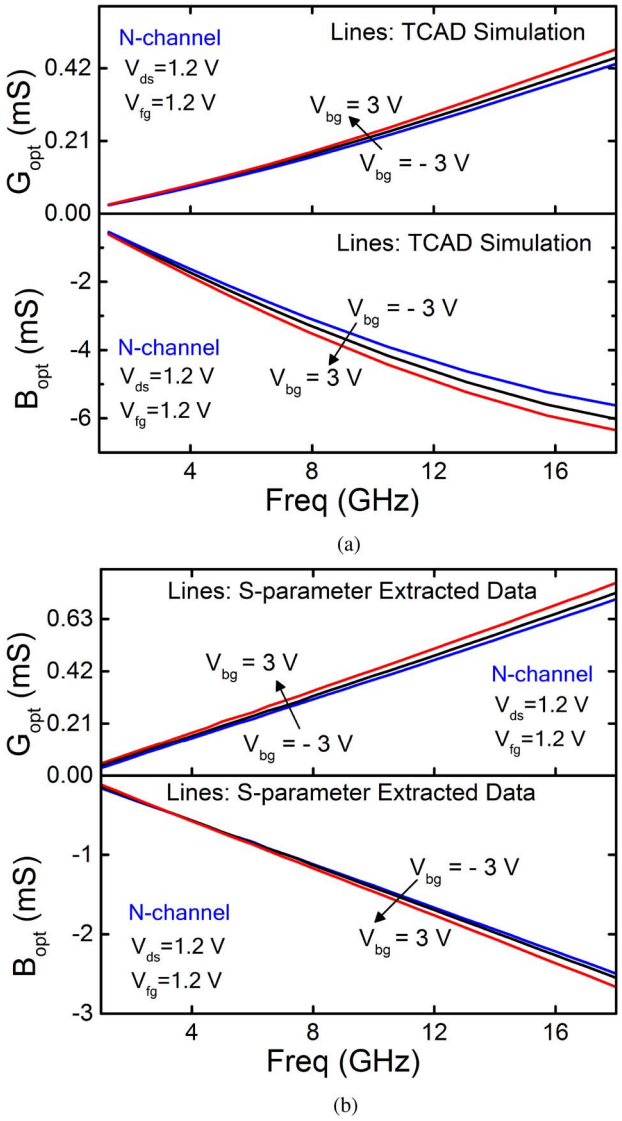

FIGURE 7. **(a) The top figure shows G_{opt} vs. frequency characteristics while the bottom figure shows B_{opt} vs. frequency characteristics, both from TCAD simulations. (b) The top figure shows G_{opt} vs. frequency characteristics while the bottom figure shows B_{opt} vs. frequency characteristics extracted from S-parameter measurements. Bias conditions are: $V_{fg} = 1.2$ V and $V_{ds} = 1.2$ V. Parameter values used to calculate the noise parameters for $L_g = 100$ nm device are: $R_{gs} = 37.47\Omega$ and $R_n = 1.7$, 2.02, 2.35 kΩ for $V_{bg} = -3$, 0, 3 V, respectively. $C_{gs} = C_{gg} - C_{gd}$, where C_{gg} and C_{gd} are shown in Fig. 10(b).**

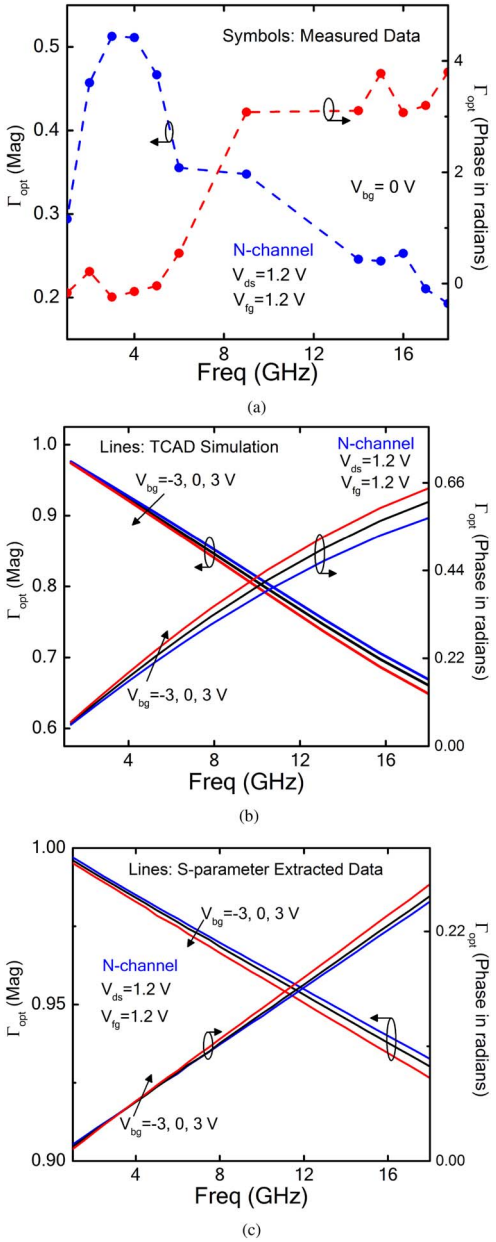

FIGURE 8. **(a) Measured Γ_{opt} vs. frequency characteristics. (b) Γ_{opt} vs. frequency characteristics from TCAD simulations. (c) Γ_{opt} vs. frequency characteristics extracted from S-parameter measurements. Bias conditions are: $V_{fg} = 1.2$ V and $V_{ds} = 1.2$ V. Parameter values used to calculate the Γ_{opt} are: $R_{gs} = 37.47$ Ω and $R_n = 1.7$, 2.02, 2.35 kΩ for $V_{bg} = -3$, 0, 3 V, respectively. $C_{gs} = C_{gg} - C_{gd}$, where C_{gg} and C_{gd} are shown in Fig. 10(b).**

from S-parameter measurements increases with frequency as expected [24], [30]. From (4) and (5), we can see that G_{opt} ($\propto$ f) and B_{opt} ($\propto -$ f) are proportional to frequency. As a result Fig. 7 shows an increase in the magnitude of G_{opt} and B_{opt} with positive and negative slopes, respectively. Fig. 8 shows the variation in the magnitude and the phase of Γ_{opt} with changing frequency. These trends of NF_{min}, G_{opt}, B_{opt} and Γ_{opt} (magnitude and phase) are in good agreement with TCAD simulations as well as with [16], [23], and [24].

Fig. 9(a) shows the behavior of the noise resistance with front gate bias for three different back gate biases. The extracted R_n does not change significantly with frequency because it depends on g_m and C_{gg} (see (1) and (3)), which are independent of frequency (see Fig. 10(a) and Fig. 10(b)).

Although noise resistance R_n is defined in (3) in terms of the device parameters, it can also be expressed as [16]:

$$R_n = R_{gs} + \frac{S_{id}}{g_m^2} I_{ds} \tag{6}$$

From Fig. 10(a), we observe that for higher V_{fg} (= 1.2 V), the transconductance, $g_m (= Re(Y_{21}))$, does not vary much

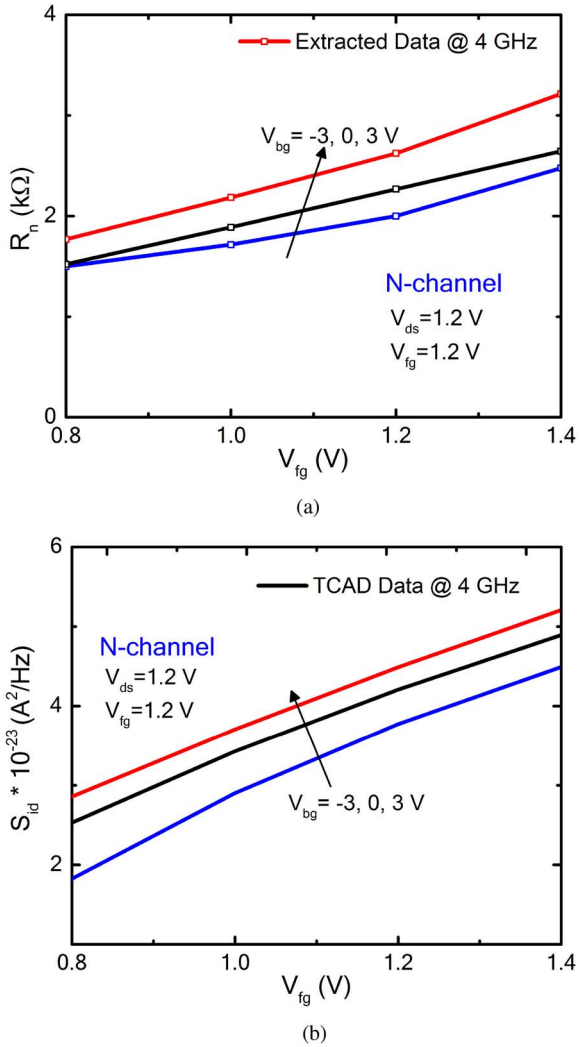

FIGURE 9. **(a) R_n vs. V_{fg} characteristics for different back-gate biases: $V_{bg} = -3, 0, 3$ V. (b) Noise power spectral density S_{id} from TCAD simulations vs. frequency characteristics for different back-gate biases: $V_{bg} = -3, 0, 3$ V. Bias conditions are: $V_{fg} = 1.2$ V and $V_{ds} = 1.2$ V. Device dimensions are: $L_g = 100$ nm, $W_g = 1$ μm, NF = 40, $T_{ox} = 1.2$ nm, $T_{box} = 25$ nm, $T_{si} = 8$ nm.**

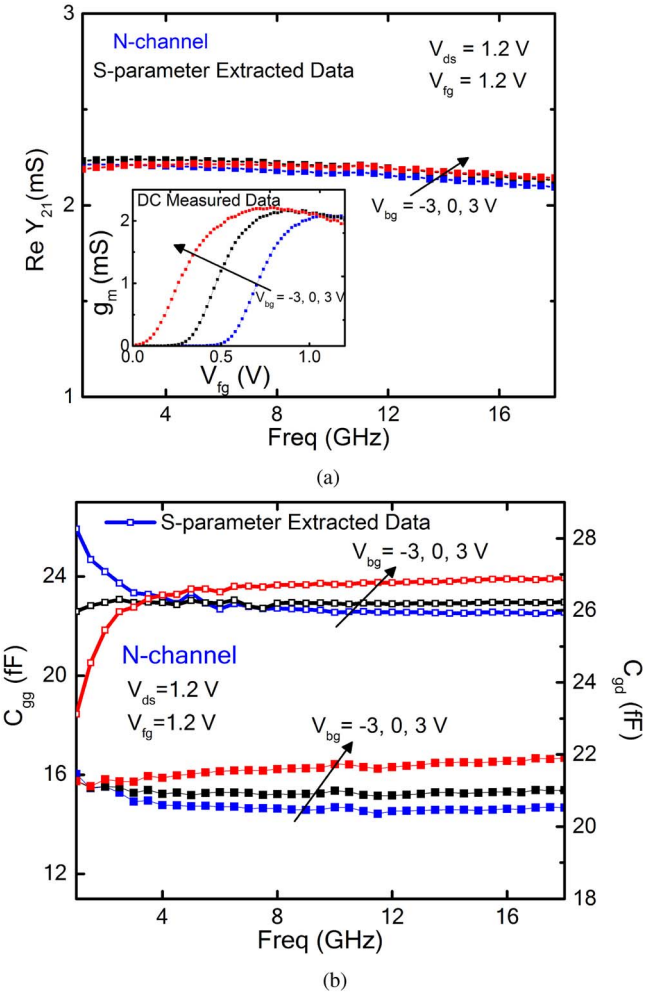

FIGURE 10. **(a) Real part of Y_{21} extracted from S-parameter measurements, vs. frequency for different back-gate biases: $V_{bg} = -3, 0, 3$ V. Inset shows g_m (DC measured data) vs. V_{fg} characteristics for different back-gate biases: $V_{bg} = -3, 0, 3$ V. (b) C_{gg} and C_{gd} extracted from S-parameter measurements vs. frequency characteristics for different back-gate biases: $V_{bg} = -3, 0, 3$ V. Bias conditions are: $V_{fg} = 1.2$ V and $V_{ds} = 1.2$ V.**

with back gate bias while Fig. 9(a) shows larger variation of R_n with back gate bias. From (6), this larger sensitivity of R_n with back bias can be attributed to the significant change in S_{id} with V_{bg} [25] as shown by TCAD simulation, in Fig. 9(b).

VI. CONCLUSION

High frequency noise characterization for ultra thin body and thin BOX FDSOI transistor has been reported for the first time. At high frequencies, substrate resistance induced thermal noise gets coupled with the channel noise and results in higher than expected NF_{min}. This noise coupling increases with reduction in BOX thickness and results in higher NF_{min}. We observe that thermal noise increases with positive back gate bias due to an increase in the number of channel carriers and their collisions. Also, noise figure does not vary significantly with drain bias due to the dominance of the velocity saturation phenomenon in the saturation region.

REFERENCES

[1] Y.-K. Choi *et al.*, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 254–255, May 2000.

[2] Y.-K. Choi *et al.*, "30 nm ultra-thin-body SOI MOSFET with selectively deposited Ge raised S/D," in *Proc. 58th Device Res. Conf. Conf. Dig.*, Denver, CO, USA, 2000, pp. 23–24.

[3] V. Kilchytska, D. Levacq, D. Lederer, J.-P. Raskin, and D. Flandre, "Floating effective back-gate effect on the small-signal output conductance of SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 414–416, Jun. 2003.

[4] S. Makovejev *et al.*, "Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications," *Solid State Electron.*, vol. 108, pp. 47–52, Jun. 2015.

[5] Q. Xie *et al.*, "Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1814–1819, Jun. 2013.

[6] C. Fenouillet-Beranger *et al.*, "Efficient multi-VT FDSOI technology with UTBOX for low power circuit design," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2010, pp. 65–66.

[7] F. Andrieu *et al.*, "Low leakage and low variability ultra-thin body and buried oxide (UT2B) SOI technology for 20nm low power CMOS and beyond," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2010, pp. 57–58.

[8] S. Khandelwal *et al.*, "BSIM-IMG: A compact model for ultrathin-body SOI MOSFETs with back-gate control," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2019–2026, Aug. 2012.

[9] P. Kushwaha *et al.*, "BSIM-IMG: Compact model for RF-SOI MOSFETs," in *Proc. IEEE 73rd Annu. Device Res. Conf.*, Columbus, OH, USA, 2015, pp. 287–288.

[10] P. Kushwaha, S. Khandelwal, J. P. Duarte, C. Hu, and Y. S. Chauhan, "RF modeling of FDSOI transistors using industry standard BSIM-IMG model," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 6, pp. 1745–1751, Jun. 2016.

[11] A. Larie, E. Kerhervé, B. Martineau, L. Vogt, and D. Belot, "2.10 A 60GHz 28nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21 % PAE, 18.2dBm P1dB and 74mW PDC," in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3.

[12] P. Kushwaha *et al.*, "Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG," *Microelectron. J.*, Sep. 2016.

[13] R. Rengel *et al.*, "High-frequency noise in FDSOI MOSFETs: A Monte Carlo investigation," in *Proc. SPIE Noise Devices Circuits*, vol. 5113. Santa Fe, NM, USA, 2003, pp. 379–386.

[14] R. Rengel *et al.*, "A microscopic interpretation of the RF noise performance of fabricated FDSOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 523–532, Mar. 2006.

[15] C. Raynauda *et al.*, "70 GHz F_*MAX* fully-depleted SOI MOSFETs for low-power wireless applications," in *Proc. 30th Eur. Microw. Week (GAAS)*, London, U.K., 2010, pp. 268–271.

[16] S. Asgaran, M. J. Deen, and C.-H. Chen, "Analytical modeling of MOSFETs channel noise and noise parameters," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2109–2114, Dec. 2004.

[17] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of gallium arsenide microwave field-effect transistors," *Adv. Electron. Electron Phys.*, vol. 38, pp. 195–265, May 2008.

[18] S. Makovejev *et al.*, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs," *Solid State Electron.*, vol. 71, pp. 93–100, May 2012.

[19] D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Devices Lett.*, vol. 26, no. 11, pp. 805–807, Nov. 2005.

[20] A. O. Adan, T. Yoshimasu, S. Shitara, N. Tanba, and M. Fukumi, "Linearity and low-noise performance of SOI MOSFETs for RF applications," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 881–888, May 2002.

[21] D. Wang *et al.*, "High performance SOI RF switches for wireless applications," in *Proc. IEEE Solid State Integr. Circuit Technol.*, Shanghai, China, 2010, pp. 611–614.

[22] J.-O. Plouchart, "Applications of SOI technologies to communication," in *Proc. IEEE Symp. Compound Semicond. Integr. Circuit*, 2011, pp. 1–4.

[23] M. J. Deen *et al.*, "High-frequency noise of modern MOSFETs: Compact modeling and measurement issues," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2062–2081, Sep. 2006.

[24] S. Asgaran *et al.*, "Analytical determination of MOSFET's high-frequency noise parameters from NF_{50} measurements and its application in RFIC design," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1034–1043, May 2007.

[25] K. Han *et al.*, "Complete high-frequency thermal noise modeling of short-channel mosfets and design of 5.2-GHz low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 726–735, Mar. 2005.

[26] P. Kushwaha *et al.*, "Modeling the impact of substrate depletion in FDSOI MOSFETs," *Solid State Electron.*, vol. 104, pp. 6–11, Feb. 2015.

[27] W. Jin, P. C. H. Chan, and J. Lau, "A physical thermal noise model for SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 768–773, Apr. 2000.

[28] A. O. Adan, M. Koyanagi, and M. Fukumi, "Physical model of noise mechanisms in SOI and bulk-silicon MOSFETs for RF applications," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 872–880, Mar. 2008.

[29] Y. Cheng, M. J. Deen, and C.-H. Chen, "MOSFET modeling for RF IC design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1286–1303, Jul. 2005.

[30] S. Asgaran, M. J. Deen, and C.-H. Chen, "An analytical method to determine MOSFET's high frequency noise parameters from 50 ohm noise figure measurements," in *Proc. IEEE Radio Frequency Integr. Circuits RFIC Symp.*, San Francisco, CA, USA, 2006, pp. 341–345.

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