Received 8 June 2016; revised 31 July 2016; accepted 10 August 2016. Date of publication 16 August 2016; date of current version 24 October 2016.
The review of this paper was arranged by Editor C. C. McAndrew.

Digital Object Identifier 10.1109/JEDS.2016.2600375

Performance Investigation of Single Grain Boundary Junctionless Field Effect Transistor

MAMIDALA SAKETH RAM[1] AND DAWIT BURUSIE ABDI[2] (Member, IEEE)

1 Faculty of Electrical Engineering and Information Technology, TU Chemnitz, 09126 Chemnitz, Germany
2 Department of Electrical Engineering, Indian Institute of Technology, New Delhi 110 016, India

CORRESPONDING AUTHOR: D. B. ABDI (e-mail: dave.abdi@gmail.com)

ABSTRACT In this paper, we report a single grain boundary (GB) junctionless thin film transistor (JLFET) on recrystallized polycrystalline silicon (poly-Si JLFET). Using 2-D simulations, the electrical performance of the poly-Si JLFET is evaluated for different single GB locations in the channel. Without the need for creating the source and the drain regions by implantation, we demonstrate the prospect of achieving thin-film poly-Si JLFETs whose performance is reasonable for silicon film thicknesses less than 10 nm.

INDEX TERMS Junctionless FET (JLFET), thin-film transistor (TFT), poly-Si, grain boundary (GB), simulation, glass substrates.

I. INTRODUCTION

Poly-crystalline silicon (poly-Si) thinfilm transistors (TFTs) are extensively used in active matrix displays, 3D multi-layer integrated circuits and flash memory applications [1]. Such poly-Si TFTs with a single grain boundary (GB) at a controlled location in the channel also exhibit performances similar to that of single crystal transistors [2]–[12]. However, annealings required for dopant activation in the source/drain regions of the TFTs can lead to severe diffusion and redistribution of dopants in 3-D structures [13], [14]. We can overcome this problem if the TFT structure does not require source and drain dopings. One such structure is the junctionless thin film transistor (JLFET) which consists of a heavily doped silicon film from the source through channel to the drain in which the current is turned-off by modulating the channel depletion region using a gate of suitable work function [15]. A JLFET is similar to a gated resistor with uniform doping. Therefore, the JLFETs do not suffer from the doping related issues [15]. As compared to the conventional inversion-mode MOSFETs, JLFETs have several advantages such as a simplified processing without diffusion related problems, a high channel conductivity due to heavily doped silicon film and low gate capacitances [17]. JLFETs have also been demonstrated on polycrystalline silicon due to their low thermal budget processes and their suitability in monolithic and 3D stacked ultra-high density memory applications and integrated circuits [18], [19]. The polycrystalline JLFETs reported earlier suffered from performance degradation owing to the small grain size. An increase in the grain size of the poly-Si channel results in a reduction in defects and leads to improved performance in terms of reduced subthreshold swing (SS) and large ON-state current [20]. Furthermore, the number and the location of the grain boundaries in the channel of the device also affect the overall performance. Poly-Si crystallization techniques, namely excimer laser anneal (ELA) methods using sequential lateral solidification (SLS), are used (i) to make short-channel TFTs (< 100 nm) with a single grain boundary and (ii) to also precisely control the grain boundary location in the channel [10]–[12].

While most studies have focused on the design and performance of poly-Si JLFETs, there is no study which focused on the impact of the position of the single grain boundary (GB) on the electrical characteristics of the poly-Si JLFET. Therefore, in this paper, to combine the advantages of the polycrystalline single GB TFT and the junctionless FET, using 2-D simulations, we report for the first time, a single GB JLFET as a potential candidate for TFT applications.

Using calibrated 2-D TCAD simulations, we have studied the effect of the GB position in the channel region on the electrical characteristics of these transistors. We demonstrate that a single GB JLFET without the need of creating source

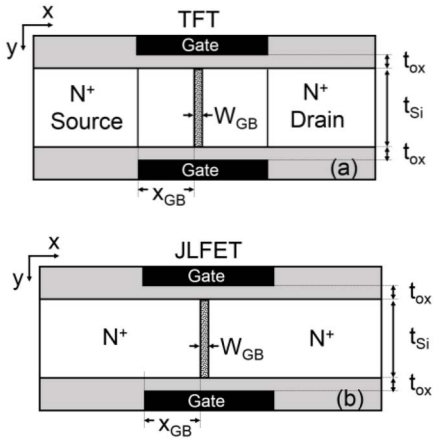

FIGURE 1. Schematic view of a single GB (a) conventional TFT and (b) JLFET.

and drain region exhibits reasonable performance for silicon film thickness (t_{si}) less than 10 nm. We believe that our results will be an incentive for further experimental exploration.

II. DEVICE STRUCTURE, MODELS AND GRAIN BOUNDARY REPRESENTATION

Fig. 1 shows the cross-sectional view of a single GB (a) TFT and (b) JLFET. For both the structures, the parameters used in our simulation are given in Table 1. Although, the channel lengths of a conventional TFT can be ~1 μm, TFTs with short channel lengths have been shown to exhibit enhanced performance [21]–[23]. For this reason, a 50 nm channel length is chosen for the devices studied in this work.

We have used Silvaco Atlas, Version 5.19.20.R [24] to perform all the simulations. Fermi-Dirac distribution, Shockley-Read-Hall (SRH) recombination, trap assisted tunneling (TAT), band-gap narrowing (BGN) and Lombardi (CVT) models were included. The trap-assisted tunneling can be modeled by suitably adjusting the appropriate enhancement factors [25] in the trap lifetimes to include the effects of phonon-assisted tunneling on the emission of electrons and holes from a trap [24]. As is the practice in earlier studies, we have considered a 4 nm long GB in the channel along with the associated acceptor-like and donor-like traps [8], [26]–[28]. The parameters used to represent the traps at the grain boundary are given in TABLE 2. Near the conduction band and the valence band, we have assumed two exponential defect state tail bands and a Gaussian distribution is used for the two deep-level bands [8], [29]. It may also be noted that in a real poly-Si film, the orientation of the GB is random. However, we have assumed the GB orientation to be orthogonal to the semiconductor surface for a worst case effect on the channel transport [8], [26]–[28]. The effect of the GB in the channel is considered by incorporating the trapped charges at the GB in Poisson's equation as well as by invoking a modified Shockley-Read-Hall (SRH) term in the carrier continuity equations. We have not considered the quantum mechanical and impact ionization effects. To validate our simulation results, we have calibrated our simulation models by first replicating the short channel TFT characteristics with a single GB in the channel [8].

TABLE 1. Device parameters.

Parameter	JLFET	TFT
Silicon film thickness t_{si}	10 nm	10 nm
Gate oxide thickness (HfO_2) t_{ox}	10 nm	10 nm
Channel length	50 nm	50 nm
Grain boundary width W_{GB}	4 nm	4 nm
Gate work function	4.72 eV	4.72 eV
Source/Drain doping N_D	$1\times10^{19}/cm^3$	$1\times10^{20}/cm^3$
Channel doping	$N_D = 1\times10^{19}/cm^3$	$N_A = 1\times10^{17}/cm^3$

TABLE 2. Simulation parameters [8], [29].

Parameter	Value
Capture cross section of (i) electrons in acceptor-like states σ_{ae} and (ii) holes in donor-like states σ_{dh}	1×10^{-16} cm^2
Capture cross section of (i) electrons in donor-like states σ_{de} and (ii) holes in acceptor-like states σ_{ah}	1×10^{-14} cm^2
Density of acceptor-like tail states N_{TA}	1×10^{21} cm^{-3} eV^{-1}
Density of donor-like tail states N_{TD}	4×10^{20} cm^{-3} eV^{-1}
Density of acceptor-like Gaussian states N_{GA}	5×10^{19} cm^{-3} eV^{-1}
Density of donor-like Gaussian states N_{GD}	5×10^{19} cm^{-3} eV^{-1}
Decay energy for acceptor-like tail states W_{TA}	0.05 eV
Decay energy for donor-like tail states W_{TD}	0.05 eV
Decay energy for acceptor-like Gaussian W_{GA}	0.1 eV
Decay energy for donor-like Gaussian W_{GD}	0.1 eV
Energy of Gaussian for acceptor-like states E_{GA}	0.51 eV
Energy of Gaussian for donor-like states E_{GD}	0.51 eV

III. RESULTS AND DISCUSSION

Fig. 2 (a) shows the transfer characteristics for JLFET without GB and with single GB with varying positions (X_{GB}) of the GB in the channel region and Fig. 2 (b) shows the transfer characteristics for the conventional TFT without GB and with single GB TFT with varying positions (X_{GB}) of the GB in the channel region. $X_{GB} = 0$ nm corresponds to the beginning of the channel. In Fig. 2(c), the transfer characteristics of these two structures are compared for different silicon film thicknesses when the single GB is in the center of the channel ($X_{GB} = 22$ nm). We observe that for $t_{si} = 10$ nm, the JLFET with a single GB exhibits a larger OFF-state current and higher SS compared to that of the single GB conventional TFT. This higher OFF-state current in a single GB JLFET is due to the inefficient depletion of the channel in the OFF-state condition. However, this problem can be overcome if t_{si} is reduced from 10 nm to 7 nm. As can be seen from Fig. 2(c), for $t_{si} = 7$ nm, the JLFET with a single GB exhibits a reduced OFF-state current and improved SS while these two parameters are not affected for the single GB conventional TFT.

For the single GB JLFET, there is negligible change in the OFF-state current when the GB position is moved away from

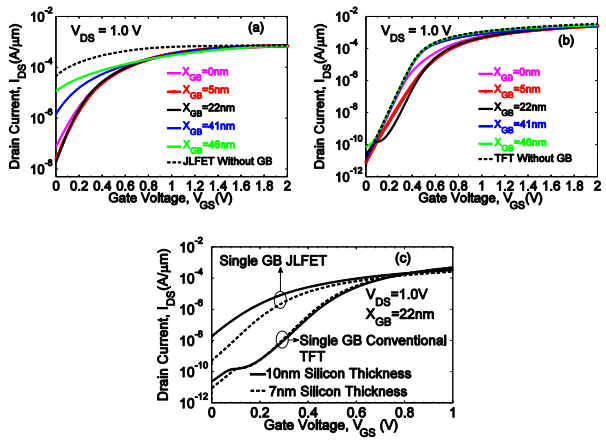

FIGURE 2. The impact of the GB and the GB position on the transfer characteristics of the single GB for silicon thickness t_{si} = 10 nm (a) JLFET and (b) TFT; and (c) comparison of the single GB JLFET and conventional TFT transfer characteristics for silicon thicknesses t_{si} = 10 nm and t_{si} = 7 nm at X_{GB} = 22 nm.

the center of the channel (i.e., X_{GB} = 22 nm) towards the source-channel. However, when the GB position is moved away from the center of the channel (i.e., X_{GB} = 22 nm) towards the channel-drain interface, there is a significant change in the OFF-state current of the single GB JLFET. This phenomena of increase in the OFF-state current as the grain boundary is moved toward the channel-drain interface can be understood from the energy band profile and the electron concentration contour shown in Fig. 3 as a function of the grain boundary positions. As shown in Fig. 3(a1-e1) of energy band profiles, the grain boundary introduces an energy barrier which inhibits electron flow from the source into the channel. For example, when the grain boundary is at the source-channel interface the channel is fully depleted as shown in the OFF-state electron concentration contours of Fig. 3(a2). However, as the position of the grain boundary moves away from the source-channel interface, part of the channel starts to get filled with electrons from the source region. This is clearly due to the movement of the barrier height along the position of the grain boundary as shown in Fig. 3(a1-e1) of energy band profile. The effect of the grain boundary position is negligible as long as the grain boundary is near the source-channel interface as most part of the channel is depleted for these positions. On the other hand, for the grain boundary position near channel-drain interface, the OFF-sate current increases due to the reduction in the channel resistance. This reduction in the channel resistance can be inferred from the electron concentration contours of Fig. 3(a2-e2) and the electron concentration variation of Fig. 3(f) for different grain boundary positions. When the grain boundary position is at the channel-drain interface (i.e., X_{GB} = 46 nm), the electron concentration in the channel is close to that of the JLFET without a grain boundary as shown in Fig. 3(g). This results in an almost equal OFF-state current for the single GB JLFET with the grain boundary position located at X_{GB} = 46 nm and the JLFET without

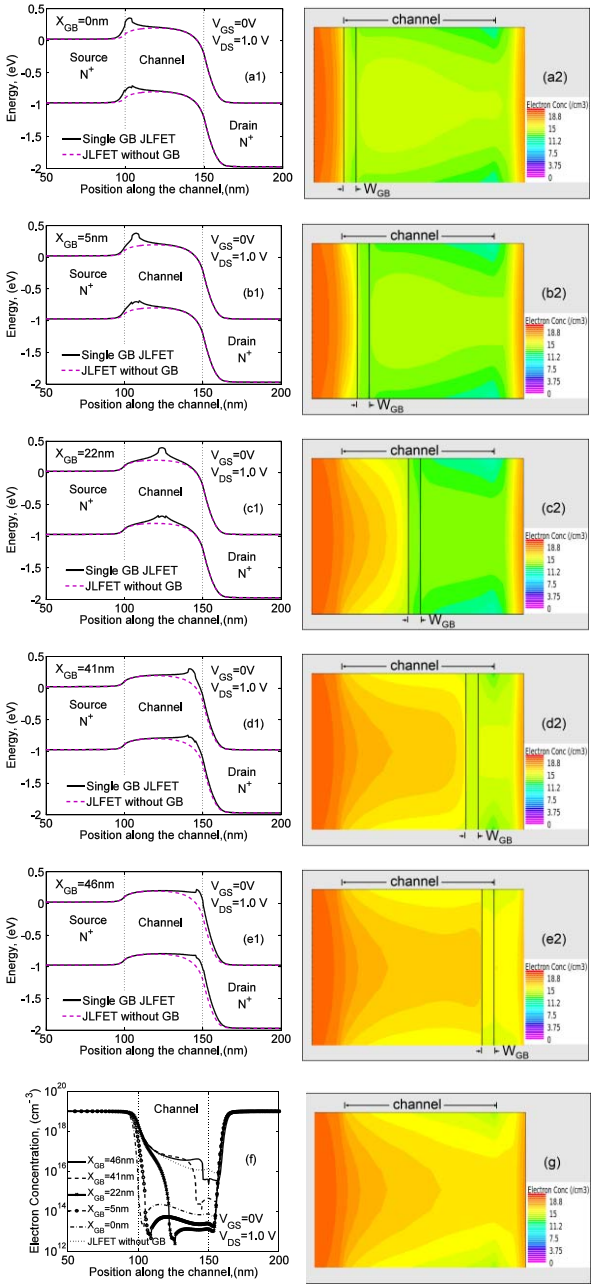

FIGURE 3. Energy-band profiles and electron concentration contours in the OFF-state (V_{GS} = 0 V, V_{DS} = 1 V) of a single GB JLFET at X_{GB} = 0 nm (a1 and a2), X_{GB} = 5 nm (b1 and b2), X_{GB} = 22 nm (c1 and c2), X_{GB} = 41 nm (d1 and d2), X_{GB} = 46 nm (e1 and e2); and (f) electron concentration in the middle of the channel (i.e., for a cutline at t_{si} = 5 nm along the x-direction) for different grain boundaries of single GB JLFET and JLFET without grain boundary; and (g) OFF-state electron concentration contour of JLFET without grain boundary.

a grain boundary as shown by the transfer characteristics of Fig. 4. The increase in the OFF-state current is not significant in the case of single GB conventional TFT when the grain boundary is moved across the channel. This is due to the PN junction nature of the source-channel junction which has an inbuilt barrier to prevent the flow of electrons into the channel irrespective of the grain boundary positions.

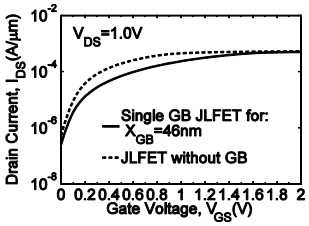

FIGURE 4. **Transfer characteristics of the single GB JLFET for the grain boundary position X_{GB} = 46 nm and the JLFET without GB. The silicon thickness for both devices is t_{si} = 7 nm.**

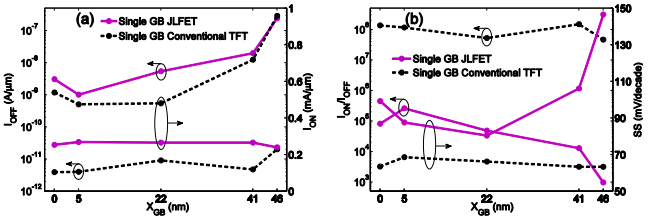

FIGURE 5. **(a) ON-state ($V_{GS} = V_{DS} = 1.0$ V) (I_{ON}) and OFF-state ($V_{GS} = 0$ V, $V_{DS} = 1.0$ V) (I_{OFF}) currents and (b) I_{ON}/I_{OFF} and the subthreshold swing (SS) for different positions (X_{GB}) of the single GB JLFET and the single GB conventional TFT with t_{si} = 7 nm.**

The effect of the GB position on I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and the sub-threshold swing (SS) of the single GB JLFET and single GB conventional TFT are shown in Fig. 5. We observe from Fig. 5(a) that the ON-state current of the single GB JLFET is relatively unaffected by the grain boundary position. However, the OFF-state current (I_{OFF}) increases as the grain boundary moves from the center of the channel towards the channel-drain interface for reasons indicated by Fig. 3. From Fig. 5(b), we observe that to get the best I_{ON}/I_{OFF} ratio and the subthreshold swing, the grain boundary position in a single GB JLFET can be anywhere between the source-channel interface and the middle of the channel. This makes the single GB JLFET a likely candidate for the display and memory technology without the need for the thermal budgets required to create the source/drain regions required in a single GB conventional TFT. Our results may provide the motivation for further experimental exploration.

IV. CONCLUSION

In this paper, using 2-D simulations, we have evaluated the performance of a single grain boundary JLFET and studied the effect of the GB position in the channel region. We have demonstrated that when a single GB is present towards the source from the center of the channel region, the proposed JLFET exhibits a reasonable performance for silicon film thicknesses less than 10 nm. Our study testifies the possibility of realizing a single GB JLFET with a low thermal budget, reduced fabrication complexity and no doping related issues by avoiding abrupt junctions. The proposed single GB JLFET could be a potential replacement for the conventional thin film transistors used in today's display or memory technology.

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MAMIDALA SAKETH RAM was born in Kitchener, ON, Canada. He received the bachelor's degree in electronics and communication engineering from the M. S. Ramaiah Institute of Technology, Bengaluru, India. He is currently pursuing the master's degree in micro and nano systems with TU Chemnitz, Germany. He was with the Center for Nano Science and Engineering, Indian Institute of Science, Bengaluru, researching on thin-film transistors. His research interests are in nanoelectronic devices, MEMS, and low-power transistors.

DAWIT BURUSIE ABDI (M'16) received the B.Sc. degree in electrical engineering from Jimma University, Ethiopia, in 2009, and the M.Tech. degree in microelectronics from the Addis Ababa Institute of Technology, Ethiopia, in 2011. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India. His current research interests include design, simulation, and modeling of nanoscale semiconductor devices.