

Received 3 June, 2016; revised 14 June, 2016; accepted 14 June, 2016. Date of publication 29 July 2016; date of current version 24 October 2016.
The review of this paper was arranged by Editor M. Chan.

Digital Object Identifier 10.1109/JEDS.2016.2586116

Modeling of Charge and Quantum Capacitance in Low Effective Mass III-V FinFETs

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This work was supported in part by the Semiconductor Research Corporation, in part by the Ramanujan Fellowship, in part by the Science and Engineering Research Board, and in part by the Council of Scientific and Industrial Research.

ABSTRACT In this paper, we present a compact model for semiconductor charge and quantum capacitance in III-V channel FETs. With III-V being viewed as the most promising candidate for future technology node, a compact model is needed for their circuit simulation. The model presented in this paper addresses this need and is completely explicit and computationally efficient which makes it highly suitable for SPICE implementation. The proposed model is verified against the numerical solution of coupled Schrödinger–Poisson equation for FinFET with various channel thickness and effective mass.

INDEX TERMS III-V, density of states (DOS), SPICE, FinFET, quantum capacitance.

I. INTRODUCTION

As the current CMOS technology with conventional silicon channel is reaching to its scaling limits, several new materials and device architectures are being actively explored for future generation [1]–[5]. Among them the III-V channel material with ultrathin-body and multigate architecture is probably the most promising candidate, especially for nMOSFETs [6]–[10]. The III-V materials because of their lower effective mass offer higher channel mobility along with the possibility of integration with the conventional silicon CMOS technology [11]–[13]. The ultrathin-body and multigate architecture offer superior electrostatic control [14]. If III-V materials had to replace silicon, especially for logic applications, it is necessary to analyze their performance at circuit level. This requires a computationally efficient compact model for circuit simulators.

Several performance metrics for circuits such as switching delay (CV/I), transconductance, and dynamic power consumption (CV^2) depend directly on the gate capacitance (C_g). Therefore, the analysis of C_g is very important for any circuit simulation and development of future technology generation. Typically in inversion regime, the total C_g of a metal-insulator-semiconductor (MIS) system

can be modeled as a series combination of the insulator capacitance ($C_{ins} = \epsilon_{ins}/t_{ins}$) and inversion layer capacitance (C_{inv}) [15]. The C_{inv} for an undoped fully depleted ultrathin-body device comprises of the centroid capacitance (C_{cen}) [16] in series with quantum capacitance (C_Q) [17], [18]. Of these, the C_Q is proportional to the density of state (DOS) and valley degeneracy. The III-V materials have lower DOS (due to their lower effective mass) and valley degeneracy as compared to the silicon. This results in a much lower C_Q and the overall C_g is then limited by the C_Q [18]. Therefore it is necessary to accurately model the impact of low DOS on the total C_g in III-V channel FETs.

Several different models have been presented in literature which include the effect of C_Q in total C_g . The formulation presented in [19] is computationally expensive and is not fit for the SPICE simulators. The models presented in [20] and [21] are physical but require iterations and result into a complicated formulation. Also these models do not consider the effect of band non-parabolicity on C_g . In this paper, we have presented a physics based model for C_Q . We have then developed a compact formulation of C_Q by utilizing this form of equation with suitable approximation.

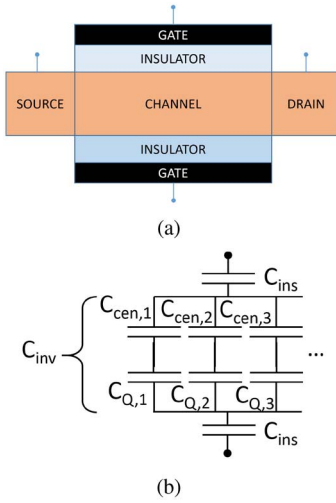


FIGURE 1. (a) Schematic diagram of the FinFET structure used in this work, (b) Equivalent capacitance network for the device shown in fig (a). C_{ins} is the gate insulator capacitance and C_{inv} is inversion capacitance, which is represented in terms of the contribution from centroid capacitance ($C_{cen,i}$) and quantum capacitance ($C_{Q,i}$) in each subband. The subscript i represents the subband number.

The developed model is computationally efficient, simple yet accurate without compromising much of the physics. The model is also extended to include the effect of conduction band non-parabolicity on C_g without compromising the computational efficiency. The proposed model is completely explicit in terms of the applied gate voltage V_G thereby making it highly suitable for SPICE implementation.

This paper is organized as follows: Section II presents the formulation and model description. Section III includes the model verification and discussion regarding the same, followed by conclusion in Section IV.

II. MODEL DESCRIPTION

Fig. 1 shows the device geometry considered in this work along with the total C_g . The C_{inv} consists of parallel combination of the contributions from each of the occupied electron subband in the channel. For each subband, the C_{inv} in turn consists of a series combination of C_{cen} and C_Q as shown in fig. 1(b) [18]. Therefore, the C_{inv} can be written as,

$$C_{inv} = \sum_i \left(\frac{1}{C_{Q,i}} + \frac{1}{C_{cen,i}} \right)^{-1} \quad (1)$$

where $C_{Q,i}$ and $C_{cent,i}$ is the quantum capacitance and centroid capacitance associated with each subband respectively. Here, we have neglected the effect of charge centroid which can later be added using conventional method of introducing a correction factor to the oxide thickness [22], [23]. Therefore the total gate capacitance (C_g) is given by

$$C_g = \left(\frac{1}{2C_{ins}} + \frac{1}{\sum_i C_{Q,i}} \right)^{-1} \quad (2)$$

Following the methodology described in [18] the quantum capacitance for each subband can be written as,

$$C_{Q,i} = q \frac{\partial (-Q_i)}{\partial (E_f - E_i)} \quad (3)$$

where Q_i is the contribution of i^{th} subband to the total semiconductor charge (Q_s), E_i is the energy level of i^{th} subband and E_f is the fermi energy. In order to get Q_s for a two dimensional (2D) system such as the FinFET structure discussed in this work, 2D DOS should be considered. Considering 2D DOS, Q_s can be formulated as,

$$Q_s = \sum_i Q_i = \sum_i \int_{E_i}^{\infty} \frac{m_{||}^* q}{\pi \hbar^2} \frac{1}{1 + \exp\left(\frac{E - E_f}{kT}\right)} dE \quad (4)$$

where $m_{||}^*$ is the in plane electron effective mass.

Substituting (4) in (3) and differentiating (3) we get,

$$C_{Q,i} = \frac{m_{||}^* q^2}{\pi \hbar^2} \frac{1}{1 + \exp\left(\frac{E_i - E_f}{kT}\right)}. \quad (5)$$

Eq. (5) along with (2) gives us the total C_g . But in order to get the C_g as a function of the applied V_G , it is necessary to get the variation of $C_{Q,i}$ with respect to V_G . Note that both the subband energy level E_i and fermi level E_f appearing in expression of $C_{Q,i}$ change with V_G (considering bottom of the conduction band E_c as the reference). Therefore, to get the variation of $C_{Q,i}$ with V_G we need to express E_f and E_i as a function of V_G . This has been derived analytically in [20] and [21] which results in complex expression of total C_g .

From (5) it can be seen that for a particular subband when $E_f \ll E_i$ the denominator is very large and $C_{Q,i}$ is negligible. When $E_f \gg E_i$, the denominator can be approximated to unity and $C_{Q,i}$ becomes constant and independent of V_G . Therefore, for both this extreme the exact relation of E_f vs V_G becomes unimportant for modeling of $C_{Q,i}$. An accurate form of this relation is only needed for a very narrow range around E_i . Leveraging this fact, instead of modeling E_f as a function V_G for entire bias range, we treat each subband separately and approximate the relation between E_f and V_G by a straight line ($E_f \propto V_G$) around the subband energy E_i . Therefore, the above expression of $C_{Q,i}$ can be written in a compact form as a function of V_G as,

$$C_{Q,i} = \frac{A_i \frac{m_{||}^* q^2}{\pi \hbar^2}}{1 + \exp\left(\frac{E_i - (B_i q V_G)}{C_i kT}\right)} \quad (6)$$

Here A_i , B_i , C_i are fitting parameters included in order to provide the flexibility to fit various real data.

The value of subband energy required to find the quantum capacitance can be derived as in [20]. However this approach still requires an implicit equation to be solved iteratively.

Since our model has a parameter to control the capacitance inflection points, we can use the subband energy calculated from an explicit expression for infinite quantum well [24]

$$E_i = \frac{i^2 \pi^2 \hbar^2}{2m_{\parallel}^* t_{ch}^2} \quad (7)$$

where t_{ch} is the channel thickness and i is the eigennumber of the subband.

Expression of $C_{Q,i}$ given by (6) along with (7) can be used in (2) to obtain an explicit expression of C_g in terms of V_G . However due to the traditional problem of charge conservation it is preferable to have a charge based implementation instead of a capacitance based which requires a continuous model of semiconductor charge [25]. Solving (4), Q_s as a function of E_f can be written as,

$$Q_s = \sum_i \frac{m_{\parallel}^* q k T}{\pi \hbar^2} \ln \left[1 + \exp \left(\frac{E_f - E_i}{k T} \right) \right] \quad (8)$$

Using the same form of approximations as for C_Q discussed above, a new compact expression of Q_s is derived as,

$$Q_s = \sum_i D_i \frac{m_{\parallel}^* q k T}{\pi \hbar^2} \ln \left[1 + \exp \left(\frac{(B_i q V_G) - E_i}{C_i k T} \right) \right] \quad (9)$$

Eq. (9) gives a continuous model of charge valid for all the regions of operation. The form of the model also ensures that the derivatives are continuous. Differentiation of (9) gives C_Q and has the same form as derived earlier.

The model is derived assuming parabolic conduction band structure, hence a constant value of effective mass is used. But, the non-parabolicity of conduction band causes effective mass to vary with energy. This is particularly important in case of III-V materials and changes the C_g in inversion [26], [27]. The effect of non-parabolic band structure could be modeled by modifying the effective mass as follows:

$$m_{\parallel}^* = m_b^* (1 + 2\alpha E) \quad (10)$$

where m_b^* is the effective mass at bottom of the conduction band, and α is known as non-parabolicity factor [28]. But, modifying the effective mass will cause difficulty in analytical derivation of Q_s and an explicit expression could not be derived. This in turn will affect the computational efficiency of the model. However, the presented model could still be modified to include this effect. For a parabolic band structure approximation, the C_Q doesn't change with V_G once the Fermi level moves above a particular subband. This is due to constant effective mass and thus constant DOS for 2D materials. But for non-parabolic bands, increase in V_G causes an increase in C_Q even after the Fermi level moves above the subband [29]. This effect could be modeled by

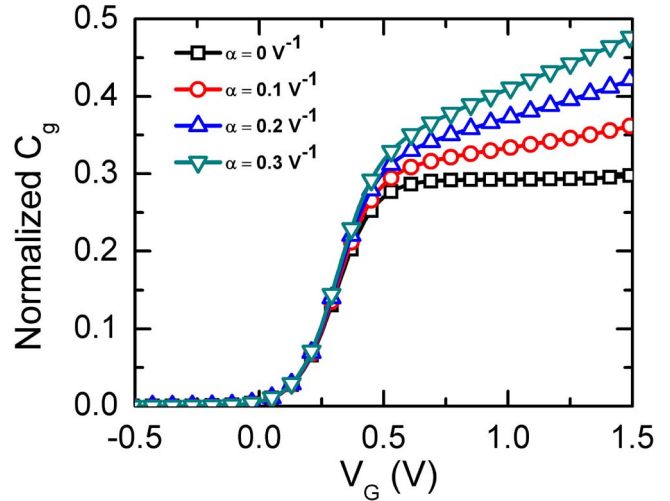


FIGURE 2. Normalized gate capacitance, C_g for different V_G at $V_{DS} = 0$ V with insulator thickness, $t_{ins} = 1$ nm and $m_b^* = 0.048m_0$, where m_0 is the free electron mass. Different curves are for different value of factor α . The normalization of C_g is done with the insulator capacitance. It can be seen that the effect of band non-parabolicity on C_g is similar to what described by Ali *et al.* [29]. Note that only one subband is considered here.

modifying (9) as follow:

$$Q_s = \sum_i D_i \frac{m_b^* (1 + \alpha V_G) q k T}{\pi \hbar^2} \ln \left[1 + \exp \left(\frac{(B_i q V_G) - E_i}{C_i k T} \right) \right] \quad (11)$$

here the factor α is similar to the non-parabolicity factor in (10) with unit V^{-1} and could be used to tune the effect of non-parabolicity.

Equation (11) captures the effect of non-parabolicity in band structure by making effective mass a function of V_G . The effect of including non-parabolicity in the model is shown in fig. 2. It can be seen that the C_g varies with V_G for non zero value of constant α , where as $\alpha = 0$ gives a constant plateau.

In the subsequent section we will verify the presented model against the numerical simulation data. The simulation assumes the parabolic band structure and hence the model with value of $\alpha = 0$ is used to match the results. However, it is shown that the model could include the effect of non-parabolicity through the factor α .

III. MODEL VERIFICATION

In this section, the C_g and Q_s , derived from the model described in Section II, are verified with the data obtained from numerical simulation of the FinFET device (shown in fig. 1). The simulation data are obtained from self-consistent solution of coupled Schrödinger-Poisson equation [30]. The simulation takes into account the finite barrier height at the insulator/semiconductor interface. A barrier height of 3.4 eV is considered in the simulation. The simulation therefore, considers the wavefunction penetration into the insulator. It also takes into account the difference in carrier effective

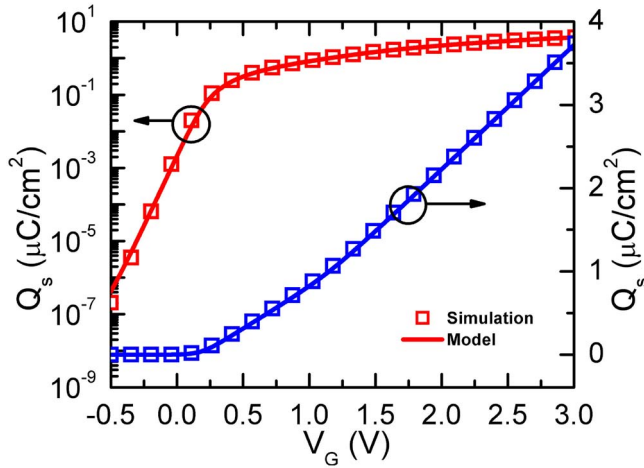


FIGURE 3. Semiconducter charge, Q_s vs V_G at $V_{DS} = 0$ V for device shown in fig. 1(a) with insulator thickness, $t_{ins} = 1$ nm, in plane effective mass, $m_{||}^* = 0.048m_0$ and channel thickness, $t_{ch} = 7$ nm.

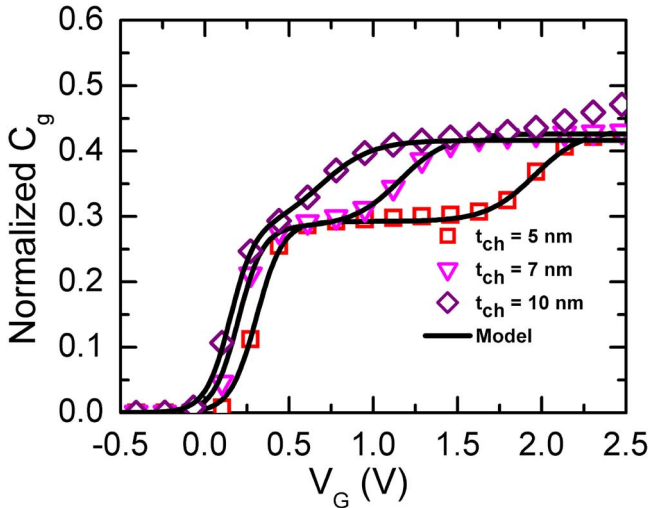


FIGURE 4. Comparison of the presented model with the simulated gate capacitance, C_g for different V_G at $V_{DS} = 0$ V with insulator thickness, $t_{ins} = 1$ nm and in plane effective mass, $m_{||}^* = 0.048m_0$. Different curves are for different channel thickness. The normalization of C_g is done with the insulator capacitance. Different inflection points in C_g corresponds to different electron subbands. Note that as only lowest two subbands are considered while plotting the capacitance using the model, the third peak in C_g for $t_{ch} = 10$ nm which corresponds to the 3rd electron subband is not captured using the model. Reduction in the channel thickness causes an increase in the subband energy which results in the shifting of the inflection point toward higher V_G values.

mass of the oxide and channel material. The SiO_2 insulator material with an effective mass of $m_{ox} = 0.55m_0$, where m_0 is the free electron mass and an undoped channel is considered.

Fig. 3 compares the semiconductor charge obtained from the model to the numerical simulation data. The data corresponds to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel with $m_{||}^* = 0.048m_0$. It can be seen from fig. 3 that the proposed model provides an excellent match to the simulation data.

Fig. 4 shows C_g versus V_G for different channel thickness with $t_{ins} = 1$ nm and $m_{||}^* = 0.048m_0$. Here only the

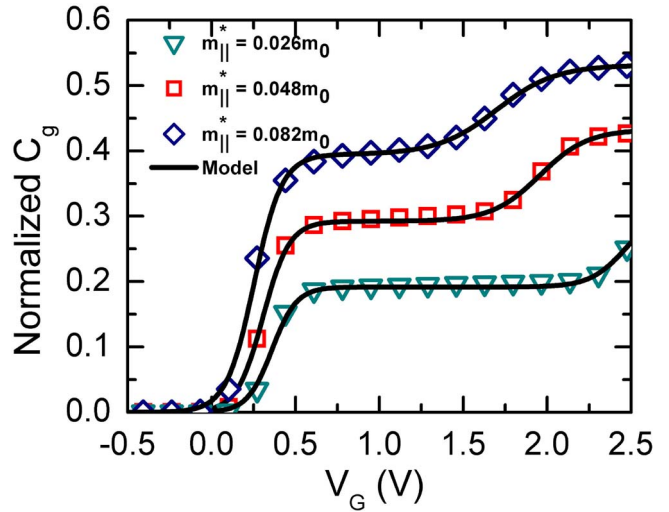


FIGURE 5. Gate capacitance, C_g versus V_G at $V_{DS} = 0$ V for devices with channel thickness, $t_{ch} = 5$ nm and insulator thickness, $t_{ins} = 1$ nm for different in-plane effective mass $m_{||}^*$. The normalization of C_g is done with insulator capacitance. In-plane effective mass of $0.026m_0$, $0.048m_0$ and $0.082m_0$ corresponds to InAs , $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and GaAs channel materials respectively. Lower in-plane effective mass gives lower C_Q and a greater impact of C_Q on C_g due to a series combination of C_{ins} and C_Q .

contribution from first two subbands is considered. Note that, this is not a limitation of the model and the effect from any number of subbands can be included. The step like behavior of C_g is due to the 2D DOS appearing in C_Q . This also shows that for low effective mass material C_g is mainly dictated by C_Q and hence the C_Q should be modeled accurately.

Fig. 5 shows the impact of $m_{||}^*$ on C_g for $t_{ch} = 5$ nm and $t_{ins} = 1$ nm. With decrease in the effective mass, the subband energy increases which shifts the capacitance inflection points towards the higher V_G values. Moreover with lower effective mass, C_Q decreases and its impact on total C_g is more pronounced (due to series combination of C_{ins} and C_Q) and hence overall C_g also decreases. Therefore, it is extremely important that the model should be efficient enough to capture the effect of quantum capacitance in low effective mass regime.

IV. CONCLUSION

To summarize, we have presented a compact model of semiconductor charge and quantum capacitance for transistors with low DOS III-V channel materials. It is shown that for future III-V FETs quantum capacitance plays an important role in deciding the total gate capacitance and the proposed model accurately captures this effect. The proposed model also has the flexibility to include the effect of non-parabolicity in the band structure. The model is simple, explicit and computationally efficient which is desired for SPICE simulators. The accuracy of the model is also verified by comparing it with the numerical simulation data for different channel thickness and in-plane effective mass.

REFERENCES

[1] S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling 20-nm germanium FinFET with the industry standard FinFET model," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 711–713, Jul. 2014.

[2] Y. Sun *et al.*, "High-performance CMOS-compatible self-aligned $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ MOSFETs with GMSAT over $2200 \mu\text{s}/\mu\text{m}$ at $V_{DD} = 0.5 \text{ V}$," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2014, pp. 25.3.1–25.3.4.

[3] S. Yadav *et al.*, "First monolithic integration of Ge p-FETs and InAs n-FETs on silicon substrate: Sub-120 nm III-V buffer, sub-5 nm ultrathin body, common raised S/D, and gate stack modules," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2015, pp. 2.3.1–2.3.4.

[4] G. Fiori and G. Iannaccone, "The challenging promise of 2D materials for electronics," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2015, pp. 27.1.1–27.1.4.

[5] N. Taoka *et al.*, "Impact of fermi level pinning inside conduction band on electron mobility of $\text{In}_x\text{Ga}_{1-x}\text{As}$ MOSFETs and mobility enhancement by pinning modulation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2011, pp. 27.2.1–27.2.4.

[6] J. A. D. Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.

[7] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.

[8] C. Zhang and X. Li, "III-V nanowire transistors for low-power logic applications: A review and outlook," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 223–234, Jan. 2016.

[9] R. Kim, U. E. Avci, and I. A. Young, "CMOS performance benchmarking of Si, InAs, GaAs, and Ge nanowire n- and pMOSFETs with $L_g=13 \text{ nm}$ based on atomistic quantum transport simulation including strain effects," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2015, pp. 34.1.1–34.1.4.

[10] V. Deshpande *et al.*, "Advanced 3D monolithic hybrid CMOS with sub-50 nm gate inverters featuring replacement metal gate (RMG)-InGaAs nFETs on SiGe-OI fin pFETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2015, pp. 8.8.1–8.8.4.

[11] M. K. Hudait *et al.*, "Heterogeneous integration of enhancement mode $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ quantum well transistor on silicon substrate using thin ($2 \mu\text{m}$) composite buffer architecture for high-speed and low-voltage (0.5 v) logic applications," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 2007, pp. 625–628.

[12] M. L. Huang *et al.*, " $\text{In}_{0.53}\text{Ga}_{0.47}$ MOSFETs with high channel mobility and gate stack quality fabricated on 300 mm Si substrate," in *Proc. IEEE Symp. VLSI Technol.*, Kyoto, Japan, 2015, pp. T204–T205.

[13] V. Djara *et al.*, "CMOS-compatible replacement metal gate InGaAs-OI FinFET with $I_{ON}=156 \mu\text{A}/\mu\text{m}$ at $V_{DD}=0.5 \text{ V}$ and $I_{OFF}=100 \text{ nA}/\mu\text{m}$," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 169–172, Feb. 2016.

[14] J. P. Colinge, "Multi-gate SOI MOSFETs," *Microelectron. Eng.*, vol. 84, nos. 9–10, pp. 2071–2076, 2007.

[15] S.-I. Takagi and A. Toriumi, "Quantitative understanding of inversion-layer capacitance in Si MOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 12, pp. 2125–2130, Dec. 1995.

[16] A. Hartstein and N. Albert, "Determination of the inversion-layer thickness from capacitance measurements of metal-oxide-semiconductor field-effect transistors with ultrathin oxide layers," *Phys. Rev. B*, vol. 38, no. 2, pp. 1235–1240, 1988.

[17] S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, no. 6, pp. 501–503, 1988.

[18] D. Jin, D. Kim, T. Kim, and J. del Alamo, "Quantum capacitance in scaled down III–V FETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Baltimore, MD, USA, Dec. 2009, pp. 1–4.

[19] S. Oh and H.-S. Wong, "Physics-based compact model of III–V heterostructure FETs for digital logic applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2008, pp. 1–4.

[20] S. Mudanai, A. Roy, R. Kotlyar, T. Rakshit, and M. Stettler, "Capacitance compact model for ultrathin low-electron-effective-mass materials," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4204–4211, Dec. 2011.

[21] C. Yadav *et al.*, "Capacitance modeling in III–V FinFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3892–3897, Nov. 2015.

[22] Y. S. Chauhan *et al.*, "BSIM6: Analog and RF compact model for bulk MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 234–244, Feb. 2014.

[23] Y. S. Chauhan *et al.*, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. London, U.K.: Academic Press, 2015.

[24] R. Eisberg and R. Resnick, *Quantum Physics of Atoms, Molecules, Solids, Nuclei, and Particles*. New York, NY, USA: Wiley, 1974.

[25] B. P. Yang, B. Epler, and P. K. Chatterjee, "An investigation of the charge conservation problem for MOSFET circuit simulation," *IEEE J. Solid-State Circuits*, vol. 18, no. 1, pp. 128–138, Feb. 1983.

[26] Y. Liu, N. Neophytou, G. Klimeck, and M. S. Lundstrom, "Band-structure effects on the performance of III–V ultrathin-body SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1116–1122, May 2008.

[27] G. Hibliot, G. Mugny, Q. Raffhay, F. Boeuf, and G. Ghibaudo, "Compact model for inversion charge in III–V bulk MOSFET including non-parabolicity," *IEEE Trans. Nanotechnol.*, vol. 14, no. 4, pp. 768–775, Jul. 2015.

[28] V. A. Altschul, A. Fraenkel, and E. Finkman, "Effects of band non-parabolicity on two-dimensional electron gas," *J. Appl. Phys.*, vol. 71, no. 9, pp. 4382–4384, 1992.

[29] A. Ali *et al.*, "Experimental determination of quantum and centroid capacitance in arsenide-antimonide quantum-well MOSFETs incorporating nonparabolicity effect," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1397–1403, May 2011.

[30] S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge, U.K.: Cambridge Univ. Press, 2005.



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