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Energy-Saving Write/Read Operation of Memory Cell by Using Separated Storage Device and Remote Reading With an MIS Tunnel Diode Sensor

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ABSTRACT An efficient way to reduce the loss of stored charge in a memory cell was proposed in this paper. Conventionally, the storage structure is stressed by applying voltages during the read operation. By structurally separating the read operation from the storage structure, lower disturbance to the stored charge can be expected. The metal–insulator–semiconductor (MIS) tunnel diode (TD) sensor was the proposed device for the read operation. The saturation current of the MIS TD can be exponentially affected by the remote stored charge. By comparing the write and read operations of the proposed memory cell with the conventional flash memory cell, it is believed that the proposed cell needs lower voltage to be applied within a read/write cycle, i.e., more energy-saving than the conventional cell.

INDEX TERMS Energy saving, write/read operation, retention time improvement, MIS tunnel diode.

I. INTRODUCTION

For conventional charge-storage memories like dynamic random access memory (DRAM), flash (floating gate) memory, and floating trap (SONOS) memory, one of the major charge loss mechanisms is that the storage device suffers from voltage stress during read operation [1], [2]. Therefore, if the read operation was structurally separated from the storage structure, the disturbance of the read voltage could be reduced, and less charge would be lost. The separated structure for read operation proposed in this work was the metal-insulator-semiconductor (MIS) tunnel diode (TD). The MIS TD is a metal-oxide-semiconductor structure with thin tunnel oxide. The saturation current of the MIS TD, $I_{TD,sat}$, is exponentially dependent on the effective Schottky barrier height of majority carriers, ϕ_h^*, i.e., [3]

$$I_{TD,sat} = A^* A_{eff} P_t T^2 \exp\left(-q\phi_h^*/kT\right) \quad (1)$$

where A^* is the effective Richardson constant, A_{eff} is the effective area that the current flows through, and P_t is the oxide-tunneling probability. Fig. 1 shows the measured current-voltage characteristics of p-type MIS TD's with various oxide thicknesses, d_{ox}'s. The inset shows the MIS TD

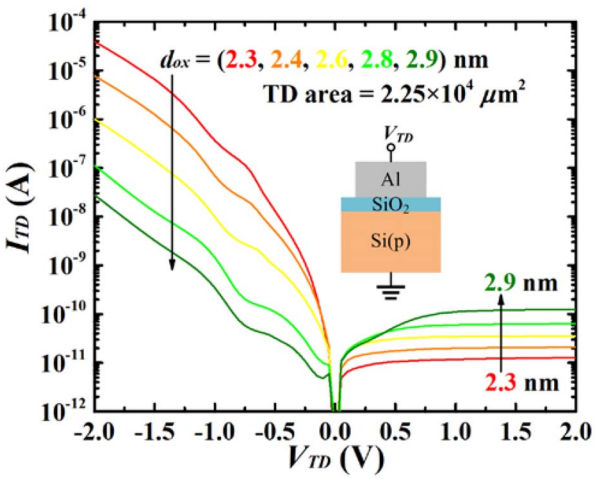

FIGURE 1. The measured current-voltage characteristics of p-type MIS TD's with various oxide thicknesses. The inset shows the MIS TD structure (Al/SiO_2/Si(p)).

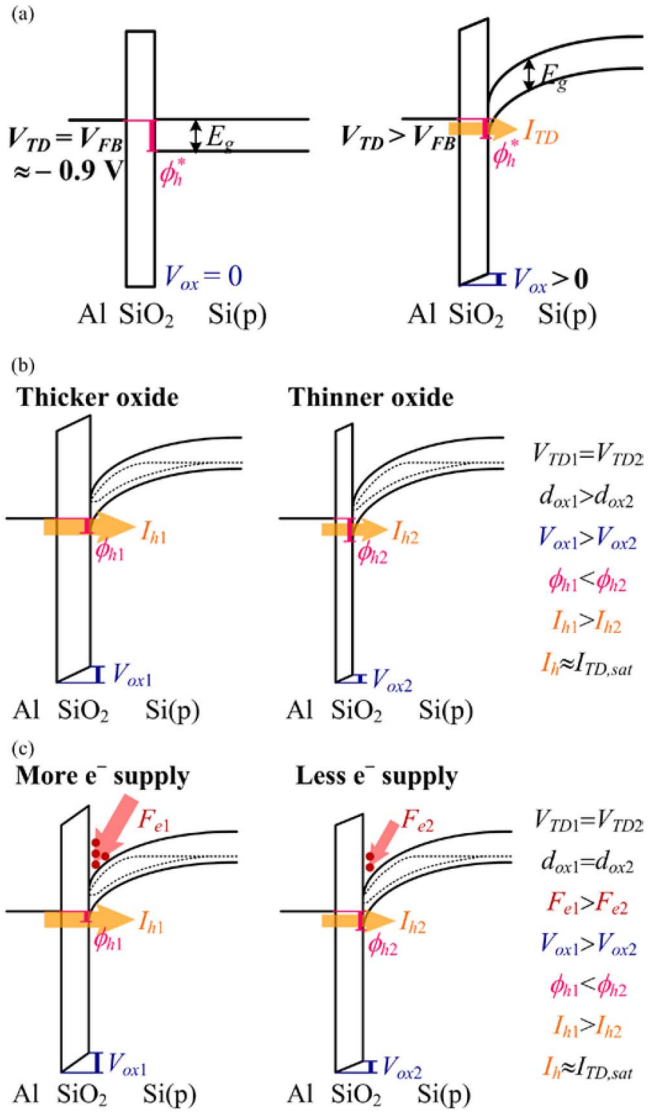

FIGURE 2. **(a) The band diagrams of p-type MIS TD's at flat-band ($V_{TD} = V_{FB}$) (left) and $V_{TD} > V_{FB}$ (right). (b) The band diagrams of p-type MIS TD's with thicker oxide (left) and thinner oxide (right). I_h is the hole current. $I_{TD,sat} \approx I_h$. (c) The band diagrams of p-type MIS TD's while the lateral electron flux is large (left) and small (right).**

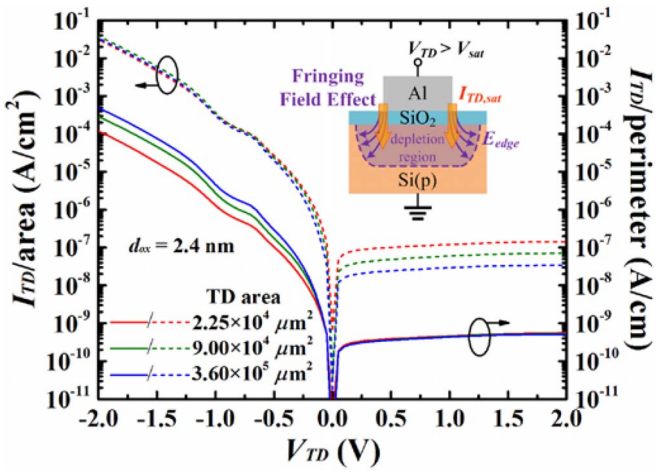

FIGURE 3. **The measured current-voltage characteristics of MIS TD's with various device areas. The dotted lines are the currents per unit device area, and the solid lines are the currents per unit device perimeter. The inset shows that the saturation current of MIS TD is mainly flowing through the edge of the device due to the fringing field effect. E_{edge} is the fringing electric field.**

structure (Al/SiO_2/Si(p)). It can be seen that the saturation current at positive bias increases abnormally with d_{ox}. It is because that the oxide voltage drop, V_{ox}, is larger for thicker oxide, and the ϕ_h^* is smaller as V_{ox} is larger, i.e., [3]

$$q\phi_h^* = q\chi_s - q\Phi_m + E_g - qV_{ox} \tag{2}$$

where $q\Phi_m$ and $q\chi_s$ are the work function of gate metal and the electron affinity of semiconductor, respectively, and E_g is the bandgap of semiconductor. The equation (2) can be illustrated by the band diagrams shown in Fig. 2(a). It is known that the V_{ox} is larger for larger d_{ox} under a certain gate voltage, and hence the saturation current increases with d_{ox} according to equations (1) and (2). The mechanism is illustrated by the band diagrams of thicker and thinner oxide as shown in Fig. 2(b). The phenomenon also had been discovered and used as the Schottky contact resistance reduction technique [4]–[7]. Note that as $V_{TD} > V_{sat}$, where V_{sat} is the voltage that current saturates, the V_{ox} doesn't increase with V_{TD} because the oxide-tunneling rate is so large that the excess inversion charges cannot be held at the silicon surface but tunnel to the metal, and the excess gate voltage drops on the silicon substrate, i.e., the depletion width increases with V_{TD}, which is a kind of deep depletion effect [8]. That explains the rectifying characteristics of the MIS TD. Also note that the V_{sat} increases with d_{ox} because larger voltage drop on oxide is needed for thicker oxide to reach the saturation point. Another feature of the MIS TD is the device-perimeter dependency of the $I_{TD,sat}$ when the ϕ_h^* is large enough that the $I_{TD,sat}$ is dominated by the Schottky emission current. Fig. 3 shows the measured current-voltage characteristics of MIS TD's with various device areas. It can be seen that the $I_{TD,sat}$ is proportional to the device perimeter. Since the electric field at device edge is larger due to the fringing field effect, the V_{ox} at device edge is larger, and hence the $I_{TD,sat}$ at the device edge is far larger than that in the interior of device according to equations (1) and (2). The inset in Fig. 3 depicts that the saturation current of MIS TD is mainly flowing through the edge of the device due to the fringing field effect. Besides the fringing field effect, it was found that the ϕ_h^* can be affected by the lateral diffusion current of minority carriers at the device edge [9], [10]. The ϕ_h^* relates to the lateral diffusion current of minority carriers, $J_{e,diff}$, as [9]

$$\phi_h^* = \phi_{h0} - \Delta\ \phi_h \tag{3a}$$

$$\Delta\phi_h = BJ_{e,diff}d_{ox} = BqF_e d_{ox} \tag{3b}$$

where B is a constant, ϕ_{h0} is the Schottky barrier height of holes without considering the effect of lateral diffusion current, $\Delta\phi_h$ is the lowering of Schottky barrier height related

to the $J_{e,diff}$ and the oxide thickness of the TD, and F_e is the lateral flux of minority carriers from outside of the TD to the edge of TD. The larger the F_e, the lower the ϕ_h^*. The mechanism is illustrated by the band diagrams of larger and smaller F_e's as shown in Fig. 2(c). It was demonstrated that the lateral diffusion current can be controlled by a remote gate [3], [11]. The gate controlled minority concentration determines the minority carrier concentration profile between the gate and the TD, which also determines the gradient of minority carrier concentration at the edge of TD, i.e., the F_e. Therefore, the higher the inversion level, the larger the F_e, and the larger the $I_{TD,sat}$. The schematic mechanism is illustrated in Fig. 4. In this work, the gate serves as the charge-storage structure. After the write/erase voltage stress is applied, the inversion charges under the gate were induced by the charges stored in the gate dielectric stack, i.e., floating traps. Different charges were stored after various gate voltage stresses, which induced different inversion levels. The inversion levels were sensed by the neighboring MIS TD by detecting the lateral flux of minority carriers at the edge of TD. Different saturation current levels of the MIS TD were therefore read, i.e., different memory states were read by the MIS TD. In contrast with the read operation of conventional memories, the proposed read operation in this work would obtain the lower charge loss since the storage structure was immune to the read voltage stress.

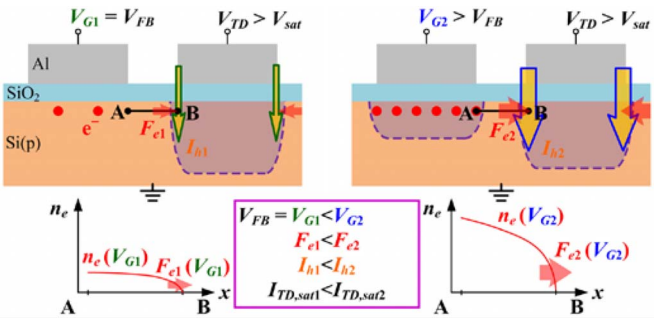

FIGURE 4. The schematic operations of gated-MIS TD as the gate was biased at flat-band ($V_G = V_{FB}$) (left) and $V_G > V_{FB}$. n_e is the minority carrier concentration along the cross section AB.

II. EXPERIMENTAL

A boron-doped 1–10 Ω-cm (100) silicon wafer was used as the substrate. After standard Radio Corporation of America (RCA) clean, a SiO_2 layer was grown on the wafer by anodization [12], [13] in deionized (DI) water at room temperature. Then, a rapid thermal process in N_2 ambient at 950 °C for 15 s was implemented. Then, a Hf film was sputtered and oxidized by the nitric acid (HNO_3:H_2O = 1:1) to form the HfO_2 layer. Then, an Al film was thermally evaporated and oxidized by the nitric acid (HNO_3:H_2O = 1:1) to form the Al_2O_3 layer. The equivalent oxide thickness (EOT) of the gate dielectric stack (Al_2O_3/HfO_2/SiO_2) is 4 nm. Then, an Al film with a thickness of 200 nm was deposited by thermal evaporation and was defined by lithography and

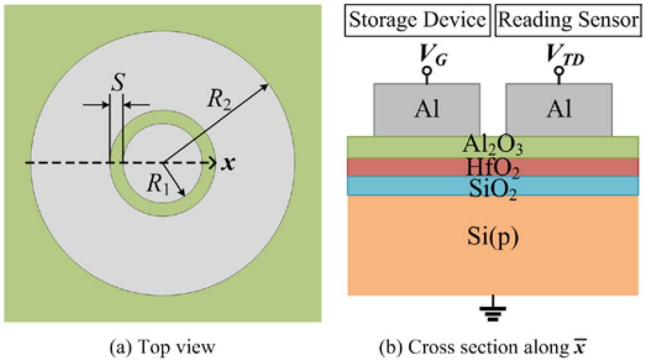

FIGURE 5. Schematic (a) top view and (b) cross section of the gated-MIS TD.

wet etching to form the top electrodes. The device pattern consists of an inner circle and a concentric ring. The inner circle structure serves as the MIS TD, and the concentric ring structure serves as the gate/charge-storage structure. The top view and the cross section of the device are shown in Fig. 5(a) and Fig. 5(b), respectively. The radius of the inner circle, R_1, is 83.6 μm. The space width between circle and ring, S, is 7.6 μm. The outside radius of the ring, R_2, is 576.1 μm. Finally, after removing the back native oxide, an Al film with a thickness of 200 nm was thermally evaporated at the back of the substrate as back electrode.

III. RESULTS AND DISCUSSION

Fig. 6(a) shows the measured current-voltage (I_{TD} vs. V_{TD}) characteristics of the MIS TD as the gate is at fresh, after the write voltage stress ($V_G = -2.5$ V, 100 s), and after the erase voltage stress ($V_G = +3.0$ V, 100 s). Distinct set and reset state currents were read by the MIS TD after the write and erase processes. Fig. 6(b) shows the measured gate capacitance, C_G,-voltage curves after the write and erase processes. Distinct flat-band voltage shift is observed. It can be seen that more electrons were trapped in the gate oxide at the set state than that at the reset state. It is noted that the stored electrons were mainly injected from the metal through Al_2O_3 to HfO_2 during setting, i.e., $V_G = -2.5$ V, in this work. However, the dielectric structure or materials can be properly designed to inject electrons from the substrate through SiO_2 to HfO_2 during setting ($V_G > 0$) as conventional set process. Also note that the oxide stored charges after the write and erase processes can't be accurately extracted from the flat-band voltage shift since the charges might be affected during the C_G-V_G measurement.

After the write and erase processes performed on the gate, two read operations were demonstrated. One was sensing the charges by the MIS TD, i.e., applying the read voltage on the MIS TD while the gate was floating, as shown in Fig. 7(a). Another one was reading the charge state by the gate itself, i.e., applying the read voltage on the gate, as shown in Fig. 7(b). Fig. 7(a) shows the retention of the set and reset current states read at $V_{TD} = 3$ V. The decay behavior at the beginning of the set state is the transient

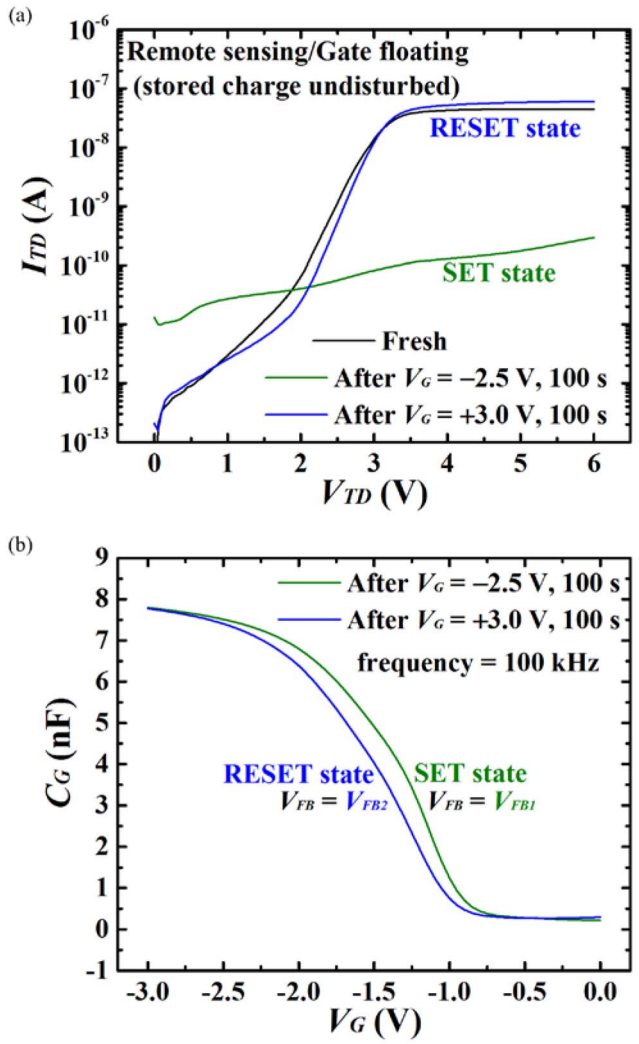

FIGURE 6. **(a) The measured current-voltage characteristics of the MIS TD as the gate is at fresh, after the write voltage stress (V_G = −2.5 V, 100 s), and after the erase voltage stress (V_G = +3.0 V, 100 s). (b) The measured gate capacitance, C_G,-voltage curves at 100 kHz after the write and erase processes.**

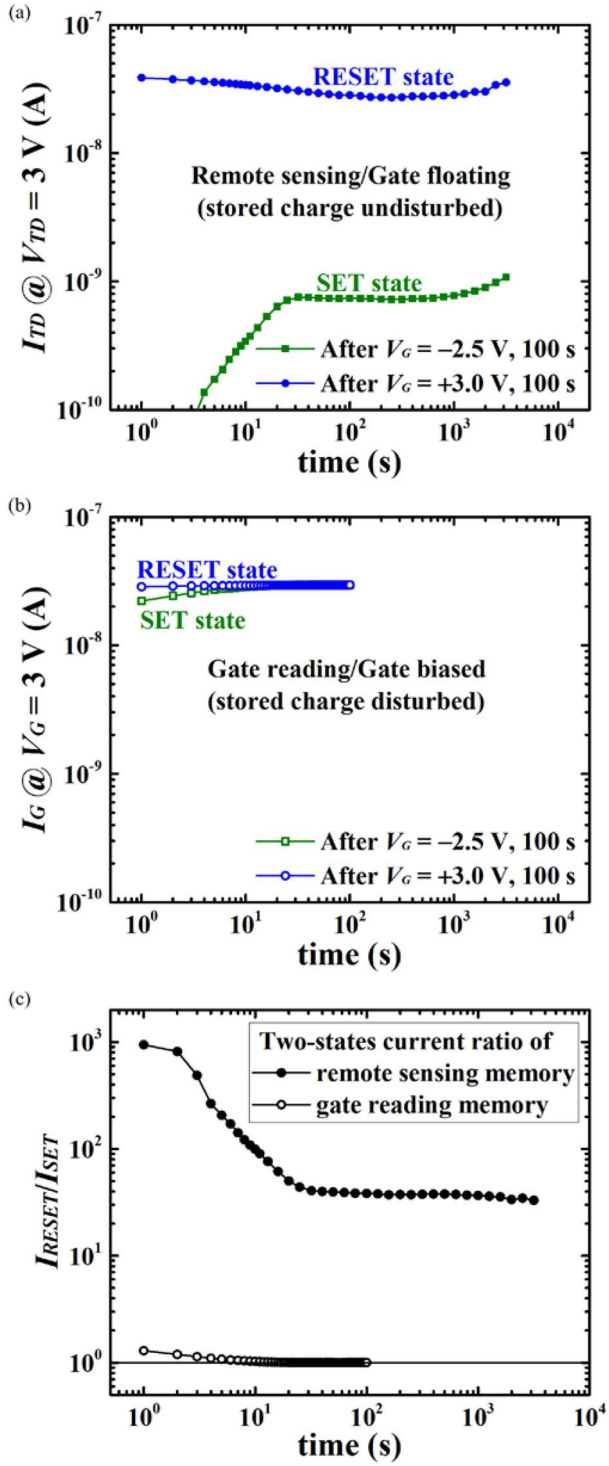

FIGURE 7. **The measured retention of the set and reset current states read at (a) V_{TD} = 3 V and (b) V_G = 3 V. (c) The extracted current ratios of set and reset states in (a) and (b).**

behavior. Fig. 7(b) shows the retention of the set and reset current states read at $V_G = 3$ V. The set state decayed much fast owing to the charge loss during the read operation. The retention time is far longer in Fig. 7(a) than that in Fig. 7(b) since the stored charges were nearly undisturbed during the read voltage stress in Fig. 7(a). Fig. 7(c) shows the current ratios of set and reset states extracted from Fig. 7(a) and Fig. 7(b).

Fig. 8 illustrates the mechanism of the read processes in Fig. 7(a). After the gate was set ($V_G = -2.5$ V, 100 s), electrons trapped in the gate oxide and less inversion charges were induced. Therefore, the lateral electron flux at the edge of MIS TD was small, and hence the read current, $I_{TD,sat}$, was small. After the gate was reset ($V_G = +3.0$ V, 100 s), the trapped electrons in the gate oxide were removed and larger inversion charges were induced. Therefore, the lateral electron flux at the edge of MIS TD was large, and hence the read current was large.

In the future work, the oxide of MIS TD can be replaced with a single SiO_2 layer instead of high-k materials since

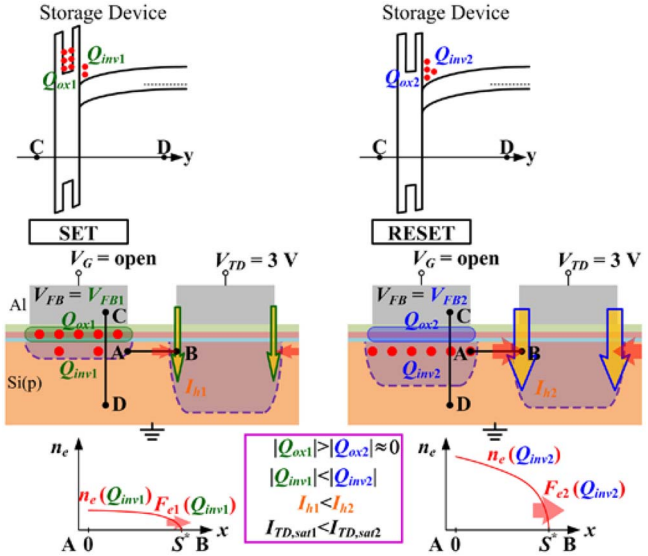

FIGURE 8. **The schematic diagrams of the read mechanism in Fig. 9(a). Left: the read process after the gate was set ($V_G = -2.5$ V, 100 s). Right: the read process after the gate was reset ($V_G = +3.0$ V, 100 s). $x = S^*$ is the position at the depletion edge of the MIS TD.**

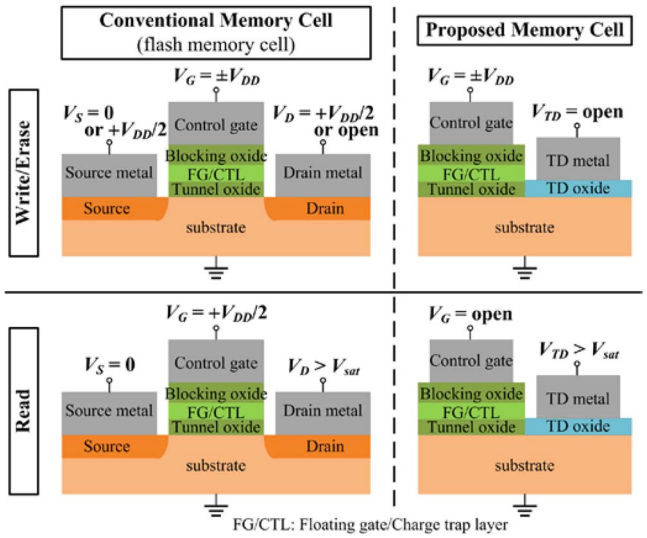

FIGURE 9. **The schematic diagrams that compares the applied voltages of write/erase and read operations of the conventional flash memory cell with that of the memory cell with MIS TD sensor proposed in this work.**

TABLE 1. **Comparison of the performance between conventional flash memory cell and the proposed memory cell.**

	Conventional flash memory cell	Proposed memory cell
Reading time	☺	
Writing time	-	-
Write/Erase leakage	-	-
Read leakage		☺
Retention		☺
Endurance		☺

The symbol "☺" represents "better" and the symbol "-" represents "the same".

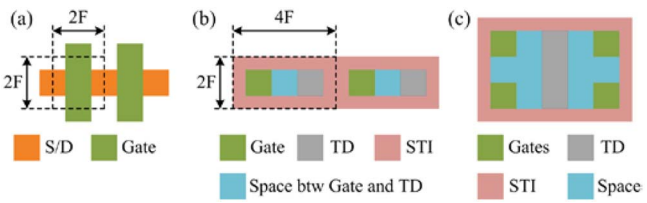

FIGURE 10. **(a) The layout of conventional NAND flash memory cells. (b) The compact layout of proposed memory cells. (c) The layout of the proposed memory cell with multi-gate structure (four gates are illustrated as an example).**

the saturation current depends on the physical oxide thickness but not the equivalent oxide thickness, i.e., the P_t in equation (1) depends on the physical oxide thickness. The charge-storage structure can be replaced by the ONO or floating gate structure to enhance the charge-trapping stability. The read voltage can be scaled down as scaling down the oxide thickness of the MIS TD since the V_{sat} decreases with the oxide thickness as described in the introduction. However, as described in the introduction, the read current, i.e., the saturation current of the MIS TD, decreases with decreasing oxide thickness. Therefore, there is a trade-off between decreasing the read voltage and increasing the read current while designing the oxide thickness of the MIS TD. The proposed read operation can be applied to any charge-storage memory. The comparison of the operations between the conventional memory cell and the proposed cell with MIS TD sensor is shown in Fig. 9. It can be seen that lower voltage is needed to be applied to the proposed cell in a read/write cycle. Therefore, more energy could be saved by applying the read operation proposed in this work. Table 1 shows the comparison of several performance aspects between the conventional flash memory cell and the proposed memory cell. The writing time and write/erase leakage (leakage current density during write/erase process) are the same between them because the voltages applied on the charge-storage structures during the write/erase processes are similar. The reading time of the conventional flash memory cell is better due to the larger read current. The read leakage, retention, and endurance of the proposed memory cell are better due to the lower charge loss during read process. Fig. 10(a) and (b) shows the layouts of conventional NAND flash memory cells and proposed memory cells with the most compact form, assuming the substrate is commonly contacted. The shallow trench isolation (STI) is used for the isolation between the cells. F is the minimum feature size of each process generation. The cells of the conventional NAND flash are connected in series that the source/drain (S/D) contact pads between the cells are not needed. By contrast, the proposed memory cells cannot be connected in series. Therefore, the minimum cell size of the proposed memory cell ($8F^2$) is supposed to be larger than that of the conventional NAND flash cells ($4F^2$). However, the multi-level memory could be realized in the proposed memory cell by using the multi-gate structure shown in

Fig. 10(c) by sensing multiple memory states with a single MIS TD, which could save more footprint areas if properly designing the arrangement. In short, the advantages of the proposed cell are lower read leakage, better retention, and better endurance. The disadvantages are longer reading time and larger footprint.

IV. CONCLUSION

An energy-saving read operation of charge-storage memories was proposed in this work. By replacing the conventional read operation with an MIS TD as the memory-states sensor at the charge-storage structure, the effect of stress on the stored charge due to conventional read operation could be greatly reduced. The retention characteristic of the storage device with MIS TD sensor was demonstrated that it is far better than the one without the sensor due to the immunity to the read voltage stress. In contrast to the conventional memory operations, the proposed cell with the MIS TD sensor needs lower voltage to be applied in a read/write cycle, and hence it is more energy-saving. Furthermore, multi-level memory could be easily realized by sensing various stored charges in multiple gates with a single MIS TD.

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