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A Perspective on SOI Symmetric Lateral Bipolar Transistors for Ultra-Low-Power Systems

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ABSTRACT The reasons why state-of-the-art vertical bipolar circuits dissipate very high power are explained. The recent advent of SOI symmetric lateral bipolar transistors invites us to rethink bipolar as a high-speed but low-power technology. Integrated Injection Logic (I^2L) and complementary bipolar (analogous to CMOS) circuits in SOI lateral bipolar offer huge design windows for power versus performance tradeoff, suggesting the possibility of ultra-low-power systems with embedded high-speed cores. I^2L SRAM cells could be more than twice as dense as CMOS SRAM cells. The SOI substrate offers a fourth device terminal that can be used to induce narrow-gap-base HBT-like *I–V* characteristics, which should further improve the power-performance of circuits in SOI lateral bipolar. Fin-structure devices enable significant improvement in $f_{\max}$ for RF and high-frequency applications. The process technology for SOI lateral bipolar is compatible with CMOS. The Si-OI version is definitely much less complex than CMOS.

INDEX TERMS Bipolar transistors, high-performance bipolar, SOI lateral bipolar, ultra-low-power bipolar.

I. INTRODUCTION

Before switching to CMOS as the logic technology for building high-speed computers, IBM and its competitors used vertical bipolar transistors to build high-end computers. Figure 1 illustrates the device structure used [1]. Its salient features include polysilicon emitter which enables scaling the base width to sub-100 nm, emitter-base self-alignment and deep and shallow trench isolation for device size and capacitance reduction, and self-aligned heavier-doped intrinsic-collector region for further speed improvement [2]–[5].

After switching from bipolar to CMOS, IBM soon adopted SOI CMOS for building all its computers. Bipolar became a niche technology for RF and analog applications. The device structure evolved to that illustrated in Fig. 2, with epitaxially grown SiGe base layer. With a graded Ge profile in its base layer, the transistor has larger current gain and Early voltage, and reduced base transit time [6].

Digital bipolar circuits using vertical transistors are fast, with circuit delays reaching sub-5 ps [7]. However, the large power dissipation makes vertical bipolar circuits not suitable for VLSI applications. That is the main reason bipolar disappeared from the VLSI scene more than twenty years ago.

Recently, there appeared an opportunity to completely revitalize bipolar in the form of symmetric lateral device structures on SOI [8], [9]. This novel device structure is illustrated in Fig. 3. It is CMOS compatible and scales in lateral dimensions like CMOS. In terms of circuits and systems, this novel bipolar device shows promise of greatly improving the power-performance of traditional bipolar circuits as well as enabling novel bipolar circuits [8]–[11].

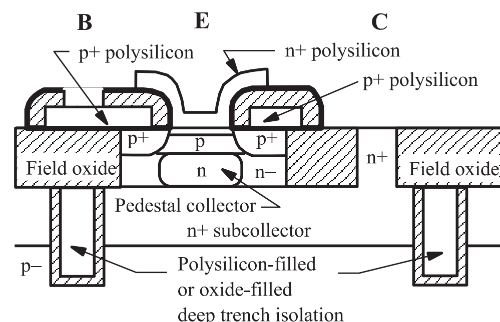

FIGURE 1. Schematic illustrating cross section of typical vertical bipolar device structure used to build high-speed computers.

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In this paper, we first examine why vertical bipolar circuits dissipate such large power. Then we discuss how the novel SOI lateral bipolar avoids the power problems associated with vertical bipolar. The merits of SOI lateral bipolar for ultra-low-power applications are also discussed.

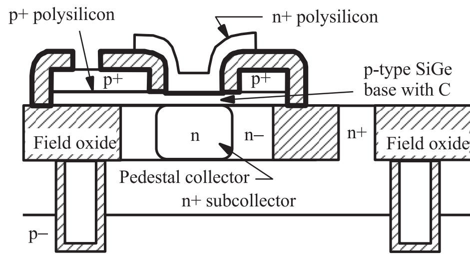

FIGURE 2. Schematic illustrating cross section of typical state-of-the-art SiGe HBT for RF and analog applications.

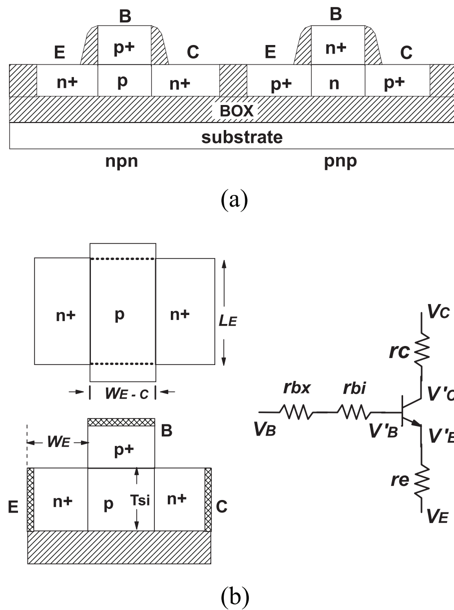

FIGURE 3. (a) Schematic illustrating the integration of symmetric lateral NPN and PNP transistors on SOI. (b) Schematic of an NPN device's top view (top left) and cross sectional view (bottom left), and device parasitic resistances and junction and terminal voltages (right) for modeling purposes. (After [9]).

II. WHY VERTICAL BIPOLAR DISSIPATES SO MUCH POWER

Figure 4 shows typical measured f_T and CML (current-mode logic) gate delay for state-of-the-art vertical SiGe HBT. (See Fig. 5 for a typical CML gate schematic.) As the transistors are driven to higher currents, the transistor speed (indicated by f_T) and circuit speed increase. However, once the current exceeds some critical level, the transistor and circuit speeds decrease rapidly as current is increased further. The decrease in speed is due to base push out (Kirk effect), where the base widens into the lightly doped collector. The speed of a vertical transistor is not limited by its base width in standby, but by the minority charge stored in the collector at high currents.

A. LIMITED CURRENT CAPABILITY AND LARGE DEVICE AREA

The current-carrying capability, i.e., the maximum collector current I_C without performance degradation, of a vertical transistor is determined by its collector doping profile. The f_T data in Fig. 4 suggest that the transistor should not be operated with I_C greater than 2 mA. A circuit requiring larger I_C should use a transistor with proportionately larger emitter area A_E. The CML data in Fig. 4 clearly show that the maximum circuit speed can be increased by using transistors with larger A_E.

Here lies one fundamental issue with vertical transistors. For a given device design, A_E must be large enough to deliver the current required to achieve the speed target. Larger A_E means larger device area and associated capacitances, which in turn imply larger power dissipation for the circuit.

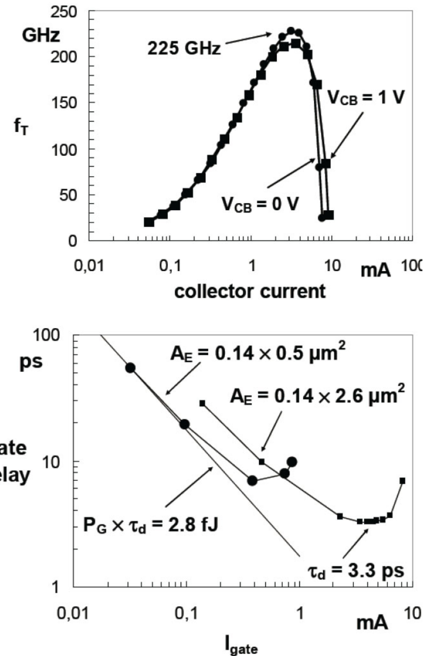

FIGURE 4. Typical measured f_T as a function of collector current (top) and CML circuit delay as a function of gate current (bottom) for vertical SiGe HBTs. The emitter area for f_T measurement was 0.14 × 2.6 μm^2. (After [7]).

B. LARGE POWER SUPPLY VOLTAGE

A standard practice in designing vertical bipolar circuits is to avoid the transistors going into saturation (collector-base diode being forward biased) in operation. Most bipolar circuits employ resistors as loads. Figure 5 shows a basic resistor-load inverter and a commonly used CML gate. The *IR* drop across a load resistor tends to drive the transistor connected to the load towards saturation. The simplest way to avoid saturation is to increase the power supply voltage V_{cc}. For the basic inverter, it can readily be shown that for a given logic swing ΔV, the minimum V_{cc} is ΔV if saturation is not an issue. V_{cc} is $2\Delta V$ if saturation is to be

avoided completely. Designers typically use V_{cc} larger than "the minimum required for circuit functionality" to avoid transistors going into saturation. This leads to larger power dissipation for the circuits.

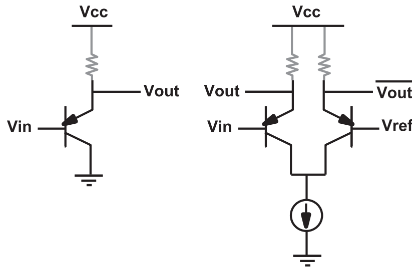

FIGURE 5. Circuit schematics of a bipolar inverter with resistor load (left) and a CML gate (right).

C. NO HIGH-SPEED CIRCUITS WITH $V_{CC} = V_{BE}$

The minimum V_{cc} for a bipolar circuit is the V_{BE} needed to deliver the desired collector currents. However, a circuit operating with $V_{cc} = V_{BE}$ puts the transistors in full saturation during operation. Many vertical bipolar circuits can operate with $V_{cc} = V_{BE}$ if speed is not important. For example, I^2L (Integrated Injection Logic) or MTL (Merged Transistor Logic) circuits [12], [13] are very simple and dense, and operate with $V_{cc} = V_{BE}$. They were actually the most popular low-cost and low-power LSI technology for several years, competing favorably with CMOS. However, with transistors operating in full saturation, the speed of vertical bipolar I^2L was simply not competitive compared to scaled CMOS.

When the base-collector diode is forward biased, minority carriers are stored in the base-collector diode regions. For a vertical transistor, most of the carriers are stored on the collector side which is more lightly doped than the base. ($N_B > 10$x N_C for a typical vertical transistor.) Referring to the inverter in Fig. 5, to turn off the inverter, i.e., to bring Vout from ground towards V_{cc}, Vout would not rise appreciably until all the minority carries in the collector have been drained off. The inverter speed is limited not by the device base width, but by the amount of stored charge in the collector region.

The idea of complementary bipolar (CBipolar) circuits, analogous to CMOS, was proposed a long time ago [14]. CBipolar circuits also operate with $V_{cc} = V_{BE}$. Vertical CBipolar was never developed because they would be far inferior to CMOS in speed and power dissipation.

III. WHAT MAKES SOI SYMMETRIC LATERAL BIPOLAR A LOW-POWER TECHNOLOGY

It is evident from Figs. 1-3 that a lateral transistor has large layout and density advantages over a vertical transistor. Such advantages translate readily into reduction in device and wiring capacitances, and hence reduction in power dissipation at the circuit/chip level. In this section, we discuss several less obvious reasons why SOI symmetric lateral bipolar is an ideal low-power bipolar technology.

A. HIGH CURRENT-CARRYING CAPABILITY

Figure 6 shows the measured currents for a typical Si-OI NPN transistor [15]. It shows a maximum current of about 5 mA/µm. Let us focus on the modeled currents assuming $r_e = r_{bx} = 0$ (dash lines). At $V_{BE} > 1.0$ V, I_B increases more slowly than $\exp(qV_{BE}/kT)$ due to intrinsic-base resistance, which is inherent in a transistor. I_C increases with V_{BE} even more slowly than I_B due to high-injection effect in the base [15].

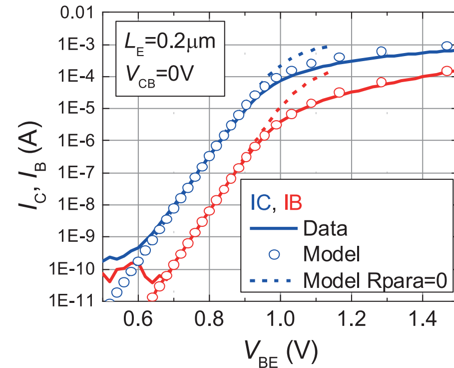

FIGURE 6. Base and collector currents of a typical Si-OI symmetric lateral NPN device. The device has T_{si} = 60 nm, N_B = 2.5E18/cm^3, and $N_E = N_C$ = 4E20/cm^3 formed by As implantation. Extracted W_B is about 10.3 nm. The modeled currents were calculated using measured r_e = 267 Ω. W_E is 48.5 nm extracted from fitting I_B (see Fig. 3 for transistor equivalent circuit and model parameters). Dash lines show calculated intrinsic device currents with no parasitic resistance. (After [15]).

With the collector more heavily doped than the base, base-push-out effect is absent in a symmetric lateral transistor. However, high-injection effect in the base, i.e., $n_p > N_B$ where n_p is the electron density in the p-type base and N_B is the base doping concentration, will cause I_C to change from an $\exp(qV'_{BE}/kT)$ dependence at small V_{BE} to an $\exp(qV'_{BE}/2kT)$ dependence at large V_{BE}. The collector current valid for all injection levels is given by [15]

$$I_C = A_E J_{C0}\left(V'_{BE}\right)\exp\left(qV'_{BE}/kT\right), \tag{1}$$

with

$$J_{C0}\left(V'_{BE}\right) = \frac{qD_{nB}n_{ieB}^2}{N_B W_B}\left[1+\frac{1}{4}\left(\sqrt{1+\frac{4n_{iB}^2\exp\left(qV'_{BE}/kT\right)}{N_B^2}}-1\right)\right]^{-1}. \tag{2}$$

When high-injection effect is appreciable, the space-charge-region widths are reduced due to the high density of mobile space charge, resulting in a larger W_B and a device speed lower than if high-injection effect were absent.

An indication of significant high-injection effect is the rapid roll off of current gain due to I_C moving towards $\exp(qV'_{BE}/2kT)$ dependence while I_B staying with

$\exp(qV'_{BE}/kT)$ dependence. Figure 7 plots the measured current gain as a function of I_C for the transistor in Fig. 6. The slow decrease in current gain at low currents is due to modulation of W_B by V_{BE}, causing a slight increase in W_B as V_{BE} is increased. It happens in bipolar transistors in general, and the effect is more pronounced in thin-base transistors [16]. The rapid decrease in current gain at large I_C is due to high-injection effect. For the device in Fig. 7, significant high-injection effect sets in when I_C exceeds about 0.6 mA, corresponding to a collector current density J_C of 50 mA/μm^2. We may consider this to be the maximum J_C without significant speed degradation for the transistor.

The current density marking the on-set of significant high-injection effect increases with N_B. By increasing N_B from 2.5E18 cm^{-3} to 1E19 cm^{-3}, and reducing W_B simultaneously to maintain a proper device design, the maximum J_C without performance degradation could be increased from 50 mA/μm^2 to about 200 mA/μm^2.

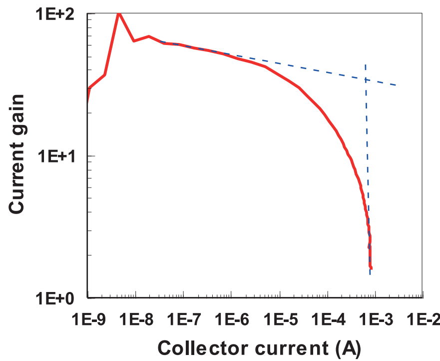

FIGURE 7. Measured current gain as a function of collector current for the NPN transistor in Fig. 6.

B. SMALL BASE-EMITTER JUNCTION AREA AND CAPACITANCE

The vertical transistors in Fig. 4 indicate a peak speed at J_C of about 9 mA/μm^2. The previous discussion suggests a lateral transistor could have peak speed at J_C of about 200 mA/μm^2. This large difference between a vertical transistor and a lateral transistor is due to the fact that N_C of a typical vertical transistor could be much smaller than N_B of a typical lateral transistor. The implication is that, for a desired value of I_C for circuit application, A_E and its associated capacitance of a lateral transistor could be $<$ 1/20 that of a vertical transistor.

C. SMALL BASE-COLLECTOR JUNCTION AREA AND CAPACITANCE

It is readily seen from Figs. 1 and 2 that the base-collector junction area A_C is much larger than A_E in vertical bipolar transistors. Depending on details of fabrication process and device design, A_C is typically 5-10x A_E. There are two capacitance components associated with the collector node of a vertical transistor, the base-collector junction capacitance and the collector-substrate junction capacitance. For a typical vertical transistor, these components are comparable to the base-emitter capacitance. For example, for the transistor with A_E of 0.14×0.26 μm^2 shown in Fig. 4, the base-emitter capacitance is 6.4 fF, the base-collector capacitance is 5.4 fF, and the collector-substrate capacitance is 3.7 fF [7]. The implication is that, just like the emitter capacitance discussed above, the collector capacitance of a lateral transistor could also be $<$ 1/20 that of a vertical transistor.

D. SMALLER-THAN-CMOS PARASITIC RESISTANCES

From the device schematics (see Fig. 3), SOI symmetric lateral bipolar looks like CMOS. However, lateral bipolar devices could have significantly smaller parasitic resistances than CMOS devices. In the case of CMOS, source and drain resistances are dominated by the source/drain "extensions" which are very shallow. In lateral bipolar devices, there are no "shallow extension" regions. The measured emitter resistance for the NPN device in Fig. 6 is 55 Ω-μm, which is about 1/4 the source/drain series resistance of a typical CMOS device.

Figure 8 compares the layout of a CMOS device with that of a lateral bipolar transistor. The two devices have the same dimension in the "width" direction. The gate metal contact is located off the channel region of a CMOS device, while the base metal contact can be located directly on top of the intrinsic base of a bipolar device. It suggests the gate resistance of a CMOS device to be larger than the extrinsic-base resistance of a lateral bipolar transistor. The resistance difference increases with device "width".

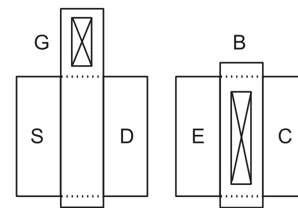

FIGURE 8. Schematics comparing the layout of a CMOS device (left) with that of a lateral bipolar transistor (right). The CMOS device has metal contact via located away from the device channel region. The metal contact to the extrinsic base of the lateral bipolar device can be located directly above the intrinsic-base region. (After [10]).

Small parasitic resistances may not be important for ultra-low-power circuits where currents are small and speeds are low. Small parasitic resistances are critically important for high-speed digital, RF and high-frequency applications.

IV. SOI LATERAL BIPOLAR FOR HIGH-SPEED CIRCUITS AT LOW POWER

The delay of a logic gate is proportional to $C\Delta V/I$, where C is the capacitance load, ΔV is the logic swing, and I is

the gate current. Consider the implementation of a bipolar circuit, e.g., CML, in both lateral transistors and in vertical transistors. The > 20x reduction in device capacitance suggest that the lateral bipolar circuit could have the same speed but at < 1/20 the power dissipation of the vertical bipolar circuit.

As discussed in Section II-B, the emitter/collector symmetry enable a lateral bipolar circuit to use a smaller V_{cc} than the same circuit in vertical bipolar. For a CML circuit, the supply voltage reduction could be larger than 30%. This reduction is on top of the reduction due to smaller capacitance.

The focus on vertical bipolar development has been towards higher f_T and $f_{\max}$ for RF and high-frequency applications. To that end, one direction has been the optimization of collector doping profile for higher f_T and $f_{\max}$ that peak at a higher J_C. In other words, the goal has been to increase the maximum J_C without performance degradation [17].

For a lateral bipolar transistor, the maximum J_C without performance degradation can be increased by increasing N_B, as discussed in Section III-A. For high-frequency applications, $f_{\max}$ can be enhanced by adopting a fin-structure, such as the one illustrated in Fig. 9. The f_T and $f_{\max}$ for a planar-structure device and a fin-structure device are compared in Fig. 10. The fin device has a longer boundary perimeter between its extrinsic base and its emitter/collector, and hence a large fringing capacitance, than the planar device. As a result, f_T of the fin device is lower than that of the planar device. The fin device has much smaller intrinsic-base resistance than the planar device, by 4x for the device in Fig. 10, resulting in significantly higher $f_{\max}$. Figure 10 shows peak $f_{\max} > 1$ THz. Adding a top contact to the intrinsic base (by removing the top insulation between the extrinsic base and the intrinsic base) could lead to further reduction of intrinsic-base resistance and hence further increase in $f_{\max}$.

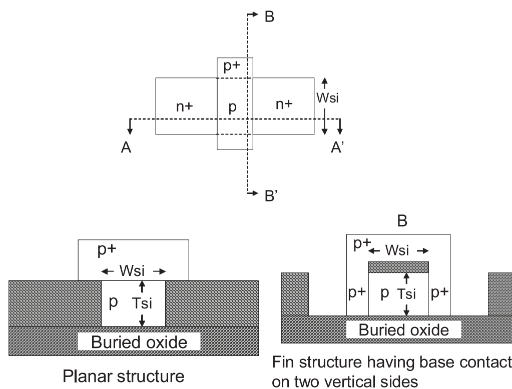

FIGURE 9. Side-view schematics of a planar-structure (bottom left) and a fin-structure (bottom right) SOI symmetric lateral bipolar transistor. For the fin-structure, the contact between the p+ extrinsic base and the p-type base can be on two sides, as illustrated here, or on three sides. The top view (top) is the same for both planar-structure and fin-structure devices.

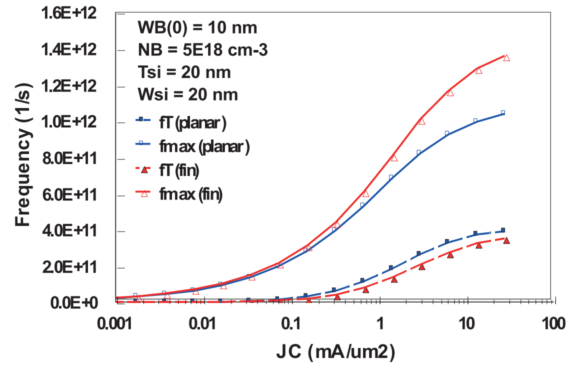

FIGURE 10. Simulated f_T and $f_{\max}$ as a function of collector current density for a planar-structure device (bottom left of Fig. 9) with extrinsic base contacting the intrinsic base only on the top surface and for a fin-structure device (bottom right of Fig. 9) with extrinsic base contacting the intrinsic base on the two vertical surfaces of the intrinsic base. The device parameters are as indicated. Low-injection approximation was assumed, i.e., the calculation is for collector currents where $n_p < N_B$.

As of this writing, there is no report of quantitative evaluation of the power reduction in designing bipolar circuits/systems using lateral transistors. Published device simulation results [18], [19] suggest that lateral devices have higher peak f_T and $f_{\max}$ compared to vertical transistors at about 100x lower current. What is needed are studies of circuits/systems quantifying the reduction in power using lateral transistors in place of vertical transistors.

V. RETHINK BIPOLAR CIRCUITS WITH $V_{CC} = V_{BE}$

Reducing V_{cc} leads directly to reducing power dissipation. The smallest V_{cc} for a bipolar circuit is one base-emitter diode voltage V_{BE}. As explained in Section II-C, a circuit that operates with $V_{cc} = V_{BE}$ requires the transistors to operate in both forward-active mode (with base-emitter diode switching) and reverse-active mode (with base-collector diode switching). Vertical bipolar transistors are very slow when operated in reverse-active mode due to the large physical volume of the lightly doped collector available for storing minority carriers. SOI symmetric lateral bipolar transistors, on the hand, are perfect for such circuits because they switch equally fast in both forward-active and reverse-active modes. In this section, we discuss two of the most interesting circuits that operate with $V_{cc} = V_{BE}$, namely I^2L and CBipolar.

A. I^2L CIRCUITS IN SOI SYMMETRIC LATERAL BIPOLAR

Figure 11 shows the schematic of an I^2L circuit with FO = 3. I^2L is by far the densest circuit. It uses minimum-size devices, and requires one PNP per gate for current injection and one NPN per fan-out. Thus a FO = 3 circuit has just four transistors. In a controlled experiment using the same vertical transistors, a divider circuit designed in I^2L is 5.6 denser than the same circuit designed in CML [20]. The main drawback of I^2L in vertical bipolar is its speed being limited to > 200 ps [20], [21], which is slow by modern CMOS standard.

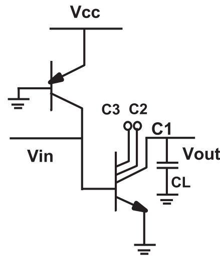

FIGURE 11. Schematic of an I^2L gate with 3 fan-outs.

When implemented in SOI symmetric lateral bipolar, I^2L should have minimum delays similar to CML. The simulated delay vs. power for an I^2L gate with FO = 3 is shown in Fig. 12. It shows minimum delays < 10 ps and a power-delay product < 100 aJ. With further scaling, a power-delay product of < 10 aJ should be possible. These results suggest I^2L in SOI lateral bipolar to be a dense and high-speed logic technology.

An I^2L SRAM cell requires only four transistors [22], [23]. In comparison, a standard CMOS SRAM cell requires six transistors. Thus one should expect an I^2L SRAM cell to be significantly denser than a CMOS SRAM cell. A sample layout of an I^2L SRAM cell in lateral bipolar is shown in Fig. 13. SRAM cell areas are best compared in terms of the half-pitch F of the wires employed to form the cell in an array. The I^2L cell in Fig. 13 has an area of $4F \times 9F = 36\ F^2$. For comparison, a 14-nm FinFET CMOS SRAM cell has an area of 73.8 F^2 [24], and a 22-nm SOI CMOS SRAM cell has an area of 90 F^2 [25]. Thus, compared to CMOS SRAM cells, I^2L SRAM cells could be more than twice as dense.

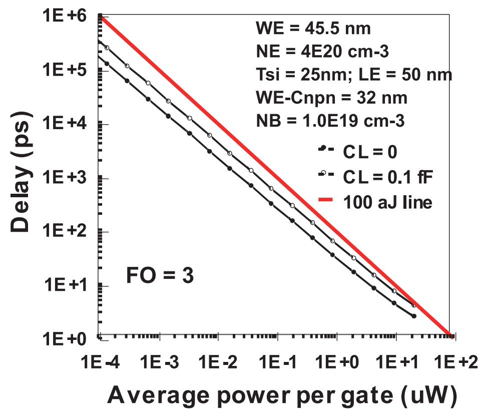

FIGURE 12. Simulated delay versus upper bound estimate of average standby power dissipation for an I^2L gate with FO = 3 (see Fig. 11). The NPN device parameters are as indicated. (After [9]).

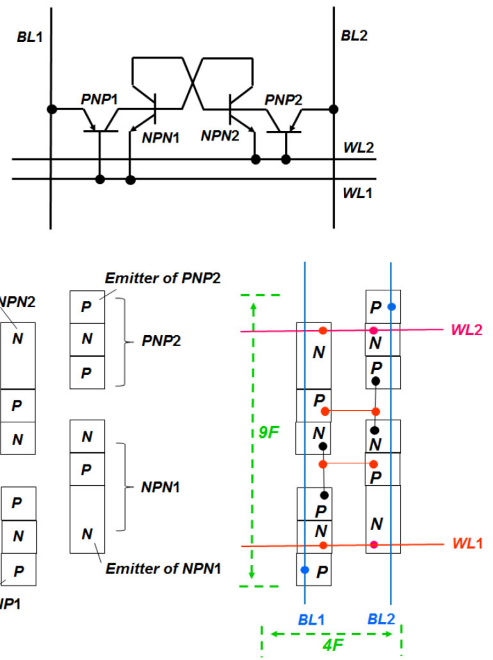

FIGURE 13. Top: Schematic of an I^2L SRAM cell (After [22]). Bottom left: Schematic of SRAM cell layout before any wiring. Bottom right: Schematic of SRAM cell with wire connections, word lines and bit lines. The cell occupies 2 wiring pitches along the word line direction and 4.5 wiring pitches along the bit line direction.

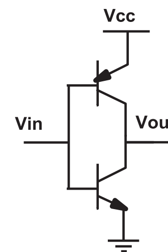

FIGURE 14. Circuit schematic of a complementary bipolar inverter.

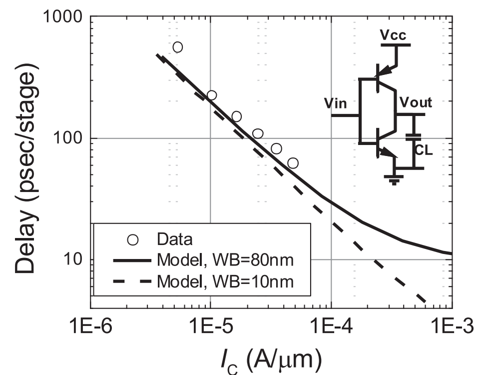

FIGURE 15. Measured 101-stage complementary bipolar inverter delay vs. average I_C. Lines are models. (After [11]).

B. CBIPOLAR CIRCUITS IN SOI SYMMETRIC LATERAL BIPOLAR

The basic building block of a CBipolar circuit is an inverter shown in Fig. 14. In standby, either the NPN or the PNP is in full saturation. Operation of CBipolar inverters in SOI symmetric lateral bipolar has been demonstrated [11], and the reported data are shown in Fig. 15.

A model for estimating the delay and standby power dissipation of CBipolar inverters in SOI symmetric lateral bipolar

has been reported [10]. The average standby current for an inverter is

$$I_{\text{standby}} = (FO + 1)\left(I_{B0npn} + I_{B0pnp}\right) e^{qV_{cc}/kT}, \quad (3)$$

where FO is the number of fan-outs, I_{B0npn} and I_{B0pnp} are the saturated base currents of the NPN and PNP transistors, respectively. In the case of Si-OI transistors, the base current is determined by the injection of carriers from the base into the emitter. Base current due to recombination in the base region is negligible, and base current due to recombination in the base-emitter space-charge region can be made negligibly small by process optimization [26].

Figure 16 shows the simulated delay and standby power vs. V_{cc} for a design using Si-OI. Also shown are two cases of projections for narrow-gap-base HBTs, one for the case of replacing the Si base region with a SiGe base region (with a bandgap 200 meV smaller than Si) and one for the case of replacing the Si base region with a Ge base region (energy bandgap = 0.66 eV). In all cases, the emitter regions remain Si. Such Si-emitter/collector and SiGe- or Ge-base HBTs remain to be demonstrated. The projections are just to see what to expect from such narrow-gap-base HBTs. One ***key assumption*** in Fig. 16 is that the base currents of the SiGe-base and Ge-base transistors are identical to that of the Si-base transistor. This assumption is good only if the base currents are determined by the injection of carrier from the base into the emitter, and if the process for producing the HBTs do not introduce additional base current components. Any additional base current components would increase the standby power of these HBT CBipolar circuits accordingly.

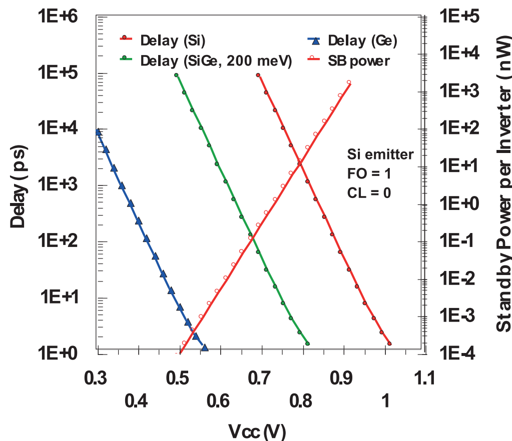

FIGURE 16. Comparison of calculated propagation delay and standby power dissipation for Si homojunction CBipolar with projections for narrow-base heterojunction CBipolar for the case of FO = 1. All devices are assumed to have the same Si emitter region, T_{Si} = 60 nm, L_E = 100 nm, N_B = 1E19 cm^{-3}, and W_B = 10 nm. The Ge-base delay is projected by shifting the Si plot to the left by 0.46 V. The SiGe-base delay is projected by shifting the Si plot to the left by 200 mV, equivalent to assuming the SiGe bandgap to be 200 meV smaller than that of Si. (After [10]).

The results in Fig. 16 show that CBipolar inverters can be fast. The only issue is standby power dissipation at the speed of interest. Let us consider the Si-OI case. With Si-emitter, V_{cc} needs to be < 0.75 V for standby power to be 1 nW per inverter. But the inverter delays at $V_{cc} < 0.75$ V are larger than 10 ns, much too slow for such standby power. However, for applications where performance is not an issues, a Si-OI CBipolar inverter can be operated at 0.5 V with only 0.1 pW standby power, with a delay of about 100 µs.

For applications where both high speed and low standby power are required, we need narrow-gap-base HBT CBipolar, with Si-emitter/collector and SiGe- or Ge base. If such HBTs were available, Fig. 16 suggests inverter delay could be 10 ps at 1 nW for the case of SiGe base and 10 ps at < 0.1 pW for the case of Ge base. These should be attractive power-performance targets for ultra-low-power technologies.

C. PERFORMANCE ON DEMAND

While the focus in advanced CMOS development, and in the search for a "beyond CMOS" technology, has been on ultra-low power dissipation, the need for high-speed systems, or high-speed subsystem within an ultra-low-power system, has not gone away. At the transistor level, it is challenging to develop a CMOS that satisfies the requirements of both high-speed and ultra-low-power systems. CMOS designers typically offer devices with several threshold-voltage options to enable chip designers some room for power-performance tradeoff and optimization. As an example, the published 14-nm FinFET [24] offers a high-speed transistor with about 3x higher on current at about 7000x larger off current than an ultra-low-power transistor. The implication is that a circuit designed in the high-speed transistors is about 3x faster than the same circuit designed in the ultra-low-power transistors by dissipating about 7000x more standby power.

At the system level, when a subsystem or core with higher speed is needed within a system, designers typically insert an accelerator (faster functional core) by packaging method. Another common practice is to enable the system to run in "turbo mode", with most of the cores powered down to enable just one or two cores to run at higher speed. In one four-core chip example [27], when three of the four cores were powered down, the remaining core ran at about 50% higher speed. The implication is that for a CMOS core to increase speed by 1.5x, it take about 4x power dissipation.

I^2L and CBipolar circuits do not employ resistors as loads. The speed of an I^2L or a CBipolar circuit can be dialed up or down simply by adjusting V_{cc}. There is no need to change the transistor size or device design as long as J_C stays below the "maximum without performance degradation" limit. Figures 12 and 16 suggest the possibility of a very large window (more than six orders) for performance vs. power tradeoff by adjusting V_{cc} for the chip or for the various cores on a chip.

The performance-on-demand characteristics of I^2L and CBipolar represent an intriguingly interesting opportunity to system designers. For example, one could imagine a processor chip containing many cores, with most cores running at base speed in ultra-low-power mode, some cores running

at 100x base speed, and a couple of cores running at 1,000x base speed as accelerators.

The performance-on-demand of an I^2L 1024 divider circuit was demonstrated in vertical bipolar [20]. The operating frequency of the divider was changed from 10 MHz to 1.2 GHz simply by changing the PNP injector current. The highest operating frequency (1.2 GHz) was limited by the fact that vertical bipolar was used.

VI. LOW-POWER I/O AND CLOCK DRIVER CIRCUITS

From a system perspective, it is not enough to consider just the power dissipation needed for computation. The power dissipation of the clock circuits for synchronizing the various operations and the I/O circuits for communication off chip must be included. The transistors for these circuits need to deliver large currents, and hence are large in area. CMOS I/O transistors typically have drive-current capability of about 1 mA/μm. As discussed in Section III-A, SOI lateral bipolar transistors could have drive-current capability of about 10 mA/μm. Therefore, compared to CMOS, SOI lateral bipolar clock and I/O circuits have much smaller area and associated capacitances, implying much lower power dissipation.

VII. SUBSTRATE AS A FOURTH DEVICE TERMINAL

The SOI substrate can be used as a fourth device terminal to further improve device characteristics [28]. Figure 17 shows that a positive substrate bias greatly increases the collector current of a NPN transistor but has little effect on its base current. Similarly, a negative substrate bias greatly increases the collector current of a PNP transistor but has little effect on its base current. In other words, the SOI substrate can be used to induce narrow-gap-base HBT-like characteristics, i.e., devices with very large current gains, in homojunction SOI lateral bipolar transistors. Figure 17 suggest current gains of greater than 10,000 should be achievable.

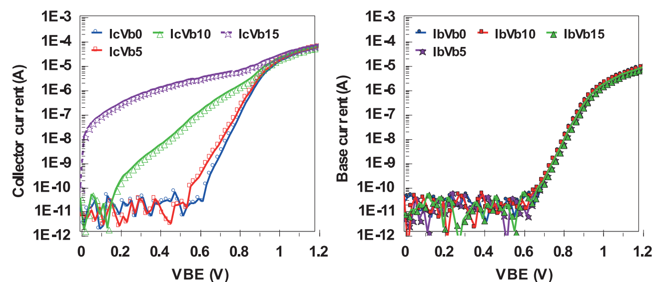

FIGURE 17. Typical effect of a positive substrate bias (from 0 to 15 V in 5-V steps) on the collector current (left) and base current (right) of a Si-OI symmetric lateral NPN transistor. The currents were measured at $V_{BC} = 0$. The transistor has $N_E = 2E20\ cm^{-3}$ and $N_B = 2.5E18\ cm^{-3}$. The BOX thickness is about 140 nm. (After [27]).

As long as the BOX is not too thin, say thicker than 20 nm, the application of a substrate bias does not change the device capacitance. The increased I_C should lead to higher circuit speed. Alternatively, for ultra-low-power applications, the increased I_C could be traded off for lower V_{cc} and lower standby power.

VIII. CONCLUSION

Circuits and systems designed using vertical bipolar transistors can be fast but dissipate very large power, making vertical bipolar of little interest for digital applications. SOI symmetric lateral bipolar greatly reduces the power dissipation of commonly used bipolar circuits. It also enables circuits that operate with $V_{cc} = V_{BE}$ to be high speed.

SOI lateral bipolar I^2L SRAM cells could be more than twice as dense as standard CMOS SRAM cells. An I^2L gate could achieve a power-delay product of about 10 aJ, with minimum delay < 10 ps. CBipolar inverters could operate with a standby power of only 1 pW, but inverter speed would depend on the device technology. If Si-emitter/collector and SiGe-base HBTs were available, the inverter speed could be about 10 ns. If Si-emitter/collector and Ge-base HBTs were available, the inverter speed could be < 10 ps. The substrate of a SOI lateral bipolar transistor can be used as a fourth device terminal to induce large increase in current gain for additional speed improvement.

From a system perspective, the huge range of power vs. performance tradeoff available to I^2L and CBipolar circuits offers an intriguing opportunity to designers of ultra-low-power systems. One could imagine a processor chip with most cores running in ultra-low-power mode, but a few cores running at much higher speed and power to enable overall high system throughput at low power.

The novel SOI lateral bipolar is CMOS compatible. Narrow-gap-base HBTs have not been reported yet, so it is hard to gauge their process complexity. However, processes for homojunction Si-OI and SiGe-OI lateral bipolar are definitely less complex than CMOS process.

SOI lateral bipolar appears to be a technology that is suitable for high-speed computing systems, high-frequency electronic systems, and ultra-low-power systems with embedded high-speed cores. What is needed is increased R&D effort to evaluate and demonstrate the advantage of this technology for real system applications.

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