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Proposal of Physics-Based Equivalent Circuit of Pseudo-MOS Capacitor Structure for Impedance Spectroscopy

ISAO YARITA, (Student Member, IEEE), SHINGO SATO, (Member, IEEE), AND YASUHISA OMURA, (Fellow, IEEE)

Faculty of Engineering Science, Kansai University, Osaka 564-8680, Japan

CORRESPONDING AUTHOR: S. SATO (e-mail: satos@kansai-u.ac.jp)

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ABSTRACT This paper proposes a detailed equivalent circuit of the pseudo-MOS capacitor structure and subjects it to impedance spectroscopy. We find, using Cole–Cole plots, that three resistance components, which correspond to interface traps, contact resistance, and bulk traps created near the contact, are observed in measurements of a silicon-on-insulator wafer. The simulation results gained from the detailed equivalent circuit proposed here well match the measurement results over the wide frequency range examined.

INDEX TERMS Silicon-on-insulator (SOI), pseudo-MOSFET, impedance spectroscopy, Cole-Cole plot.

I. INTRODUCTION

In recent years, silicon-on-insulator (SOI) Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) have been applied to digital integrated circuits to realize various low-power devices [1]. Since the performance of the SOI MOSFET is sensitive to the quality of the SOI wafer, we need a reliable method that can confirm its many physical parameters before subsequent device processing. One of the most interesting technologies is the pseudo (Ψ)-MOSFET, which inverts the structure of the conventional MOSFET and makes it possible to evaluate the low-field mobility simply by loading the metal probes onto the top SOI film of the SOI wafer without any manufacturing process [2]. A recent article subjected the Ψ-MOS capacitor structure to capacitance measurements to extract the interface-trap information of the SOI wafer, and the influence of the contact resistance which includes the access resistance has been already clarified [3], [4]. Previous studies [3], [4] proposed the equivalent circuit that combines, in series, the capacitance of the buried oxide and the resistance near the contact on the SOI film. This circuit for the Ψ-MOS capacitor structure successfully explains the frequency dependency of its capacitance. However, this equivalent circuit is so simple that it fails to consider the ac response resulting from interface traps, bulk traps and so on. The conditions (thickness, doping, trap density, etc) for which the enriched model provides additional information need to be given. A comprehensive model based on the physical mechanisms of the ac response for the Ψ-MOS capacitor structure must be constructed to evaluate SOI wafer quality as soon as possible.

This paper analyzes the impedance of the Ψ-MOS capacitor structure as a function of the frequency using Cole-Cole plots, which is proposed by Cole and Cole and reveals the relationship between the real and the imaginary parts of the physical component [5], and then proposes a physics-based equivalent circuit of the Ψ-MOS capacitor structure. The dominant physical mechanism over a wide frequency range is clarified. The small capacitance component, of the order of pico farad and cannot be elucidated by conventional C-V measurements, is revealed when the resistance components are comparable to each other. This paper demonstrates the validity of the advanced Ψ-MOS based parameter extraction technique based on Cole-Cole plots.

II. MEASUREMENT SETTING

Electrical characteristics are accurately measured using the four probe station provided by HiSOL, Inc. and a hand-made conduction vacuum chuck made of Aluminum [6]. The probes are made of tungsten carbide. The probe radius

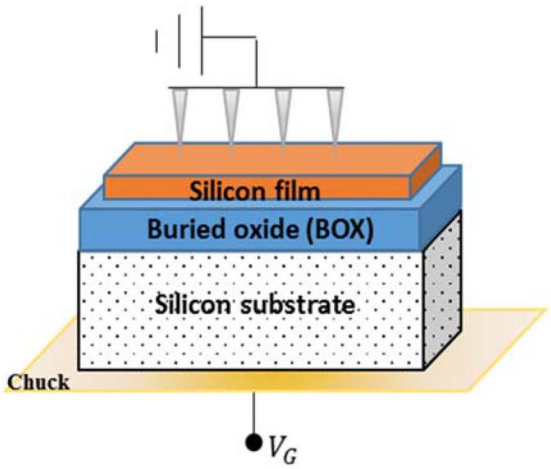

FIGURE 1. Ψ-MOS capacitor structure in measuring capacitance and impedance.

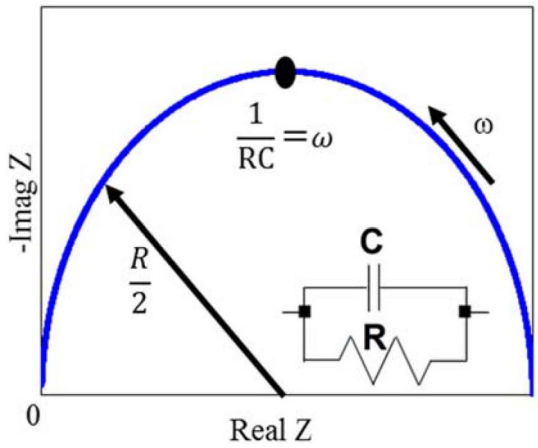

FIGURE 2. Cole-Cole plot of a simple RC parallel circuit.

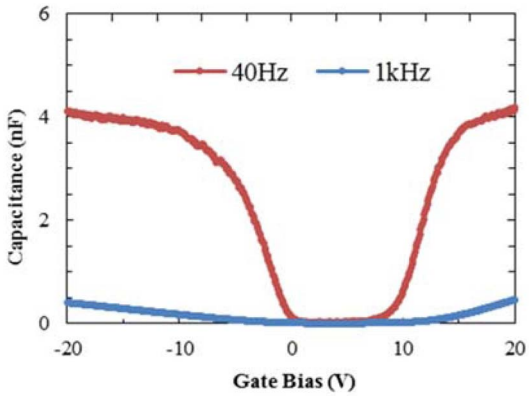

FIGURE 3. C-V characteristics of Ψ-MOS capacitor structure for two different frequencies.

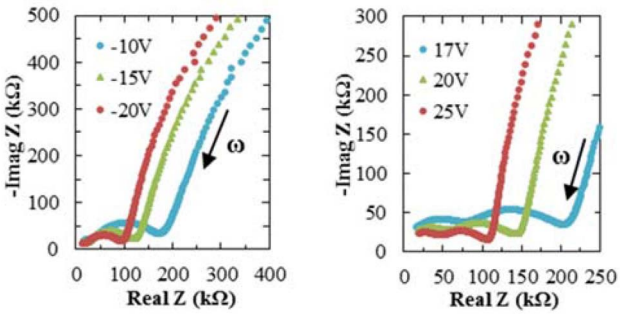

FIGURE 4. Impedance of Ψ-MOS capacitor structure on Cole-Cole plot with gate bias as the parameter. (a) negative gate biases, (b) positive gate biases.

is 40 μm and the probe pressure is 85 g. The probe pitch is 1.27 mm. The whole probe station is covered with a shield-box to suppress electrical and optical noises.

A 4-inch bonded SOI wafer is used without creating any Si islands. Nominal thicknesses of the SOI and Buried oxide (BOX) layers are 2.0 μm and 1.0 μm, respectively. Both the SOI layer and the substrate have resistivity of 1∼10 Ωcm and p-type polarity.

An Agilent 4294A precision impedance analyzer is used to analyze the ac response of the Ψ-MOS capacitor structure. Figure 1 shows the Ψ-MOS capacitor structure when measuring the ac response. Constant dc voltage for V_G (gate bias) and superimposed ac signal are applied to the substrate of SOI wafer (called the gate here). The frequency of the ac signal is swept from 40 Hz to 2 MHz. The amplitude of the ac signal is 20 mV. The capacitance given by the Pseudo-MOS capacitor structure is measured as a function of the gate voltage (V_G) using the C_p-G_p parallel-circuit model. The impedance given by the Pseudo-MOS capacitor structure is measured as a function of the frequency using the |Z|-θ model. Cole-Cole plots are drawn by plotting the real and imaginary parts of the impedance on the complex plane and a semicircle is found on the plane when the material behaves as a parallel circuit of resistance R and capacitance C, as shown in Fig. 2. Impedance (Z) of the RC parallel circuit is expressed as

$$\mathrm{Z}=\frac{R}{1+\omega^2C^2\mathrm{R}^2}-\mathrm{j}\frac{\omega CR^2}{1+\omega^2C^2\mathrm{R}^2}. \quad (1)$$

The semicircle gives the following relation.

$$\left(\mathrm{Real\ Z}-\frac{R}{2}\right)^2+\mathrm{Imag\ Z}^2=\left(\frac{\mathrm{R}}{2}\right)^2 \quad (2)$$

According to eq. (2), the radius of the semicircle gives the half value of the resistance component (R/2), and its peak frequency is expressed as f_p=ω/2π=1/(2πRC) [7]–[9].

III. RESULTS AND DISCUSSION

Figure 3 shows the measured capacitance of the Ψ-MOS capacitor structure at two frequencies. At the high frequency, the measured capacitance degrades due to the contact resistance as already reported in [3] and [4].

Figures 4(a) and 4(b) show the Cole-Cole plot of the measured impedance with the parameter of negative and positive gate biases (V_G). Three semicircles are found in

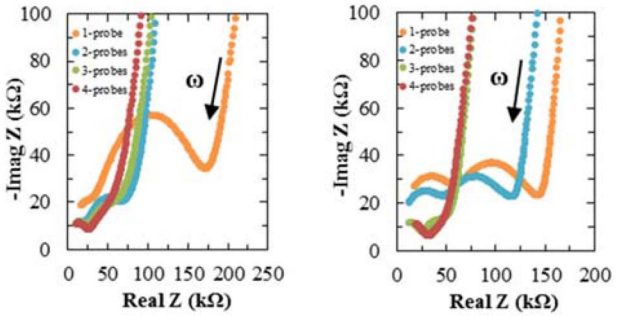

FIGURE 5. Impedance of Ψ-MOS capacitor structure on Cole-Cole plot with probe number as the parameter. (a) negative gate biases, (b) positive gate biases.

the low, middle and high frequency ranges. The radii of semicircles in the middle and high frequency ranges have decreased as the absolute value of the gate bias increases. Figures 5(a) and 5(b) show the Cole-Cole plot with the parameter of the probe number at gate biases of -10V and 20V. Since the radius of the semicircle in the middle frequency range decreases as probe number increases, it is expected that the resistance component in the middle frequency range is responsible for the contact resistance between the probe and SOI layer [3]. This is acceptable because multiple probes form a parallel circuit. We discovered that that the capacitance component of the semicircle in the high frequency range is almost independent of the gate bias (a few pF). It is expected that the capacitance component stems from the current component flowing on the top surface of the SOI wafer because of its rapid response to the high frequency signal. By the surface ac current, we mean the displacement current of the surface charge of the SOI wafer. It is anticipated that such displacement of the surface charge consists of an additional capacitance component to the substrate. This capacitance component is, for the Ψ-MOS capacitor structure, so small that it is difficult to extract from the standard C-V curve, but it is successfully shown with the Cole-Cole plot for the first time. Since the resistance component of the semicircle in the high frequency range strongly depends on gate bias, this resistance component is not primarily due to the substrate resistance. We guess that the resistance component is created by the bulk traps formed by the pressure of the probes. The resistance component stemming from the contact and the bulk traps strongly depends on the magnitude of the gate voltage [10]. It is anticipated that the semicircle in the low frequency range stems from interface traps between the SOI layer and the BOX layer or between the BOX layer and the substrate as already reported in the analysis of standard MOSFET [10], [11].

IV. EQUIVALENT CIRCUIT MODEL

Figure 6 shows the equivalent circuit proposed in previous studies [3], [4]. The calculation result yielded the model given by Fig. 6 is shown by the solid line in Fig. 7 for comparison with the experimental result. Parameter values

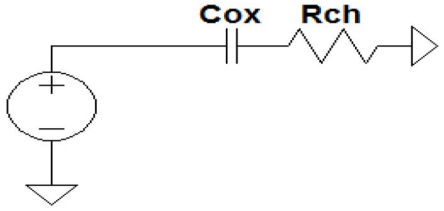

FIGURE 6. The equivalent circuit of Ψ-MOS capacitor structure assumed in [3] and [4].

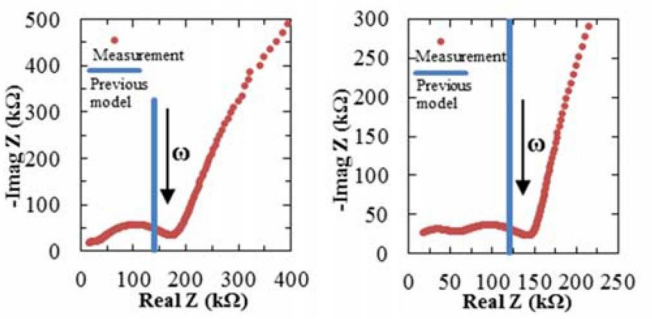

FIGURE 7. Comparison of the experimental result and the calculation result based on the model shown in [3] and [4]. (a) negative gate bias, (b) positive gate bias.

TABLE 1. Parameter values calibrated for the simulations.

Parameters	Values		Method
	accumulation	inversion	
Rpr	140[kΩ]	120[kΩ]	meas.
Cpr	10[pF]	10[pF]	meas.
Rit	70[kΩ]	140[kΩ]	meas.
Cssoi	0.3[nF]	11[nF]	theory
Ritsoi	50[kΩ]	300[kΩ]	meas.
Citsoi	800[nF]	1000[nF]	meas.
Cssb	9[nF]	0.5[nF]	theory
Ritsb	280[kΩ]	30[kΩ]	meas.
Citsb	1000[nF]	800[nF]	meas.
Rpa	3.8[kΩ]	3.8[kΩ]	meas.
Cpa	2.5[pF]	2.1[pF]	meas.
Cox	12[nF]	12[nF]	meas.

assumed for R_{ch} and C_{ox} are equal to those for R_{pr} and C_{ox} summarized in Table 1. The model shown in Fig. 6 does not result in any semicircles in Fig. 7 because the model has no parallel circuit of resistance R and capacitance C. This reveals that the equivalent circuit model proposed here is superior to that shown in Fig. 6 [3], [4]. Our impedance analysis yielded the physics-based equivalent circuit of the Ψ-MOSFET proposed in Fig. 8. C_{ox} is the capacitance of the BOX layer. C_{ssb} and C_{ssoi} are the semiconductor capacitance of the substrate and the SOI layer itself, respectively. C_{itsb} and R_{itsb} are the capacitance and resistance components associated with the interface traps at the BOX layer/substrate interface. C_{itsoi} and R_{itsoi} are the capacitance and resistance components associated with the interface traps at the SOI layer/BOX layer interface. R_{pr} is the contact resistance. C_{pr} and R_{it} are the capacitance and resistance components associated with bulk traps created near the probe contact. C_{pa} and

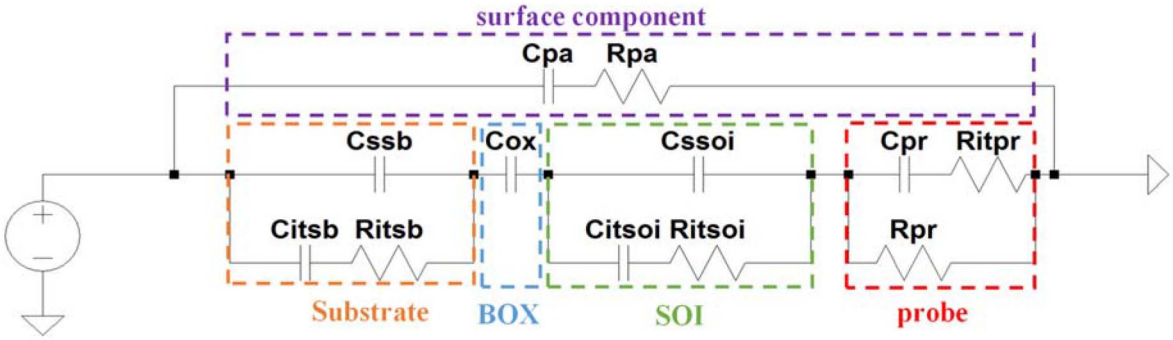

FIGURE 8. Equivalent circuit of Ψ-MOS capacitor structure based on impedance analysis.

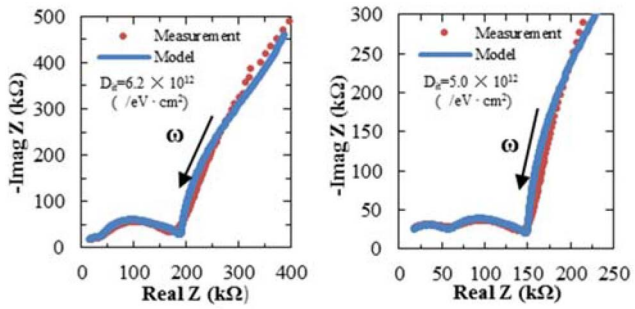

FIGURE 9. Comparison between the measured values and the predicted curve. (a) negative gate bias, (b) positive gate bias.

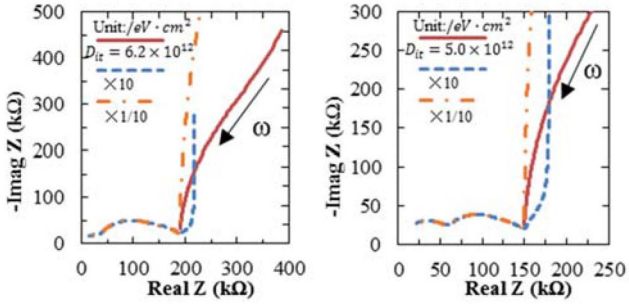

FIGURE 10. Simulated Cole-Cole plot as a parameter of the interface trap density Dit with constant time constant. (a) negative gate bias, (b) positive gate bias.

R_{pa} are the capacitance and resistance components associated with the current flowing on the top surface of the SOI wafer. When the frequency of the applied ac voltage is low, the impedance yielded by C_{pr} and R_{it} is very large in comparison to R_{pr}. In the same way, the impedance yielded by C_{pa} and R_{pa} is also very large in comparison to the impedance of the SOI wafer itself. By eliminating the ac response of the interface traps, the model proposed here is reduced to the simplified model [3], [4].

Figures 9(a) and 9(b) show the simulation results corresponding to Fig. 8 for V_G = -10V (accumulation near the SOI layer/BOX layer interface and depletion near the BOX layer/substrate interface) and V_G = 20V (depletion near the SOI layer/BOX layer interface and accumulation near the BOX layer/substrate interface). The parameter values assumed here are shown in Table 1. Values of C_{ssb} and C_{ssoi} are estimated from the doping concentration of each layer. Values of C_{itsb} and C_{itsoi} are calculated by assuming that the interface trap density is of the order of 10^{12}/eV·cm^2. Maximal error between the simulation result and the measurement result is less than 10 % over the whole frequency range. The simulation results successfully trace the measurement results for both negative and positive gate bias conditions over the wide frequency range examined. The equivalent circuit proposed here will be applicable to the analysis of wafers with an ultrathin SOI layer although the adjustment of some parameters, for example the decrease and increase in the contact resistance and the depletion capacitance, will be needed.

Figures 10(a) and 10(b) show the simulation results of the Cole-Cole plots for V_G = -10V and V_G = 20V with the parameter of interface trap density; the time constant with a constant value is a tentative assumption. Numerical orders of the interface trap densities at the BOX layer/substrate interface and at the SOI layer/BOX interface are modified.

The aspect of the change in the curve's shape is almost identical between Figs. 10(a) and 10(b). In the case of high interface trap density, the radius of the semicircle in the low frequency range is diminished because we do not assume a variable time constant tentatively. In addition, the total resistance between the gate terminal (the chuck stage) and the contact (the probe) decreases. Therefore, the influence of the impedance component ($1/j\omega C_{ox}$) appears in the Cole-Cole plot curve. On the other hand, the radius of the semicircle in the low frequency range increases in the case of low interface trap density. Thus, the Cole-Cole plot for the Ψ-MOS capacitor structure enables advanced parameter extraction for the interface trap density by carefully fitting the experimental result to the circuit model proposed here for both the resistance component and the capacitance component.

V. CONCLUSION

Various aspects of the ac impedance of the Ψ-MOS capacitor structure were analyzed. Three semicircles, which

correspond to interface traps, probe contact resistance, and bulk traps, were found in Cole-Cole plots created from low, middle and high frequency range measurements. Simulations using the physics-based equivalent circuit model proposed here successfully matched the measurement results over a wide range of frequencies. The equivalent circuit model proposed here will enable us to quantitatively extract physical parameters of SOI wafers like interface trap density from their Cole-Cole plots.

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ISAO YARITA (S'15) was born in Osaka, Japan, in 1993.

He received the B.S. degree from the Faculty of Electrical and Electronic Information Engineering, Kansai University, Osaka, in 2016, where he is currently pursuing the M.S. degree in electrical engineering.

His current research interests include characterization and parameter extraction of the SOI wafer using impedance spectroscopy.

SHINGO SATO was born in Osaka, Japan, in 1981. He received the B.S., M.S., and Ph.D. degrees in electronics from Kansai University, Osaka, in 2003, 2005, and 2008, respectively.

In 2008, he joined Renesas Technology Corporation, Hyogo, Japan, where he was involved in the development of the manufacturing process for SoC, microprocessor, and CMOS image sensor. In 2013, he moved from Renesas Electronics Corporation, Hyogo, to Kansai University.

His current research interests include MOS device physics and material characterization and modeling.

YASUHISA OMURA (M'85–SM'97–F'10) received the M.S. degree in applied science and the Ph.D. degree in electronics from Kyushu University, Japan, in 1975 and 1984, respectively. He joined the Musashino Electrical Communications Laboratories, NTT, Tokyo, Japan, in 1975. He worked on short-channel CMOS/SIMOX design, LSI processing, and SOI device modeling. In NTT, he contributed to trial demonstrations of CMOS/SIMOX SRAM on the device design and fabrication processing. He moved his position from NTT Atsugi Research and Development Center to Kansai University, Osaka, as a Professor, in 1997, and he is currently working on device physics of ultimately miniaturized MOSFET/SOI, device modeling for MOS device design, and fluctuation physics. He has published 150 regular papers and 180 conference proceedings. He is one of co-authors having published the book entitled *Device and Circuit Cryogenic Operation for Low Temperature Electronics* (Kluwer Academic, 2001), *Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications* (Springer, 2006), and has authored the book entitled *SOI Lubistors: Lateral, Unidirectional, Bipolar-Type, Insulated-Gate Transistor* (IEEE/Wiley, 2013).

He served as a Committee Member for the Technical Committee of the IEEE International SOI Conference, from 1997 to 1998, and the Program Committee of International Symposium on VLSI Technology, from 1997 to 2006. He also served as the lead organizer for the Electrochemical Society Symposium, from 2009 to 2015. He has been serving as an International Advisory Member for the Program Committee of International Workshop on Low-Temperature Electronics, since 1998. From 2007 to 2010, he shared the Vice Chair and the Chair of IEEE EDS Kansai Chapter and the Conference Chair of the IEEE IMFEDK since 2009.

Dr. Omura is a Regular Member of the Japan Society of Applied Physics, the Electrochemical Society and the Institute of Electronics, Information and Communication Engineers.